

RJK5026DPP

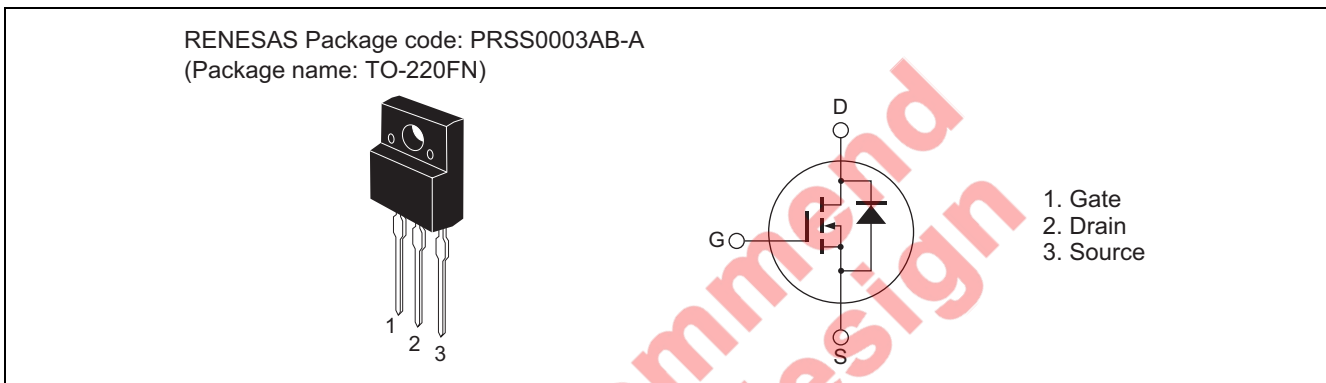
Silicon N Channel MOS FET
High Speed Power Switching

R07DS0360EJ0200
(Previous: REJ03G1734-0100)
Rev.2.00
Apr 15, 2011

Features

- Low on-resistance
 $R_{DS(on)} = 1.35 \Omega$ typ. (at $I_D = 3 A$, $V_{GS} = 10 V$, $T_a = 25^\circ C$)
- Low leakage current
- High speed switching

Outline



Absolute Maximum Ratings

($T_a = 25^\circ C$)

| Item | Symbol | Ratings | Unit |
|---|----------------------------------|-------------|--------------|
| Drain to source voltage | V_{DSS} | 500 | V |
| Gate to source voltage | V_{GSS} | ± 30 | V |
| Drain current | I_D ^{Note4} | 6 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | 18 | A |
| Body-drain diode reverse drain current | I_{DR} | 6 | A |
| Body-drain diode reverse drain peak current | $I_{DR(pulse)}$ ^{Note1} | 18 | A |
| Avalanche current | I_{AP} ^{Note3} | 4 | A |
| Avalanche energy | E_{AR} ^{Note3} | 0.88 | mJ |
| Channel dissipation | P_{ch} ^{Note2} | 28.5 | W |
| Channel to case thermal impedance | θ_{ch-c} | 4.38 | $^\circ C/W$ |
| Channel temperature | T_{ch} | 150 | $^\circ C$ |
| Storage temperature | T_{stg} | -55 to +150 | $^\circ C$ |

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. $ST_{ch} = 25^\circ C$, $T_{ch} \leq 150^\circ C$
 4. Limited by maximum safe operation area

Electrical Characteristics

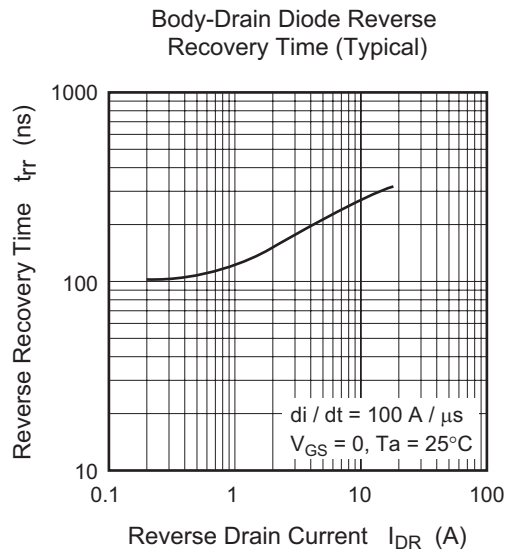
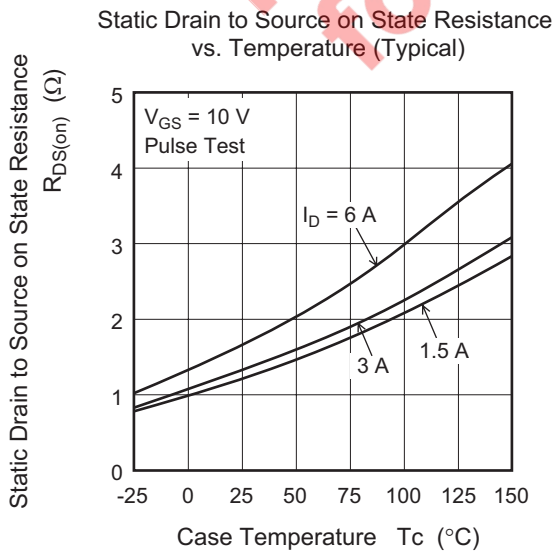
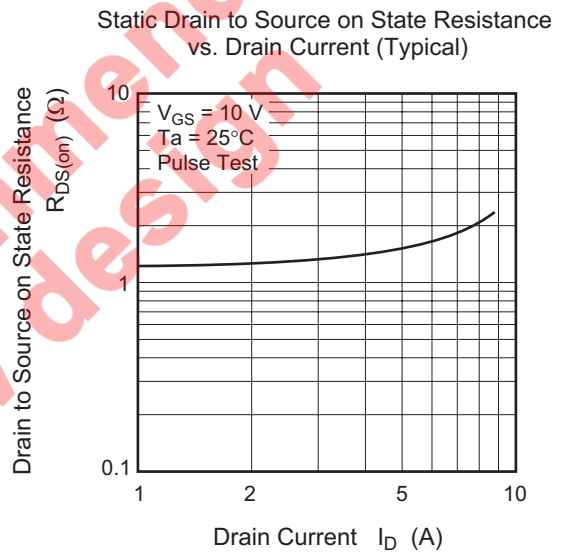
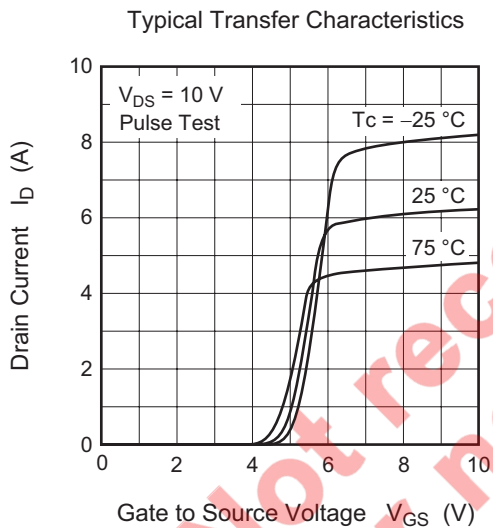
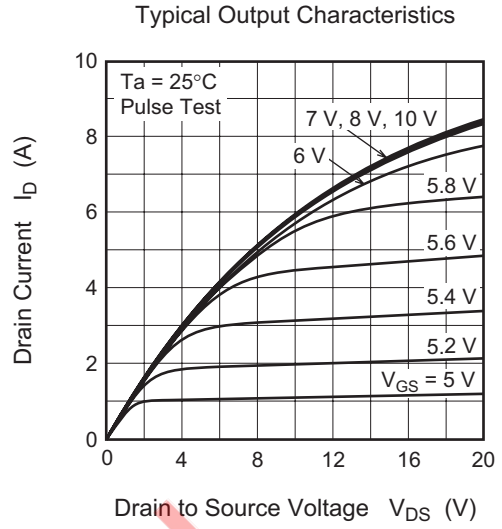
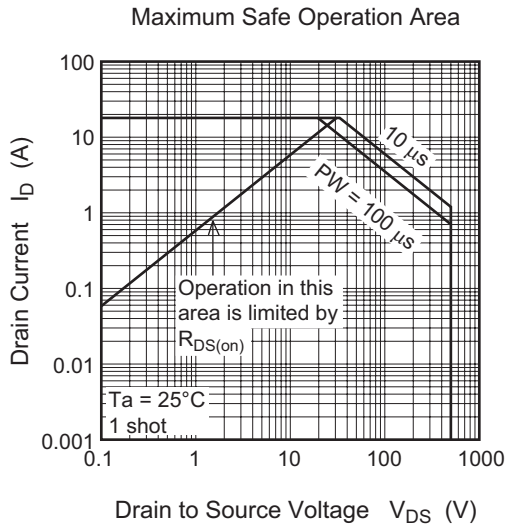
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|-----|------|-----------|---------------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 500 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 500 \text{ V}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 0.1 | μA | $V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 3.0 | — | 4.5 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 1.35 | 1.70 | Ω | $I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note5} |
| Input capacitance | C_{iss} | — | 440 | — | pF | $V_{DS} = 25 \text{ V}$ |
| Output capacitance | C_{oss} | — | 52 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 7 | — | pF | $f = 1 \text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 26 | — | ns | $I_D = 3 \text{ A}$ |
| Rise time | t_r | — | 19 | — | ns | $V_{GS} = 10 \text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 50 | — | ns | $R_L = 83.3 \Omega$ |
| Fall time | t_f | — | 14 | — | ns | $R_g = 10 \Omega$ |
| Total gate charge | Q_g | — | 14 | — | nC | $V_{DD} = 400 \text{ V}$ |
| Gate to source charge | Q_{gs} | — | 2.5 | — | nC | $V_{GS} = 10 \text{ V}$ |
| Gate to drain charge | Q_{gd} | — | 6.9 | — | nC | $I_D = 6 \text{ A}$ |
| Body-drain diode forward voltage | V_{DF} | — | 0.95 | 1.50 | V | $I_F = 6 \text{ A}$, $V_{GS} = 0$ ^{Note5} |
| Body-drain diode reverse recovery time | t_{rr} | — | 230 | — | ns | $I_F = 6 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$ |

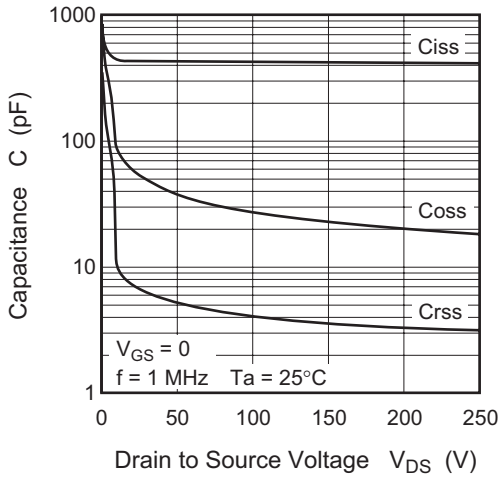
Notes: 5. Pulse test

Not recommended
for new designs

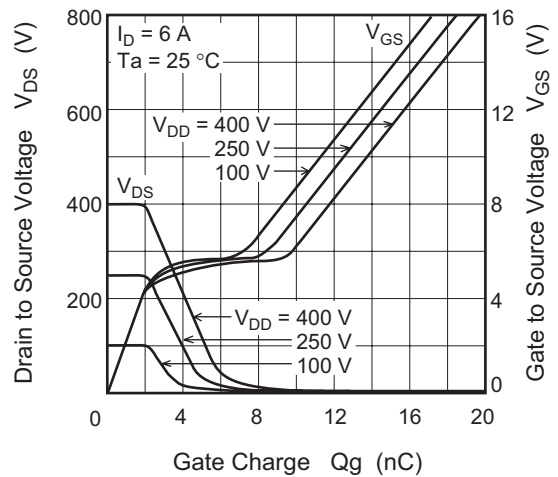
Main Characteristics



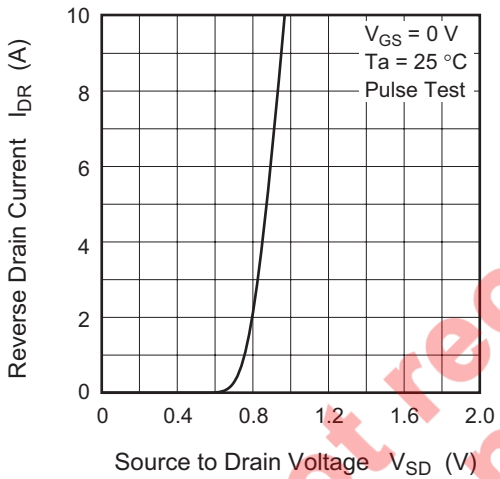
Typical Capacitance vs. Drain to Source Voltage



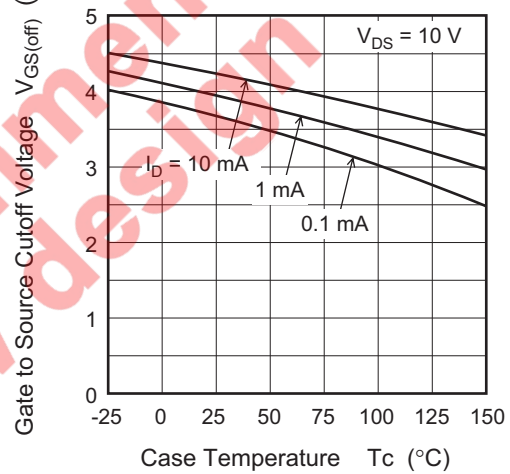
Dynamic Input Characteristics (Typical)



Reverse Drain Current vs. Source to Drain Voltage (Typical)

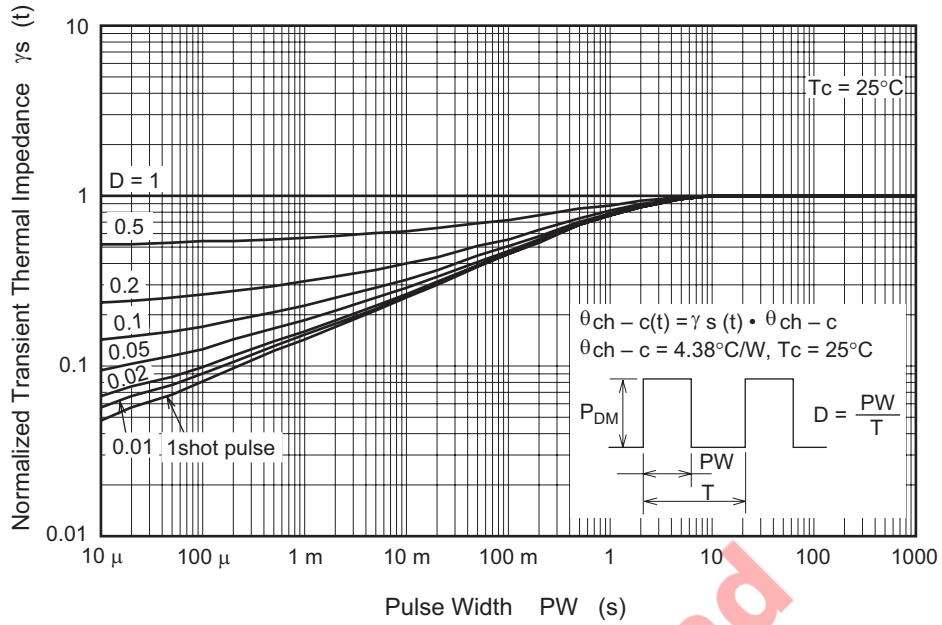


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

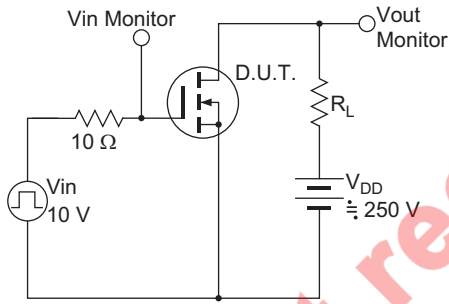


Not recommended for new designs

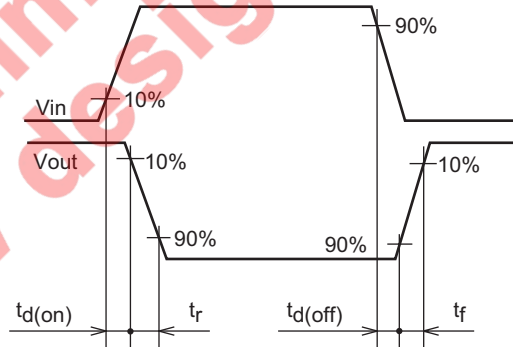
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

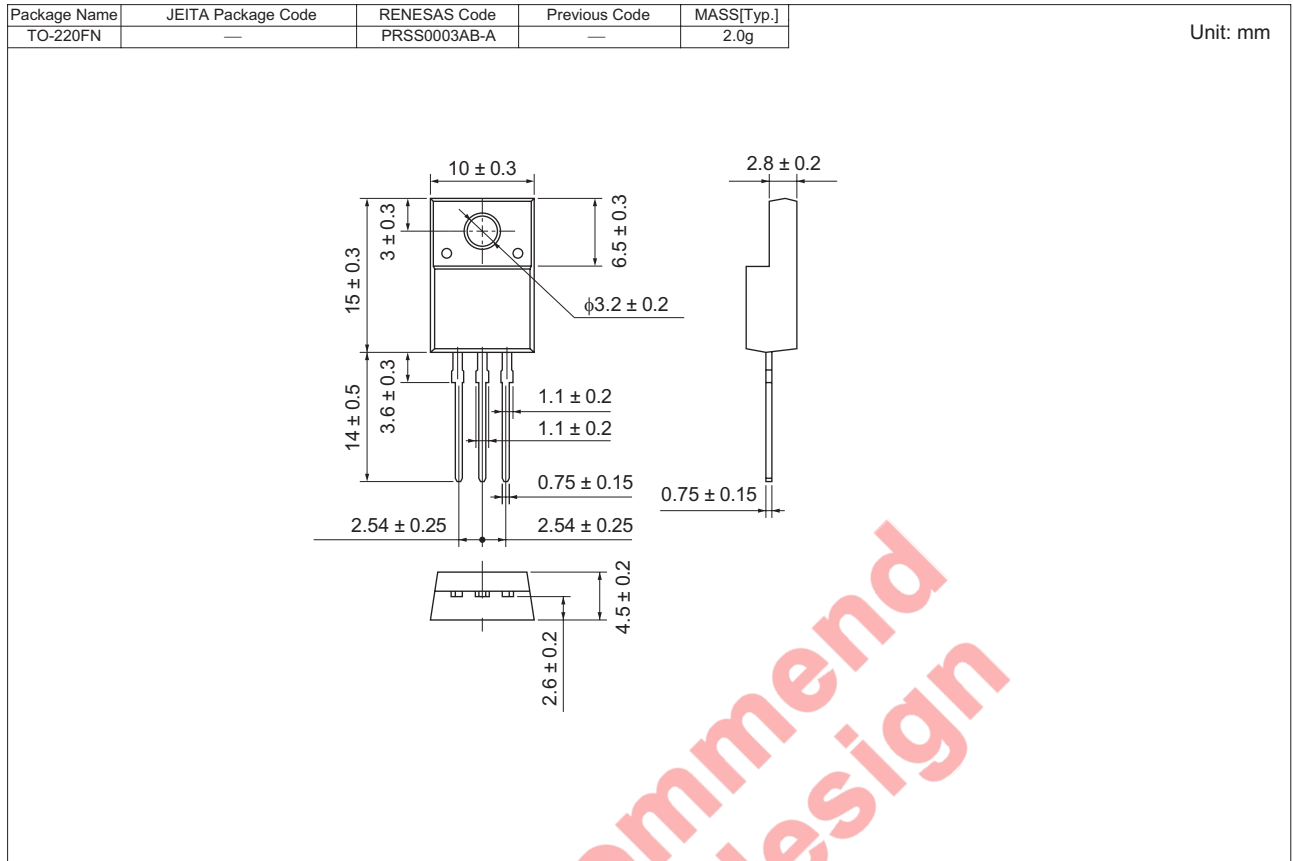


Waveform



Not recommended for new design

Package Dimensions



Ordering Information

| Orderable Part Number | Quantity | Shipping Container |
|-----------------------|----------|--------------------|
| RJK5026DPP-00-T2 | 1050 pcs | Box (Tube) |
| RJK5026DPP-E0-T2 | 1050 pcs | Box (Tube) |

Not recommend
for new design

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