- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT533 . . . J OR W PACKAGE
SN74ABT533A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20 V_{CC}
$1\overline{Q}$	2	19 $8\overline{Q}$
1D	3	18 8D
2D	4	17 7D
$2\overline{Q}$	5	16 $7\overline{Q}$
$3\overline{Q}$	6	15 $6\overline{Q}$
3D	7	14 6D
4D	8	13 5D
$4\overline{Q}$	9	12 $5\overline{Q}$
GND	10	11 LE

SN54ABT533 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D, $1\overline{Q}$, $\overline{OE}$, V_{CC}, $8\overline{Q}$ (pins 3, 2, 1, 20, 19)
Left side: 2D (4), $2\overline{Q}$ (5), $3\overline{Q}$ (6), 3D (7), 4D (8)
Right side: 8D (18), 7D (17), $7\overline{Q}$ (16), $6\overline{Q}$ (15), 6D (14)
Bottom pins: $4\overline{Q}$ (9), GND (10), LE (11), $5\overline{Q}$ (12), 5D (13)

description

These octal transparent D-type latches with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse of the levels at the D inputs.
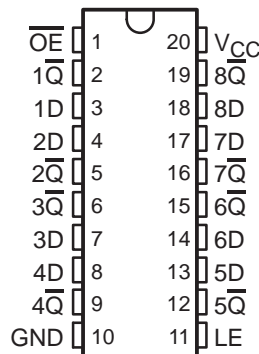
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.
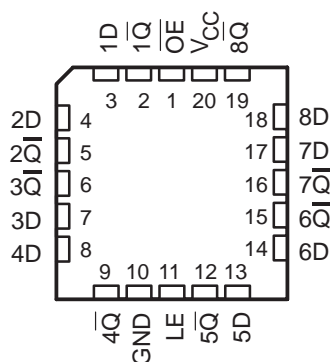
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT533 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT533A is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol[†]

logic diagram (positive logic)

To Seven Other Channels
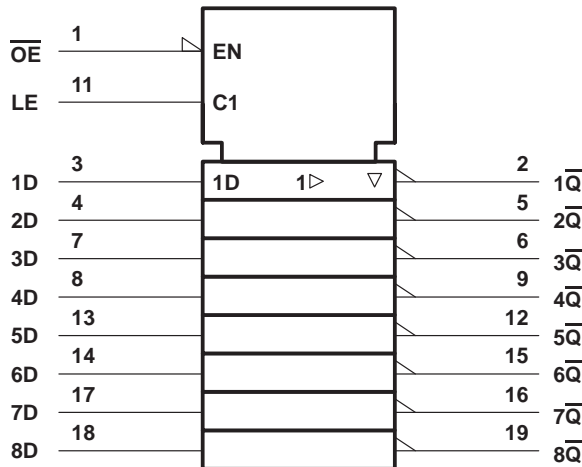
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
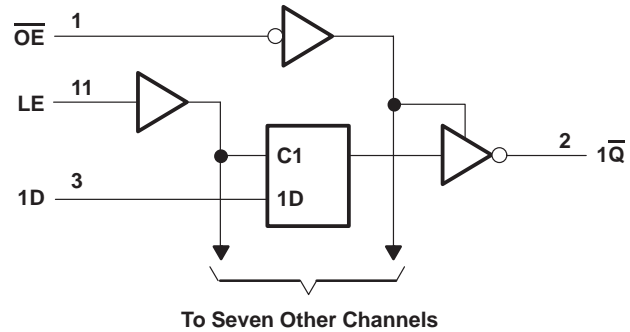
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT533 . . . . 96 mA
                                                            SN74ABT533A . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 115°C/W
                                                          DW package . . . . 97°C/W
                                                          N package . . . . 67°C/W
                                                          PW package . . . . 128°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
            2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT533 MIN	SN54ABT533 MAX	SN74ABT533A MIN	SN74ABT533A MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3:   Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP†	$T_A = 25°C$ MAX	SN54ABT533 MIN	SN54ABT533 MAX	SN74ABT533A MIN	SN74ABT533A MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = −18$ mA				−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = −3$ mA		2.5			2.5		2.5		V
	$V_{CC} = 5$ V, $I_{OH} = −3$ mA		3			3		3		
	$V_{CC} = 4.5$ V	$I_{OH} = −24$ mA	2			2				
		$I_{OH} = −32$ mA	2*					2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
		$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}				100						mV
I_I	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V				10		10		10	µA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.5$ V				−10		−10		−10	µA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±150				±150	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡	$V_{CC} = 5.5$ V, $V_O = 2.5$ V		−50	−140	−180	−50	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}§	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs high			1.5		1.5		1.5	mA
		Outputs low			1.5		1.5		1.5	
		Outputs disabled			1.5		1.5		1.5	
C_i	$V_I = 2.5$ V or 0.5 V			3.5						pF
C_o	$V_O = 2.5$ V or 0.5 V			6.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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INSTRUMENTS

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT533				UNIT
			$V_{CC} = 5$ V, $T_A = 25°C$		MIN	MAX	
			MIN	MAX			
t_w	Pulse duration, LE high		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High or low	2.1		2.1		ns
t_h	Hold time, data after LE↓	High or low	1.5		1.5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT533A				UNIT
			$V_{CC} = 5$ V, $T_A = 25°C$		MIN	MAX	
			MIN	MAX			
t_w	Pulse duration, LE high		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High or low	2.1		2.1		ns
t_h	Hold time, data after LE↓	High or low	2.1		2.1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT533					UNIT
			$V_{CC} = 5$ V, $T_A = 25°C$			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	$\overline{Q}$	1.9	4.2	5.4	1.9	6.7	ns
t_{PHL}			3.1	4.9	6.3	3.1	6.9	
t_{PLH}	LE	$\overline{Q}$	2.7	4.9	6.2	2.7	7.6	ns
t_{PHL}			3.5	5.4	6.8	3.5	7.5	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	1.6	3.7	4.8	1.6	5.8	ns
t_{PZL}			2.4	4.2	6.2	2.4	6.9	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	2.8	5.1	6.2	2.8	7.2	ns
t_{PLZ}			2	4.1	6	2	6.9	

TEXAS
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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT533A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	$\overline{Q}$	1.7	4.2	5.4	1.7	6.4	ns
t_{PHL}			2.6	4.9	6.3	2.6	6.6	
t_{PLH}	LE	$\overline{Q}$	2.7	4.9	6.2	2.7	7.3	ns
t_{PHL}			3.5	5.4	6.8	3.5	7.3	
t_{PZH}	$\overline{OE}$	$\overline{Q}$	1.6	3.7	4.8	1.6	5.7	ns
t_{PZL}			2.4	4.2	6.2	2.4	6.7	
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	1.6	5.1	6.2	1.6	6.9	ns
t_{PLZ}			2	4.1	6	2	6.5	

PARAMETER MEASUREMENT INFORMATION

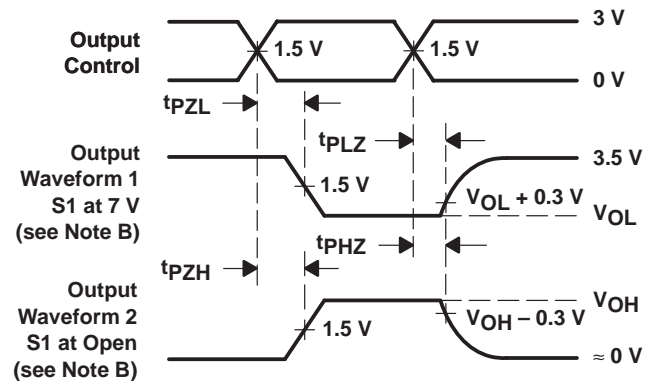| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9584301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9584301Q2A SNJ54 ABT533FK	Samples
5962-9584301QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9584301QRA SNJ54ABT533J	Samples
SN74ABT533AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT533AN	Samples
SN74ABT533APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB533A	Samples
SNJ54ABT533FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9584301Q2A SNJ54 ABT533FK	Samples
SNJ54ABT533J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9584301QRA SNJ54ABT533J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT533APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT533APWR	TSSOP	PW	20	2000	367.0	367.0	38.0

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.050 (1,27)

0.045 (1,14) / 0.035 (0,89)

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. Falls within JEDEC MS−004

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DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

A

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ | 0,10 Ⓜ

20   11

△D 4,50 / 4,30   6,60 / 6,20

1   10

6,60 / 6,40

△C

0,15 NOM

Gage Plane

0°−8°   0,25   0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane

◺ | 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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