ANALOG DEVICES

Mixed-Signal Processor with Host Interface Port

ADSP-21msp50A/55A/56A

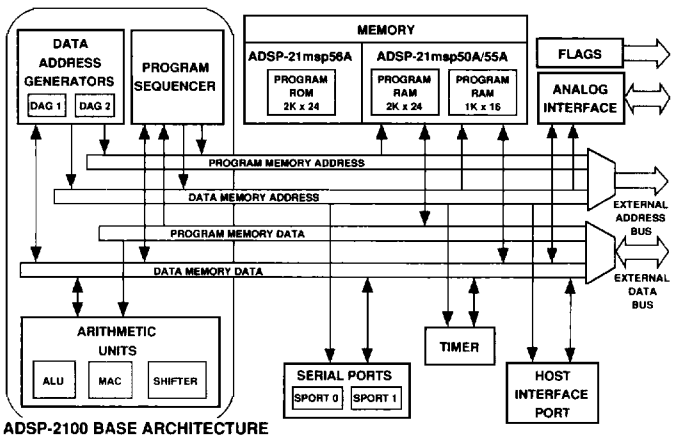
FEATURES

77 ns Instruction Cycle Time from 13.00 MHz Crystal
ADSP-2100 Family Code & Function Compatible
2K Words of On-Chip Program Memory RAM
1K Words of On-Chip Data Memory RAM
2K Words of On-Chip Program Memory ROM (ADSP-21msp56A Only)
8- or 16-Bit Parallel Host Interface Port
Analog Interface Provides
- **16-Bit Sigma-Delta ADC and DAC**
- **Programmable Gain Stages**
- **On-Chip Antialiasing and Anti-Imaging Filters**
- **8 kHz Sampling Frequency**
- **65 dB ADC, SNR and THD**
- **77 dB DAC, SNR and THD**

<1 mW Powerdown Mode with 100 Cycle Recovery
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides:
- **Zero Overhead Looping**
- **Conditional Instruction Execution**

Two Double-Buffered Serial Ports with Companding Hardware, One Serial Port Has Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
100-Lead PQFP and 144-Pin PGA

FUNCTIONAL BLOCK DIAGRAM



ADSP-2100 BASE ARCHITECTURE

The ADSP-21msp5xA combines the ADSP-2100 base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a host interface port, an analog front end, a programmable timer, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-21msp50A and ADSP-21msp55A provide 2K words (24-bit) of program RAM and 1K word (16-bit) of data memory. The ADSP-21msp56A provides an additional 2K words (24-bit) of program ROM. All of the products in the ADSP-21msp5xA family integrate a high performance analog front end based on a single chip, voice band front end, the AD28msp02. Powerdown circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-21msp50A is available in a 144-pin PGA package. The ADSP-21msp55A and ADSP-21msp56A, reduced pin versions, are available in a 100-pin PQFP package.

GENERAL DESCRIPTION

The ADSP-21msp5xA Family of Mixed-Signal Processors (MSProcessors™) are fully integrated, single chip DSPs complete with a high performance analog front end. The ADSP-21msp5x Family is optimized for voice band applications such as Speech Compression, Speech Processing, Speech Recognition, Text-to-Speech, and Speech-to-Text conversion.

MSProcessors is a trademark of Analog Devices, Inc.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

Table I. ADSP-21msp5xA Processor Differences

	Total Pins	V_{CC}	V_{DD}	GND_A	GND	Program Memory	Flags	Powerdown Acknowledge Pin	HIP Width
ADSP-21msp50A	144	1	5	2	7	2K RAM	3	Y	8 or 16 Bits
ADSP-21msp55A	100	1	4	2	5	2K RAM	1	N	8 Bits
ADSP-21msp56A	100	1	4	2	5	2K RAM 2K ROM	1	N	8 Bits

Table I highlights the differences among ADSP-21msp5xA processors.

Fabricated in a high-speed, double poly, double metal. low power, CMOS process, the ADSP-21msp5xA family operates with a 77 ns instruction cycle time. Every instruction executes in a single cycle.

The ADSP-21msp5xA's flexible architecture and comprehensive instruction set allow the processor to perform multiple tasks in parallel. In one cycle the ADSP-21msp5xA can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- perform an analog conversion
- receive and transmit data through the two serial ports
- receive and/or transmit data through the host interface port

In-Circuit Emulation

Analog Devices provides an ADSP-21msp5xA In-Circuit Emulator (ICE) to debug your system. The emulator consists of hardware, host computer resident software, and the emulator probe (the part of the emulator that fits in the ADSP-21msp5xA socket in your system). If you plan to use the emulator, you should consider the following:

- the physical dimensions of the emulator probe (you must leave enough clearance around the ADSP-21msp5xA socket to connect the probe)
- the emulator probe has the same footprint as the 144-pin PGA package; adapter sockets are available to convert the probe to 100-lead PQFP packages
- the emulator's restrictions (differences between emulator and processor operation).

For detailed information about the restrictions, operation, and mechanical specifications of the emulator, see the ADDS-21XX-ICE data sheet, ADSP-21msp50A Emulator release note, and the *ADSP-21msp50A Emulator Manual Addendum* to the *ADSP-2111 Emulator Manual.*

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-21msp5xA. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code, and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM programmer compatible files. The C Compiler generates ADSP-21msp5xA assembly source code.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-21msp5xA. The ADSP-21msp50A EZ-ICE® emulator aids in the hardware debugging of ADSP-21msp5xA systems. The emulator performs a full range of emulation functions including stand-alone operation, single-step or full-speed operation in the target, changing register values, and setting breakpoints. The EZ-LAB® demonstration board is a complete ADSP-21msp5xA system that executes EPROM-based programs.

Additional Information

This data sheet provides a general overview of ADSP-21msp5xA functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual.* For more information about the Development System and ADSP-21msp5xA programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals*, the *ADSP-2111 Emulator Manual*, and the *ADSP-21msp50A Emulator Manual Addendum.*

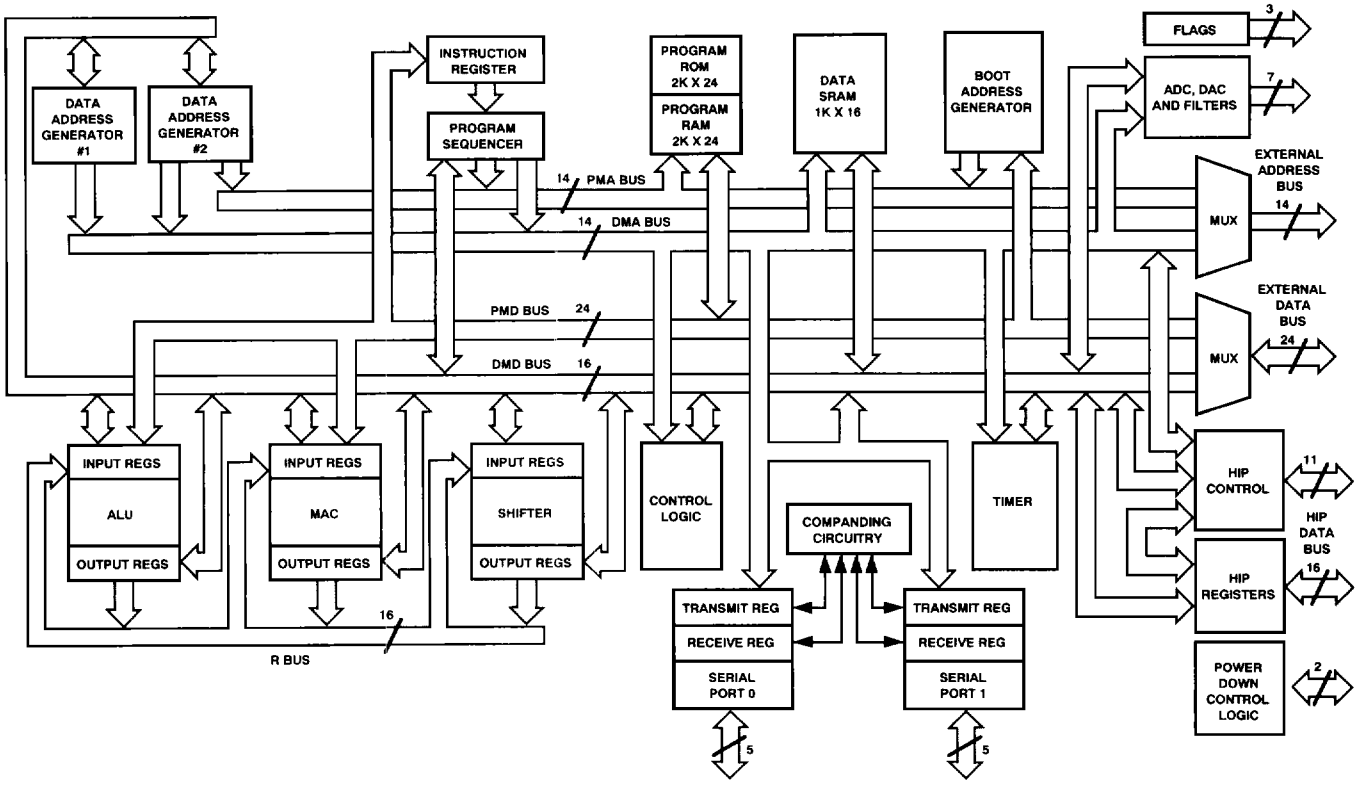


Figure 1. ADSP-21msp5xA Block Diagram

DIGITAL ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-21msp5xA. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21msp5xA executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off chip, and the two data buses (PMD and DMD) share a single external data bus.

Program memory can store both instructions and data, permitting the ADSP-21msp5xA to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-21msp5xA can fetch an operand from on-board program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). Bus grant has two modes of operation. If GoMode is enabled in the MSTAT register, instruction execution continues from internal memory. If GoMode is disabled, the processor stops instruction execution and waits for the deassertion of $\overline{BR}$.

In addition to the address and data bus for external memory connection, the ADSP-21msp5xA has a Host Interface Port (HIP) for easy connection to a host processor. The HIP is made up of 16 data/address pins and 11 control pins (only 8 data/address and 10 control pins on the ADSP-21msp55A/56A). The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000

series, the Intel 80C51 series and the Analog Devices' ADSP-2101 can be easily connected to the HIP. The host processor can boot the ADSP-21msp5xA's on-chip memory through the HIP.

The ADSP-21msp5xA can respond to eleven interrupts. There can be up to three external interrupts, configured as edge or level sensitive, and eight internal interrupts generated by the Timer, the Serial Ports ("SPORTs"), the HIP, the powerdown circuitry, and the analog interface. There is also a master RESET signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 77 ns ADSP-21msp5xA to use an external 250 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware. The on-chip program memory can also be initialized through the HIP.

The ADSP-21msp5xA features three general-purpose flag outputs whose states are controlled through software. (Only one flag output is available on the ADSP-21msp55A/56A.) You can use these outputs to signal an event to an external device. In addition, the data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n-1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-21msp5xA instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-21msp5xA assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-21msp5xA incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-21msp5xA SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORTs receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORT0 can receive and transmit an entire circular buffer of data with only one overhead cycle per data word (Autobuffering Mode). An interrupt is generated after a completed data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be reconfigured for two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-21msp5xA is available in a 100-lead PQFP and a 144-pin PGA package. Table II contains the pin descriptions. Pins marked with an asterisk (*) differ according to the package.

Table II. ADSP-21msp5xA Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Digital Pins			
Address	14	O	Address output for program, data and boot memory spaces
Data	24	I/O	Data I/O pins for program and data memories. Input only for boot memory space, with two MSBs used as boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor reset input
$\overline{\text{IRQ2}}$	1	I	External interrupt request #2
$\overline{\text{BR}}$	1	I	External bus request input
$\overline{\text{BG}}$	1	O	External bus grant output
$\overline{\text{PMS}}$	1	O	External program memory select
$\overline{\text{DMS}}$	1	O	External data memory select
$\overline{\text{BMS}}$	1	O	Boot memory select
$\overline{\text{RD}}$	1	O	External memory read enable
$\overline{\text{WR}}$	1	O	External memory write enable
MMAP	1	I	Memory map select
CLKIN, XTAL	2	I	External clock or quartz crystal input
CLKOUT	1	O	Processor clock output
$\overline{\text{HSEL}}$	1	I	HIP select input
$\overline{\text{HACK}}$	1	O	HIP acknowledge output
HSIZE	*	I	8/16 bit host select input 0 = 16-bit; 1 = 8-bit ADSP-21msp50A only
BMODE	1	I	Boot mode select input 0 = EPROM/data bus; 1 = HIP
HMD0	1	I	Bus strobe select input 0 = RD, WR; 1 = RW, DS

Table II. 21msp5x Pin List (Continued)

Pin Group Name	# of Pins	Input/ Output	Function
HMD1	1	I	HIP address/data mode select input 0 = separate; 1 = multiplexed
$\overline{HRD}/\overline{HRW}$	1	I	HIP read strobe/ read/write select input
$\overline{HWR}/\overline{HDS}$	1	I	HIP write strobe/ host data strobe select input
HD15-0/ HAD15-0	*	I/O	HIP data/data and address Only HD7-0 on ADSP-21msp55A/56A
HA2/ALE	1	I	Host address 2/ Address latch enable input
HA1-0/ unused	2	I	Host addresses 1 and 0 inputs
SPORT0	5	I/O	Serial port 0 I/O pins (TFS0, RFS0, DT0, DR0, SCLK0)
SPORT1	5	I/O	Serial port 1 I/O pins
or			
$\overline{IRQ1}$ (TFS1)	1	I	External interrupt request #1
$\overline{IRQ0}$ (RFS1)	1	I	External interrupt request #0
SCLK1	1	O	Programmable clock output
FO (DT1)	1	O	Flag Output pin
FI (DR1)	1	I	Flag Input pin
FL2-0	*	O	General purpose flag output pins, Only FL0 on ADSP-21msp55A/ 56A
V_{DD}	*		Digital power supply, 4 on 100-lead PQFP, 5 on 144-pin PGA
GND	*		Digital ground, 5 on 100-lead PQFP, 7 on 144-pin PGA
$\overline{PWD}$	1	I	Powerdown pin
PWDACK	*	O	Powerdown acknowledge pin, ADSP-21msp50A only
Analog Pins			
VIN_{NORM}	1	I	Input terminal of the NORM amplifier for the encoder section (ADC)
VIN_{AUX}	1	I	Input terminal of the AUX amplifier for the encoder section (ADC)
DECOUPLE	1	I	Ground reference of the NORM and AUX amplifiers for the encoder section (ADC)
$VOUT_P$	1	O	Noninverting output terminal of the differential amplifier from the decoder section (DAC)
$VOUT_N$	1	O	Inverting output terminal of the differential amplifier from the decoder section (DAC)
V_{REF}	1	O	Output voltage reference
REF_FILTER	1	O	Voltage reference external bypass filter node
V_{CC}	1		Analog power supply, 1 on 100-lead PQFP and 144-pin PGA
GND_A	2		Analog ground, 2 on 100-lead PQFP and 144-pin PGA

Host Interface Port

The ADSP-21msp5xA host interface port is a parallel I/O port that allows for an easy connection to a host processor. Through the HIP, the ADSP-21msp5xA can be used as a memory-mapped peripheral to a host computer. The HIP can be thought of as an area of dual-ported memory, or mailbox registers, that allow communication between the computational core of the ADSP-21msp5x and the host computer.

The HIP is completely asynchronous. The host processor can write data into the HIP while the ADSP-21msp5xA is operating at full speed.

The HIP can be configured with the following pins:

- HSIZE (ADSP-21msp50A only) configures HIP for 8-bit or 16-bit communication with the host processor.
- BMODE determines whether the ADSP-21msp5xA boots from the host processor (through the HIP) or external EPROM (through the data bus).
- HMD0 configures the bus strobes as separate read and write strobes, or a single read/write select and a host data strobe.
- HMD1 selects separate address (3-bit) and data (16-bit) buses, or a multiplexed, 16-bit address/data bus with address latch enable.

Tying these pins to appropriate values configures the ADSP-21msp5x for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

In 8-bit reads, the ADSP-21msp5xA tristates the upper eight bits of the bus. When the host processor writes an 8-bit value to the HIP, the upper eight bits are all zeros. For additional information refer to the *ADSP-2100 Family User's Manual*, Chapter 7, Host Interface Port.

HIP Operation

The HIP contains six data registers (HDR5–0) and two status registers (HSR7–6) with an associated HMASK register for masking interrupts from individual HIP data registers. All HIP data registers are memory-mapped into the internal data memory of the ADSP-21msp5xA. HIP transfers can be managed using either interrupts or a polling scheme. These registers are shown in the section "ADSP-21msp5xA Registers."

The HIP allows a software reset to be performed by the host processor. The internal software reset signal is asserted for five ADSP-21msp5xA cycles.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-21msp5xA provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, and the flags. The ADSP-21msp5xA also supports internal interrupts from the timer, the host interface port, the two serial ports, the analog interface, and the powerdown control circuit. The interrupt levels are internally prioritized and individually maskable (except powerdown and reset). The input pins can be programmed to be either level- or edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table III, and the interrupt registers are shown in Figure 2.

Table III. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)	
Reset (or Power-Up with PUCR = 1)	0000	*(highest priority)*
Powerdown (Nonmaskable)	002C	
$\overline{IRQ2}$	0004	
HIP Write	0008	
HIP Read	000C	
SPORT0 Transmit	0010	
SPORT0 Receive	0014	
Analog Interface Transmit	0018	
Analog Interface Receive	001C	
SPORT1 Transmit or $\overline{IRQ1}$	0020	
SPORT1 Receive or $\overline{IRQ0}$	0024	
Timer	0028	*(lowest priority)*

Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The powerdown interrupt is nonmaskable.

The interrupt control register, ICNTL, allows the external interrupts to be either edge- or level-sensitive. Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially.

The IFC register is a write-only register used to force an interrupt or clear a pending edge-sensitive interrupt.

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt nesting.

System Interface

Figure 3 shows a basic system configuration with the ADSP-21msp5x, two serial devices, a host processor, a boot EPROM, optional external program and data memories, and an analog interface. Up to 15K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories. The ADSP-21msp5xA also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

The ADSP-21msp5xA can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated at any frequency other than the one specified. Operating the ADSP-21msp5xA at any other frequency changes the analog performance, which is not tested or supported.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

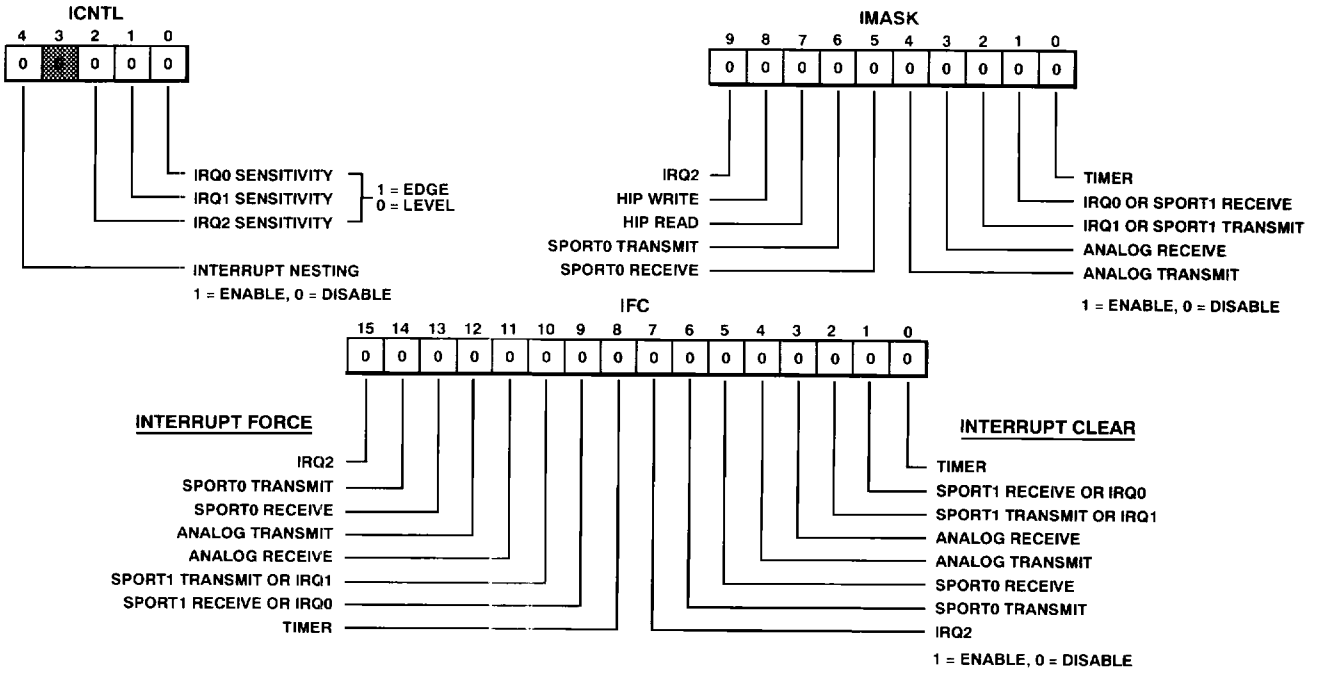


Figure 2. Interrupt Registers

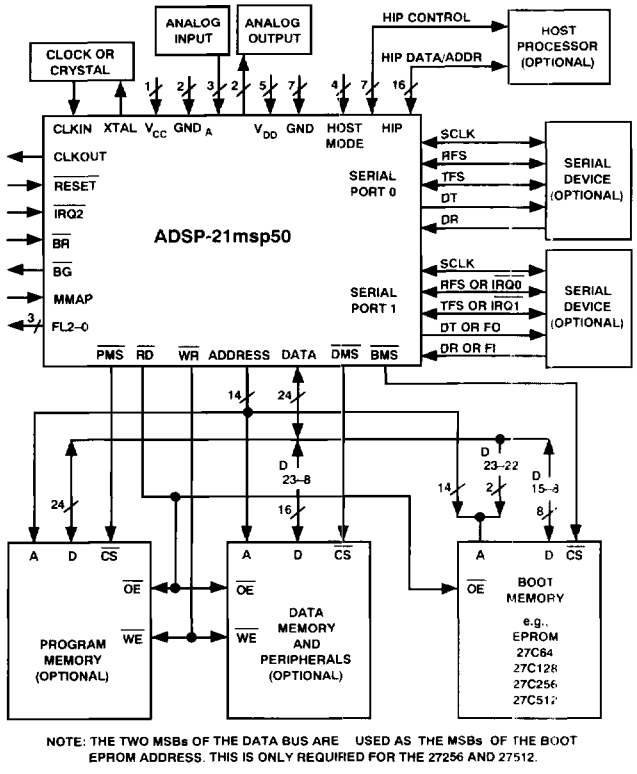


Figure 3. ADSP-21msp5xA Basic System Configuration

Because the ADSP-21msp5xA includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

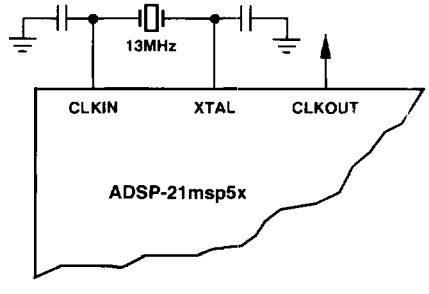


Figure 4. External Crystal Connections

A clock output (CLKOUT) signal is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-21msp5xA. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000 and execution begins.

Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words. 4K words of memory for the ADSP-21msp5xA with optional 2K words ROM and 2K words of RAM memory for non-ROM versions are on chip.

The program memory data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe.

The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal. An external program memory access should always be qualified with the $\overline{\text{PMS}}$ signal.

The ADSP-21msp5xA writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

ADSP-21msp50A/55A

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the two configurations. When MMAP = 0, internal RAM occupies 2K words beginning at address 0x0000; external program memory uses the remaining 14K words beginning at address 0x0800. In this configuration, the boot loading sequence (described in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of external program memory begin at address 0x0000 and internal RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, the boot loading sequence does not take place; execution begins immediately after RESET.

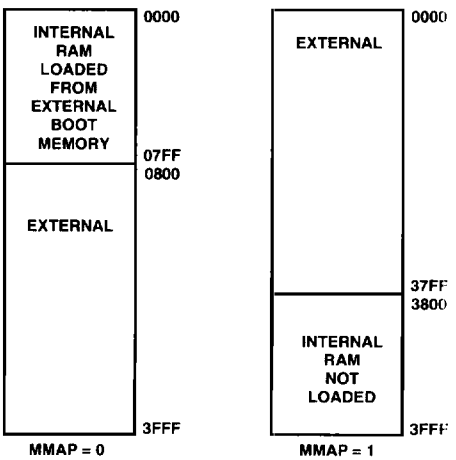


Figure 5. ADSP-21msp50A/55A Program Memory Maps

ADSP-21msp56A

The ADSP-21msp56A is functionally identical to the ADSP-21msp50A/55A. The ADSP-21msp56A includes an additional 2K by 24-bit mask programmable ROM (see Figure 6). The ROM can be used to hold program instructions or data and can be accessed twice in one instruction cycle if necessary. The ROM always resides at locations PM[0x0800] through PM[0x1000] regardless of the state of the MMAP pin. The ROM is enabled by setting the ROMENABLE bit in the Data Memory Wait State control register, DM[0x3FFE]. When the ROMENABLE bit is set to 1, addressing program memory in this range will access the on-chip ROM. When set to zero, addressing program memory in this range will access external program memory. The ROMENABLE bit is set to 0 on chip reset.

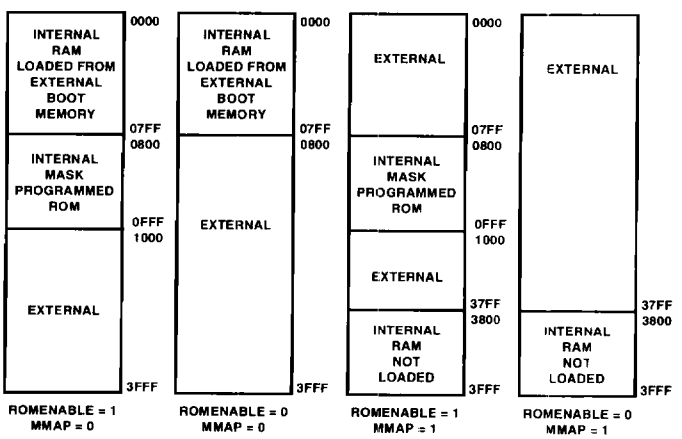


Figure 6. ADSP-21msp56A Program Memory Maps

The program memory interface can generate 0 to 7 wait states for external memory devices; default is 7 wait states after $\overline{\text{RESET}}$.

Data Memory Interface

The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{\text{DMS}}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21msp5xA supports memory-mapped I/O, with the peripherals memory mapped into the data or program memory address spaces and accessed by the processor in the same manner.

Data Memory Map

The on-chip data memory RAM resides in the 1K words of data memory beginning at address 0x3800, as shown in Figure 7. In addition, data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration, host interface port, codec, and serial port operations are located in this region of memory.

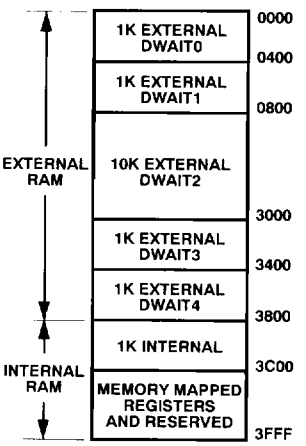


Figure 7. ADSP-21msp5xA Data Memory Map

The remaining 14K of data memory is external. External data memory is divided into five zones, each associated with its own wait state generator. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{\text{RESET}}$.

Boot Memory Interface

The ADSP-21msp5xA can load on-chip memory from external boot memory space. The boot memory space consists of 64K by 8-bit space, divided into eight separate 8K by 8-bit pages. Three bits in the system control register select which page is loaded by the boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{\text{RESET}}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 3 wait states after $\overline{\text{RESET}}$. This allows the ADSP-21msp5x to boot from a single low cost EPROM such as a 27256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{\text{BMS}}$ and $\overline{\text{RD}}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate addressing up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

The ADSP-2100 Family Assembler and Linker support the creation of programs and data structures requiring multiple boot pages during execution.

$\overline{\text{RD}}$ and $\overline{\text{WR}}$ must always be qualified by $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, or $\overline{\text{BMS}}$ to ensure the correct program, data, or boot memory accessing.

HIP Booting

The ADSP-21msp5xA can also boot programs through its Host Interface Port. If BMODE = 1, the ADSP-21msp5xA boots from the HIP. If BMODE = 0, the ADSP-21msp5xA boots through the data bus (in the same way as the ADSP-2101), as described above in "Boot Memory Interface." For additional information about HIP booting, refer to the *ADSP-2100 Family User's Manual*, Chapter 7, "Host Interface Port."

The ADSP-2100 Family Development Software includes a utility program called the HIP Splitter. This utility allows the creation of programs that can be booted via the ADSP-21msp5xA's HIP, in a similar fashion as EPROM-bootable programs generated by the PROM Splitter utility.

Bus Request and Bus Grant

The ADSP-21msp5xA can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{\text{BR}}$) signal. If the ADSP-21msp5xA is not performing an external memory access, then it responds to the active $\overline{\text{BR}}$ input in the following cycle by

- tristating the data and address buses and the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
- asserting the bus grant ($\overline{\text{BG}}$) signal, and
- halting program execution.

If the Go mode is enabled, the ADSP-21msp5xA will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21msp5xA is performing an external memory access when the external device asserts the $\overline{\text{BR}}$ signal, then it will not tristate the memory interfaces or assert the $\overline{\text{BG}}$ signal until the cycle after the access completes, which can be up to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{\text{BR}}$ signal is released, the processor releases the $\overline{\text{BG}}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{\text{RESET}}$ is active.

ANALOG INTERFACE

The analog interface contains encoding circuitry (ADC), decoding circuitry (DAC), and processor interface logic. A block diagram of the ADSP-21msp5xA analog section is shown in Figure 8.

The analog interface is configured through the Analog Control Register and the Analog Autobuffer/Powerdown Register (refer to "ADSP-21msp5xA Registers"). The Analog Control Register DM[0x3FEE] configures the programmable gain stages, the analog input multiplexer and the analog interface powerdown state. Note that unused bits in this register must be cleared to zero.

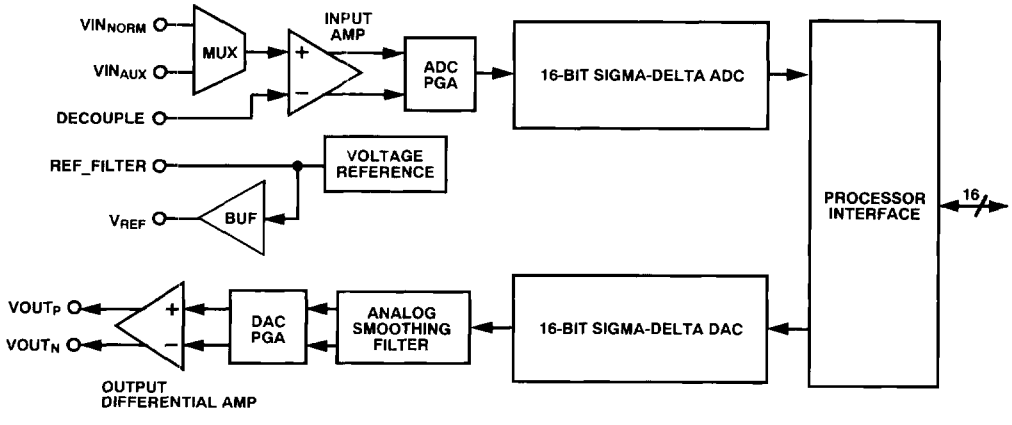


Figure 8. Analog Interface Block Diagram

A/D Conversion

The A/D conversion circuitry of the ADSP-21msp5xA consists of an analog multiplexer, an input amplifier, a programmable gain amplifier (ADC PGA), and a 16-bit sigma-delta ADC.

Analog Input Amplifiers and Multiplexer

The analog multiplexer selects either the NORM or AUX channel as the input to the ADC's sigma-delta modulator. The analog inputs should be ac coupled.

The ADC PGA may be used to additionally increase the signal level by +6 dB, +20 dB, or +26 dB. This gain is selected by Bit 9 and Bit 0 (IG0, IG1) of the analog control register. Input signal level to the sigma-delta ADC should not exceed the V_{INMAX} specification.

ADC

The analog interface's ADC consists of a 2nd-order analog sigma-delta modulator, an antialiasing decimation filter, and an optional digital high-pass filter. For a detailed description of the ADC components, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

D/A Conversion

The D/A conversion circuitry of the ADSP-21msp5xA's analog interface consists of a sigma-delta digital-to-analog converter (DAC), an analog smoothing filter, a programmable gain amplifier (DAC PGA), and a differential output amplifier.

DAC

The DAC consists of an optional digital high-pass filter, an anti-imaging interpolation filter, and a digital sigma-delta modulator. The digital filters and sigma-delta modulator have the same characteristics as the filters and modulator of the ADC. For a detailed description of the DAC components, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

Analog Smoothing Filter & Programmable Gain Amplifier

The analog smoothing filter consists of a 2nd-order Sallen-Key continuous-time filter and a 3rd-order switched capacitor filter. The Sallen-Key filter has a 3 dB point at approximately 80 kHz.

The DAC's programmable gain amplifier (DAC PGA) can be used to adjust the output signal level by −15 dB to +6 dB in 3 dB increments. This gain is selected by Bits 2–4 (OG0, OG1, OG2) of the of the analog control register.

Differential Output Amplifier

The ADSP-21msp5xA's analog output signal ($VOUT_P$–$VOUT_N$) is produced by a differential amplifier. The differential amplifier meets specifications for loads greater than 2 kΩ, it can drive loads as small as 50 Ω with degraded performance, and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The output signal is dc-biased to the ADSP-21msp5xA's on-chip voltage reference (V_{REF}) and can be ac coupled directly to a load or dc-coupled to an external amplifier.

The $VOUT_P$–$VOUT_N$ outputs must be used as a differential signal; do not use either pin as a single-ended output.

OPERATING THE ANALOG INTERFACE

The analog interface of the ADSP-21msp5xA is operated with several memory-mapped control and data registers. The ADC and DAC I/O data is received and transmitted through two memory-mapped data registers. The data can also be autobuffered directly into (or from) on-chip memory. In both cases, the I/O processing is interrupt-driven: two ADSP-21msp5xA interrupts are dedicated to the analog interface, one for ADC receive data and one for DAC transmit data.

The ADSP-21msp5xA must have an input clock frequency of 13 MHz. At this frequency, analog-to-digital and digital-to-analog converted data is transmitted at an 8 kHz rate with a single 16-bit word transmitted every 125 μs.

For detailed information about the Analog Interface, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

Autobuffering

In some applications it is advantageous to perform block data transfers between the analog converters and processor memory. Analog interface autobuffering enables the automatic transfer of data blocks directly from the ADC to on-chip processor data memory or from on-chip processor data memory to the DAC.

ADC & DAC Interrupts

The analog interface generates two interrupts that signal either: 1) that a 16-bit, 8 kHz analog-to-digital or digital-to-analog conversion has been completed, or 2) that an autobuffer block transfer has been completed (i.e. the data buffer contents have been received or transmitted).

When an analog interrupts occurs, the processor vectors to the addresses listed in *Table III, Interrupt Priority and Interrupt Vector Address*.

The ADC receive and DAC transmit interrupts occur at an 8 kHz rate, indicating when the data registers should be accessed. On the receive side, the ADC interrupt is generated each time an A/D conversion cycle is completed and the 16-bit data word is available in the ADC receive register. On the transmit side, the DAC interrupt is generated each time a D/A conversion cycle is completed and the DAC transmit register is ready for the next 16-bit data word.

Both interrupts are generated simultaneously at an 8 kHz rate, occurring every 1625 instruction cycles with a 13.00 MHz processor clock. The interrupts are generated continuously, starting when the analog interface is powered up by setting the APWD bits (Bits 5, 6) to ones in the analog control register. Because both interrupts occur simultaneously, only one should be enabled (in IMASK) to vector to a single service routine which handles both transmit and receive data. However, when using autobuffer transfers, both interrupts should be enabled.

POWERDOWN

The ADSP-21msp5xA processors contain a low power feature that allows the processor to enter a very low power dormant state through hardware or software control. Here is a brief list of powerdown features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9, "System Interface" for detailed information about the powerdown features.

- Powerdown mode holds the processor in CMOS standby with a maximum current of less than 100 µA in some modes.
- Quick recovery from powerdown. In some modes, the processor can begin executing instructions in less than 100 cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during powerdown without affecting the lowest power rating and 100 cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 cycle startup.
- Powerdown is initiated by either the powerdown pin ($\overline{PWD}$) or the software powerdown force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering-down. The powerdown interrupt also can be used as a nonmaskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the powerdown state.
- The $\overline{RESET}$ pin also can be used to terminate powerdown, and the host software reset feature can be used to terminate powerdown under certain conditions.
- Powerdown acknowledge pin (on ADSP-21msp50A only) indicates when the processor has entered powerdown.

Idle

When the ADSP-21msp5xA is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction.

Slow Idle

The IDLE instruction is enhanced on the ADSP-21msp5xA to slow the processor's internal clock, which further reduces power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction. The format of the instruction is

IDLE(n);

where: n = 16, 32, 64, or 128.

The instruction keeps the processor fully functional, operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK and timer clock, are reduced by the same ratio. CLKOUT remains at normal rate; it is not reduced. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE(n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts—the 1-cycle response time of the standard idle state—is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-21msp5xA remains in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE(n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processors cycles).

ADSP-21msp5xA Registers

Figure 9 summarizes all the registers in the ADSP-21msp5xA. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

A secondary set of registers in all computational units allows a single-cycle context switch.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT register, timer registers, HIP control registers, HIP data registers, and SPORT control registers are all mapped into data memory; that is, you access these registers by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

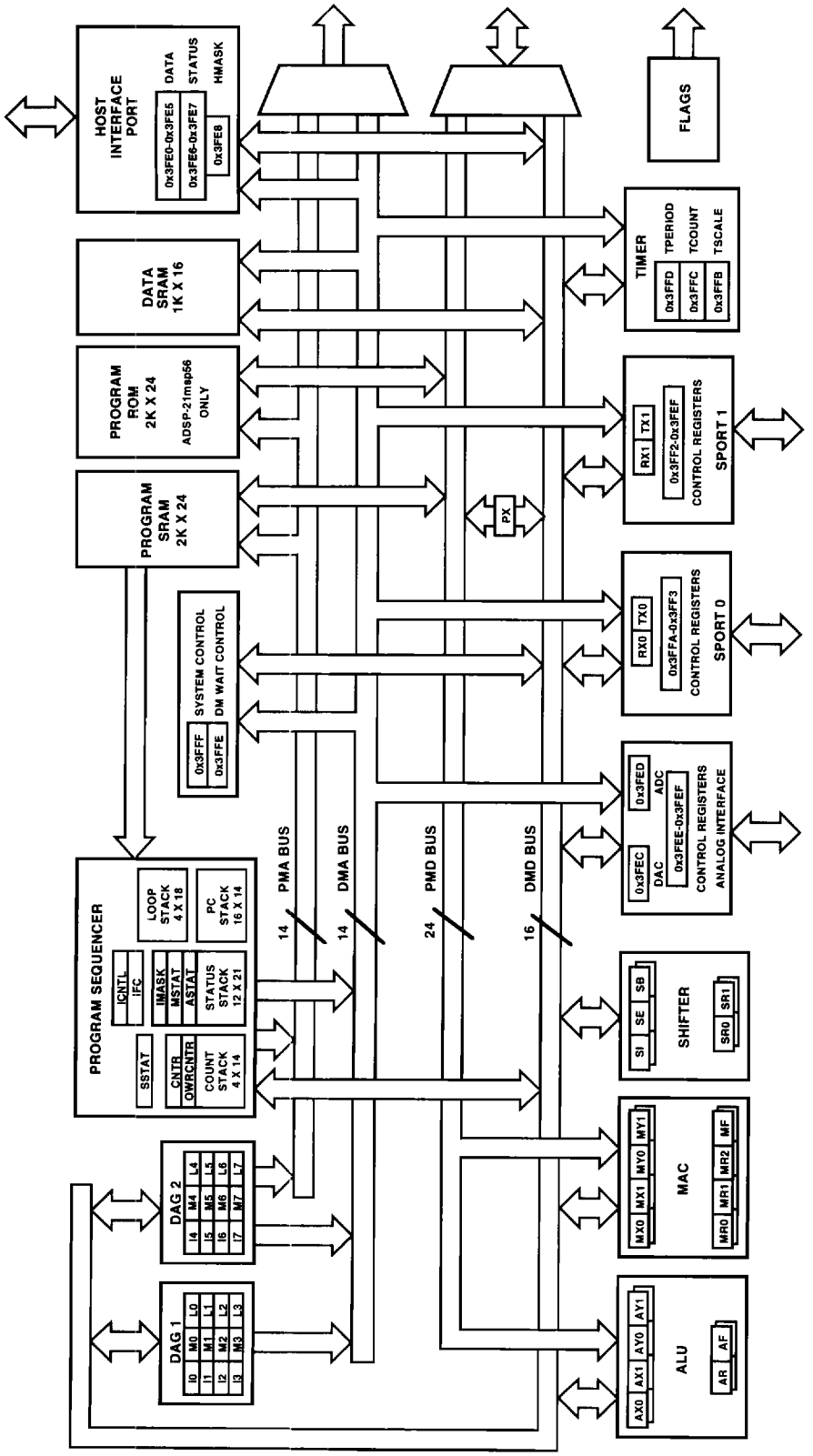
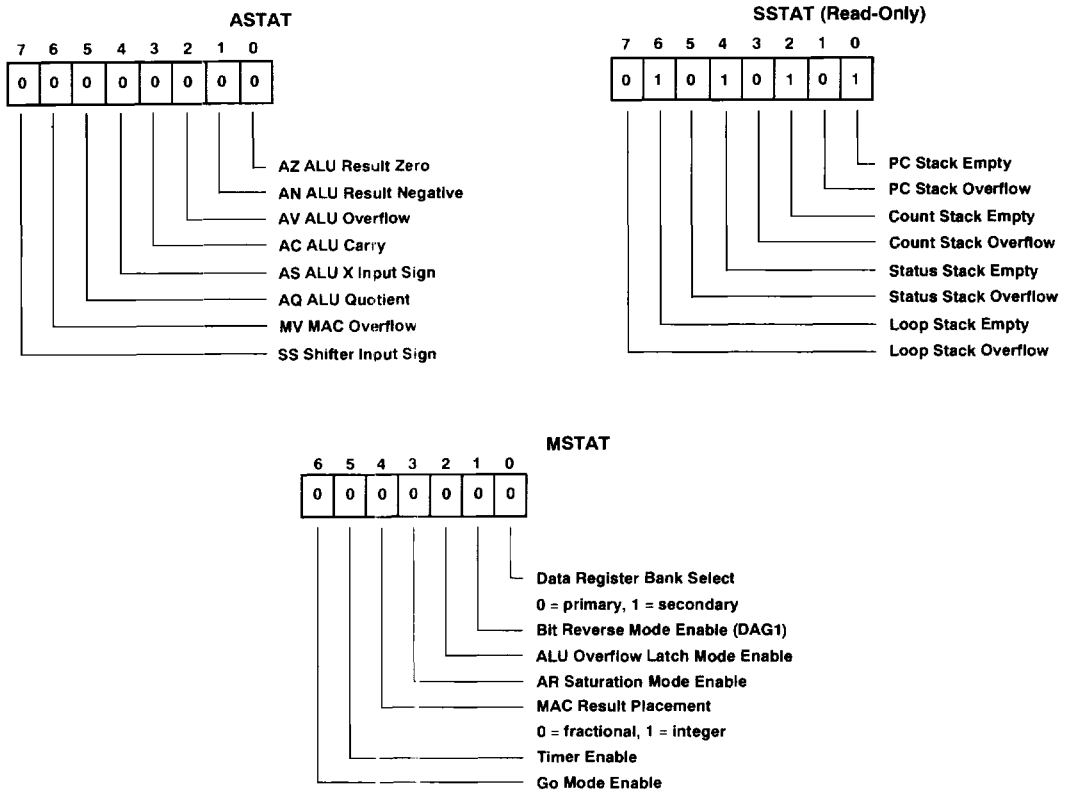
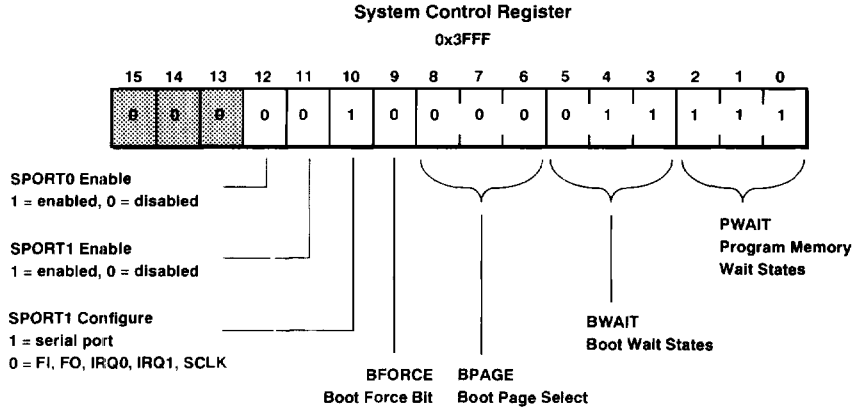
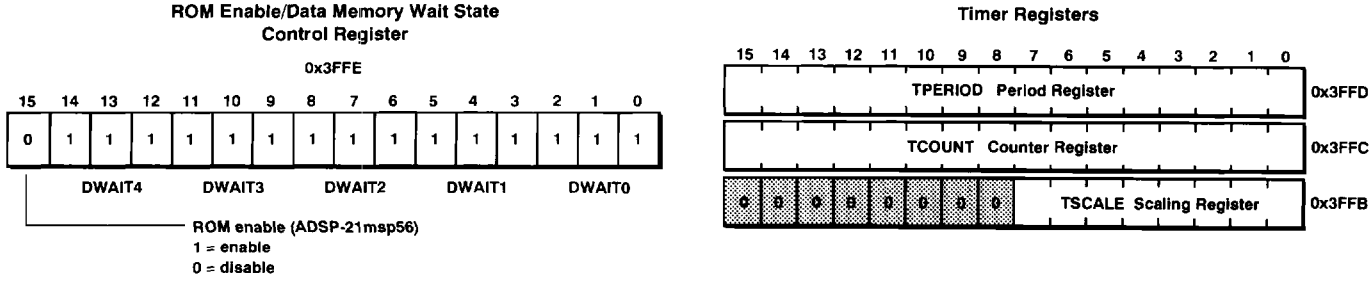


Figure 9. ADSP-21msp5xA Registers







Control Registers

SPORT0 Multichannel Receive Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FFA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0x3FF9

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Multichannel Transmit Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FF8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0x3FF7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Control Register

0x3FF6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Multichannel Enable MCE
- Internal Serial Clock Generation ISCLK
- Receive Frame Sync Required RFSR
- Receive Frame Sync Width RFSW
- Multichannel Frame Delay MFD
  Only If Multichannel Mode Enabled
- Transmit Frame Sync Required TFSR
- Transmit Frame Sync Width TFSW
- ITFS Internal Transmit Frame Sync Enable
  (or MCL Multichannel Length; 1 = 32 words, 0 = 24 words
  Only If Multichannel Mode Enabled)
- SLEN Serial Word Length
- DTYPE Data Format
  00 = right justify, zero-fill unused MSBs
  01 = right justify, sign extend into unused MSBs
  10 = compand using μ-law
  11 = compand using A-law
- INVRFS Invert Receive Frame Sync
- INVTFS Invert Transmit Frame Sync
  (or INVTDV Invert Transmit Data Valid
  Only If Multichannel Mode Enabled)
- IRFS Internal Receive Frame Sync Enable

SPORT0 SCLKDIV
Serial Clock Divide Modulus

0x3FF5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 RFSDIV
Receive Frame Sync Divide Modulus

0x3FF4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Autobuffer Control Register

0x3FF3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0											0	0

TIREG TMREG RIREG RMREG

- TBUF Transmit Autobuffering Enable
- RBUF Receive Autobuffering Enable

SPORT1 Control Register

0x3FF2

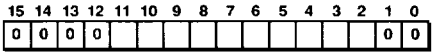
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Flag Out (Read Only)
- Internal Serial Clock Generation ISCLK
- Receive Frame Sync Required RFSR
- Receive Frame Sync Width RFSW
- Transmit Frame Sync Required TFSR
- Transmit Frame Sync Width TFSW
- ITFS Internal Transmit Frame Sync Enable
- SLEN Serial Word Length
- DTYPE Data Format
  00 = right justify, zero-fill unused MSBs
  01 = right justify, sign extend into unused MSBs
  10 = compand using μ-law
  11 = compand using A-law
- INVRFS Invert Receive Frame Sync
- INVTFS Invert Transmit Frame Sync
- IRFS Internal Receive Frame Sync Enable

Control Registers

Analog Autobuffer/Powerdown Control Register

0x3FEF



XTALDIS
XTAL pin disable during powerdown
1 = disabled, 0 = enabled
(disable XTAL pin when no external crystal connected)

XTALDELAY
Delay startup from powerdown 4096 cycles
1 = delay, 0 = no delay

PDFORCE
Powerdown force

PUCR
Exit from powerdown context
1 = soft reset, 0 = resume execution

ARBUF
ADC Receive Autobuffer Enable

ATBUF
DAC Transmit Autobuffer Enable

ARMREG
Receive M register

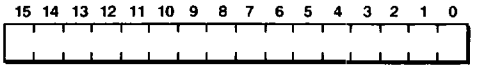
ARIREG
Receive I register

ATMREG
Transmit M register

ATIREG
Transmit I register

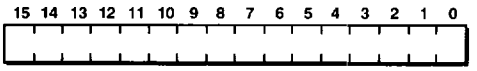
SPORT1 SCLKDIV
Serial Clock Divide Modulus

0x3FF1



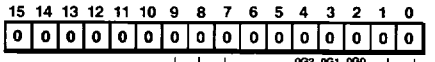
SPORT1 RFSDIV
Receive Frame Sync Divide Modulus

0x3FF0



Analog Control Register

0x3FEE



IG0
ADC Input Gain

DABY
DAC High Pass Filter Bypass
1 = bypass, 0 = insert

ADBY
ADC High Pass Filter Bypass
1 = bypass, 0 = insert

APWD
Analog Interface Powerdown
0 = powerdown, 1 = enable
(set both bits to 1 to enable interface)

IG1
ADC Input Gain

IMS
ADC Input Multiplexer Select
1 = AUX input, 0 = NORM input

0G2, 0G1, 0G0
DAC Output Gain (for PGA)

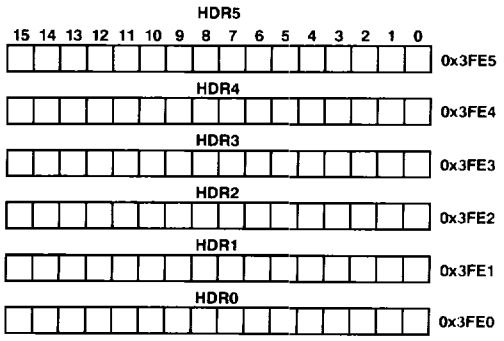
Gain	0G2	0G1	0G0
+6dB	0	0	0
+3dB	0	0	1
0dB	0	1	0
–3dB	0	1	1
–6dB	1	0	0
–9dB	1	0	1
–12dB	1	1	0
–15dB	1	1	1

IG1,IG0
ADC Input Gain (for PGA)

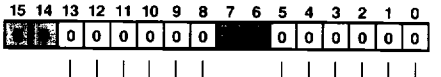
Gain	IG1	IG0
0dB	0	0
+6dB	0	1
+20dB	1	0
+26dB	1	1

All bits are set to 0 at processor reset.
(Reserved bits 10-15 must always be set to 0)

HIP Data Registers



HMASK Register

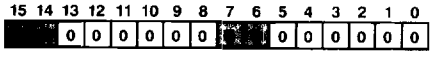


HOST HDR5 READ
HOST HDR4 READ
HOST HDR3 READ
HOST HDR2 READ
HOST HDR1 READ
HOST HDR0 READ

HOST HDR0 WRITE
HOST HDR1 WRITE
HOST HDR2 WRITE
HOST HDR3 WRITE
HOST HDR4 WRITE
HOST HDR5 WRITE

INTERRUPT ENABLES
1 = enable
0 = disable

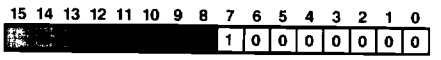
HSR6 Register



21msp5x HDR5 WRITE
21msp5x HDR4 WRITE
21msp5x HDR3 WRITE
21msp5x HDR2 WRITE
21msp5x HDR1 WRITE
21msp5x HDR0 WRITE

HOST HDR0 WRITE
HOST HDR1 WRITE
HOST HDR2 WRITE
HOST HDR3 WRITE
HOST HDR4 WRITE
HOST HDR5 WRITE

HSR7 Register



OVERWRITE MODE

SOFTWARE RESET

21msp5x HDR0 WRITE
21msp5x HDR1 WRITE
21msp5x HDR2 WRITE
21msp5x HDR3 WRITE
21msp5x HDR4 WRITE
21msp5x HDR5 WRITE

Control Registers

INSTRUCTION SET DESCRIPTION

The ADSP-21msp5xA assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize internal memory and conform to the ADSP-21msp5x's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
  MF=MX0*MY1 (RND), MX0=DM (I2,M1); {MF= error*beta}
  MR=MX0*MF (RND), AY0=PM (I6,MS);
  DO adapt UNTIL CE;
        AR=MR1 + AY0, MX0=DM (I2,M1), AY0=PM (I6,M7);
adapt:  PM(I6,M6) =AR, MR=MX0*MF (RND);
  MODIFY (I2, M3);                {Point to oldest data}
  MODIFY (I6, M7);                {Point to start of data}
```

CIRCUIT DESIGN CONSIDERATIONS

The following sections discuss interfacing analog signals to the ADSP-21msp5xA.

Analog Signal Input

Figure 10 shows the recommended input circuit for the ADSP-21msp5xA's analog input pin (either VIN_{NORM} or VIN_{AUX}). The circuit of Figure 10 implements a first-order low-pass filter (R_1C_1) with a 3 dB point less than 20 kHz. This is the only filter required external to the processor to prevent aliasing of the sampled signal. Since the ADSP-21msp5xA's sigma-delta ADC uses a highly oversampled approach that transfers the bulk of the antialiasing filtering into the digital domain, the off-chip antialiasing need only be of low order.

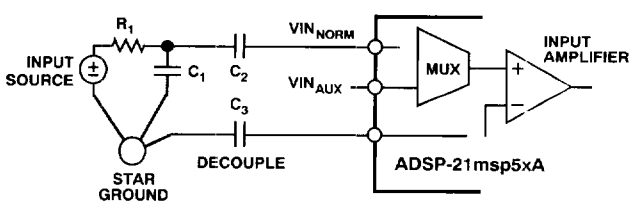


Figure 10. Recommended Analog Input Circuit

The ADSP-21msp5xA's on-chip ADC PGA can be used when there is not enough gain in the input circuit. The PGA gain is set by Bits 9 and 0 (IG1, IG0) of the processor's analog control register. The gain must be chosen to ensure that a full-scale input signal (at R1 in Figure 10) produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed V_{INMAX} (refer to the "Analog Interface Electrical Characteristics" specifications).

VIN_{NORM} and VIN_{AUX} are biased at the Internal Reference Voltage (nominal of 2.5 V) of the msp5xA, which lets the analog section of the msp5xA operate from a single supply. The input signal to the msp5xA should be ac coupled with an external capacitor (C_2). The value of C_2 is determined by the input resistance of the msp5xA (125 kΩ) and the desired cutoff frequency. The cutoff frequency should be ≤30 Hz. The following equations should be used to determine the values for R_1, C_1, C_2; R_1 should be less than or equal to 200 Ω. C_2 should be ≥0.047 μf; C_3 should be equal to C_2.

$$C_2 = \frac{1}{2\,\pi\, f_1\, R_{IN}}$$

R_{IN} = MSP5x input resistance (125 kΩ)
f_1 = cutoff frequency <30 Hz

$$R_1 = \frac{1}{2\,\pi\, f_2\, C_1}$$

$R_1 \leq 200\ \Omega$
f_2 >8 kHz <20 kHz

$$C_1 = \frac{1}{2\,\pi\, f_2\, R_1}$$

Analog Signal Output

The ADSP-21msp5xA's differential analog output ($VOUT_P$–$VOUT_N$) is produced by an on-chip differential amplifier which is part of the processor's analog interface. The differential amplifier meets specifications for loads greater than 2 kΩ, it can drive loads as small as 50 Ω with degraded performance, and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The differential output can be ac coupled directly to a load or dc-coupled to an external amplifier.

Figure 11 shows a simple circuit providing a differential output with ac coupling. The capacitor of this circuit (C_{OUT}) is optional; if used, its value can be chosen as follows:

$$C_{OUT} = \frac{1}{(60\,\pi)\, R_L}$$

The $VOUT_P$, $VOUT_N$ outputs must be used as differential outputs; do not use either as a single-ended output. Figure 12 shows an example circuit which can be used to convert the differential output to a single-ended output. The circuit uses a differential-to-single-ended amplifier, the Analog Devices SSM2141.

Voltage Reference Filter Capacitance

Figure 13 shows the recommended reference filter capacitor connections. The capacitor grounds should be connected to the same star ground point shown in Figure 10.

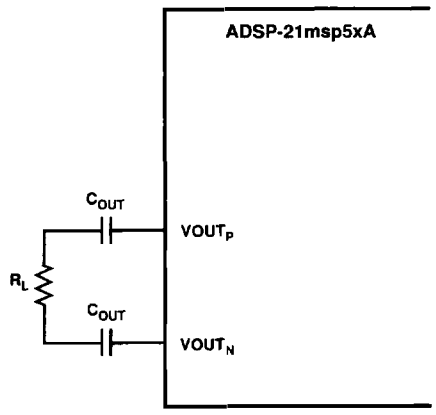


Figure 11. Example Circuit for Differential Output with AC Coupling

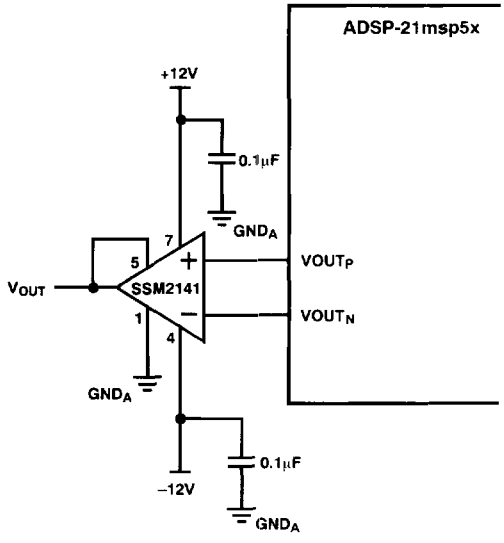


Figure 12. Example Circuit for Single-Ended Output

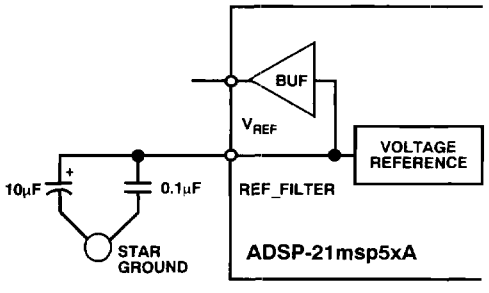


Figure 13. Voltage Reference Filter Capacitor

APPLICATION EXAMPLES

The ADSP-21msp5xA is ideal for speech processing applications where high performance for analog and digital circuitry is required, but board space is severely limited. The cellular radio handset is one application. Here, the ADSP-21msp5xA can digitize the speech, then perform compression algorithms that sufficiently reduce the bit rate for transmission in a limited radio bandwidth.

DEFINITION OF SPECIFICATIONS

Absolute Gain

Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured with a 1.0 kHz sine wave at 0 dBm0. The absolute gain specification is used as a reference for gain tracking error specification.

Gain Tracking Error

Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 1 kHz at 0 dBm0 (equal to absolute gain). Gain tracking error at 0 dBm0 is 0 dB by definition.

SNR + THD

Signal-to-noise ratio plus total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300–3400 Hz, including harmonics but excluding dc.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For final testing, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

Idle Channel Noise

Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300–3400 Hz).

Crosstalk

Crosstalk is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of the same signal which couples onto the adjacent channel. Crosstalk is expressed in dB.

Power Supply Rejection

Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Group Delay

Group delay is defined as the derivative of radian phase with respect to radian frequency, $\partial\phi(\omega)/\partial\omega$. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay away from a constant indicates the degree of nonlinear phase response of the system.

ADSP-21msp50A/55A/56A—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	°C

Refer to Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = −0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = −100 μA[10]	V_{DD} − 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	μA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	μA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	μA
I_{DD}	Digital Supply Current (Idle)[8, 9]	Codec Inactive		16	mA
I_{DD}	Digital Supply Current (Dynamic)[9]	Processor 80% Loaded, Codec Active[11]		90	mA
I_{DD}	Digital Supply Current (Powerdown)[9]	See ADSP-2100 Family User's Manual, Chapter 9		100	μA
I_{CC}	Analog Supply Current (Dynamic)[9]	Codec Active		28	mA
C_I	Input Pin Capacitance[1, 10, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 10, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES

[1]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1–0.

[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, DT0, DT1, CLKOUT, $\overline{\text{HACK}}$, FL2–0.

[3]Bidirectional pins: D0–D23, RFS0, $\overline{\text{RFS1}}$, SCLK0, SCLK1, TFS0, TFS1 HD0–HD15/HAD0–HAD15.

[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$. DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, HD0–HD15/HAD0–HAD15.

[5]$\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 input pins.

[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).

[7]Although specified for TTL outputs, all ADSP-21msp5xA outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc loads.

[8]Idle refers to ADSP-21msp5xA state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND. Refer to chart in back for lower IDLE currents.

[9]Current reflects device operating with no output loads.

[10]Guaranteed but not tested.

[11]V_{CC} = V_{DD} = max, t_{CK} = 77 ns, ambient temperature = +85°C, 80% execution type 1 instructions, with random data. Refer to section titled "Power Dissipation" for typical figures for digital and analog supply currents.

[12]Applies to PGA and PQFP package types.

[13]Output pin capacitance is the capacitive load for any tristated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} +0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range (Ambient) . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-21msp5xA is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-21msp5xA features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-21msp5xA has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-21msp5xA timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	Address Setup to Write End
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

FREQUENCY RESPONSE

Freq (Hz)	ADC Max (dB)	ADC Min (dB)	DAC Max (dB)	DAC Min (dB)
0+	−60.00	N/A	−60.00	N/A
95	−25.00	N/A	−25.00	N/A
150	+0.266	−0.134	+0.015	−0.185
300	+0.272	−0.128	+0.03	−0.17
1000	+0.00	+0.00	+0.00	+0.00
2000	+0.05	−0.35	+0.00	−0.20
3000	−0.20	−0.60	−0.10	−0.30
3400	−0.30	−0.70	−0.14	−0.34
3700	−0.375	−0.775	−0.17	−0.37
3850	−25.00	N/A	−25.00	N/A
4000	−60.00	N/A	−60.00	N/A

NOTES
All specs relative to absolute gain @ 1.0 kHz
Both ADC and DAC high-pass filters *inserted*.
ADC specs *include* input RC filter attenuation (see Analog Test Conditions for RC filter details).

NOISE AND DISTORTION

Parameter	Min	Max	Unit	Test Conditions
ADC Intermodulation Distortion		−55	dB	m, n = 1 and 2; f_a = 984; f_b = 1047
DAC Intermodulation Distortion		−70	dB	m, n = 1 and 2; f_a = 984; f_b = 1047
ADC Idle Channel Noise		65	dBm0	
DAC Idle Channel Noise		72	dBm0	
ADC Crosstalk (DAC to ADC)		−65	dB	DAC signal level: 1.0 kHz, 0 dBm0 ADC at idle
DAC Crosstalk (ADC to DAC)		−65	dB	DAC idle ADC signal level: 1.0 kHz, 0 dBm0
ADC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
DAC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
ADC Group Delay[1]		1	ms	300–3000 Hz
DAC Group Delay[1]		1	ms	300–3000 Hz
ADC SNR + THD		65	dB	1.0 kHz; 0 dBm0
DAC SNR + THD		77	dB	1.0 kHz, 0 dBm0

[1]Guaranteed but not tested.

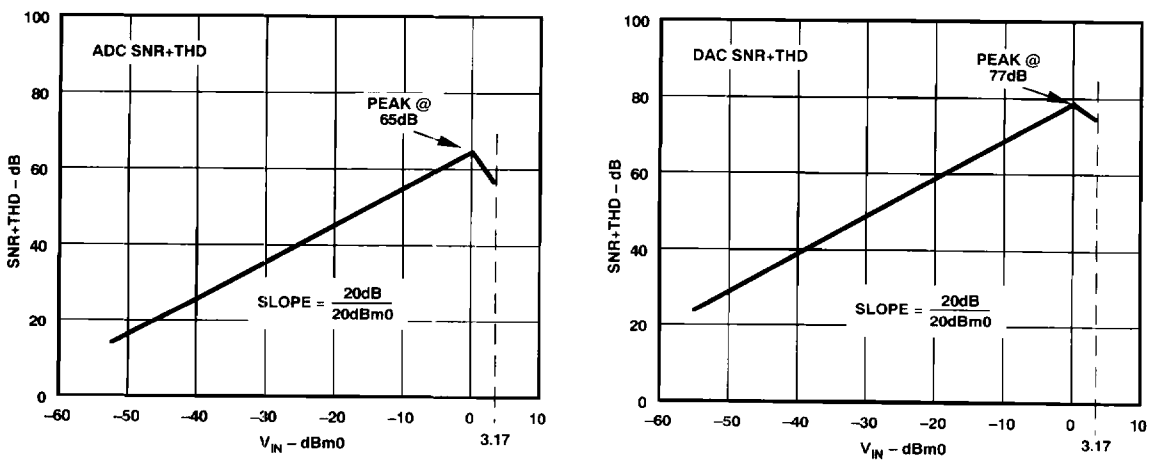


Figure 14. SNR + THD vs. V_{IN}

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ADC:					
R_I	Input Resistance[4] at VIN_{NORM}, VIN_{AUX}		125		kΩ
VIN_{MAX}	Maximum Input Range[1, 4]			3.156	V p-p
DAC:					
R_O	Output Resistance[2, 4]		2.5		Ω
V_{OOFF}	Output DC Offset[3]	−400		400	mV
V_{VREF}	Voltage Reference (V_{REF})	2.25		2.75	V
V_O	Maximum Voltage Output Swing (p–p) Across R_L				
	Single-Ended[4]			3.156	V p-p
	Differential[4]			6.312	V p-p
R_L	Load Resistance[2, 4]	2			kΩ

Test Conditions for all analog interface tests: Unity input gain, ADC PGA bypassed, D/A PGA set for 0 dB gain, no load on analog output ($VOUT_P$–$VOUT_N$).

[1]At input to sigma-delta modulator of ADC.
[2]At $VOUT_P$–$VOUT_N$.
[3]Between $VOUT_P$ and $VOUT_N$.
[4]Guaranteed but not tested.

GAIN

Parameter	Min	Typ	Max	Unit	Test Conditions
ADC Absolute Gain	−0.6	0	0.6	dBm0	1.0 kHz, 0 dBm0
ADC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0
DAC Absolute Gain	−0.6	0	0.6	dBm0	1.0 kHz, 0 dBm0
DAC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0
DAC PGA Relative Gain	−0.6		0.6	dBm0	1.0 kHz
ADC PGA Relative Gain	−0.6		0.6	dBm0	1.0 kHz

Parameter		Min	Max	Unit
Clock Signals				
Timing Requirement:				
t_{CK}[1]	CLKIN Period	76.9	150	ns
t_{CKL}	CLKIN Width Low	20		ns
t_{CKH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CPL}	CLKOUT Width Low	$0.5t_{CK}$ – 10		ns
t_{CPH}	CLKOUT Width High	$0.5t_{CK}$ – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[2]		ns

NOTES
[1]t_{CK} values within the range of CLKIN period should be substituted for all relevant timing parameters to obtain specification value. Example: t_{CPH} = 0.5 t_{CK} –10 ns = 0.5 (76.9) –10 ns = 28.5 ns.
[2]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 processor cycles assuming stable CLKIN (not including crystal oscillator start-up time).

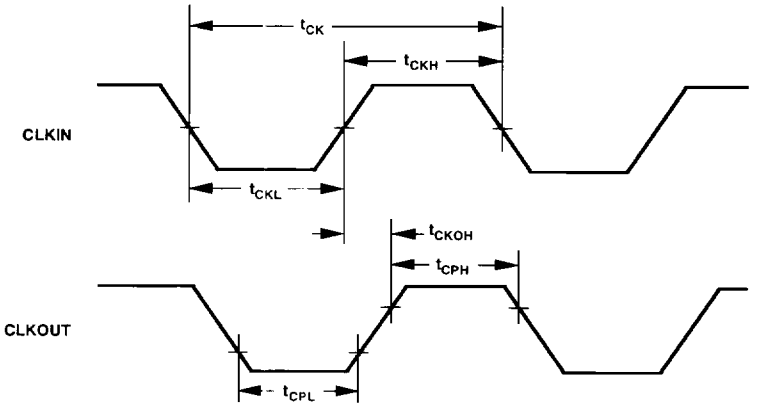


Figure 15. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	IRQx or FI Setup before CLKOUT Low[1, 2]	$0.25t_{CK}$ + 18		ns
t_{IFH}	IRQx or FI Hold after CLKOUT High[1, 2]	$0.25t_{CK}$		ns
	IRQx = $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$			
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT High	0		ns
t_{FOD}	Flag Output Delay from CLKOUT High		15	ns
	Flag Output = FL0, FL1, FL2, and FO			

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

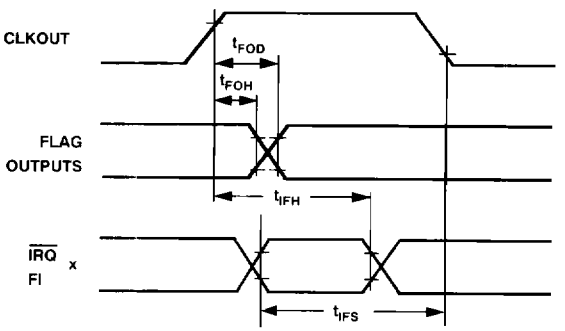


Figure 16. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 20		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ − 10		ns

NOTE
[1]$\overline{BR}$ is a synchronous signal which must meet setup/hold time requirements. Refer to the User's Manual for $\overline{BR}/\overline{BG}$ cycle relationships.

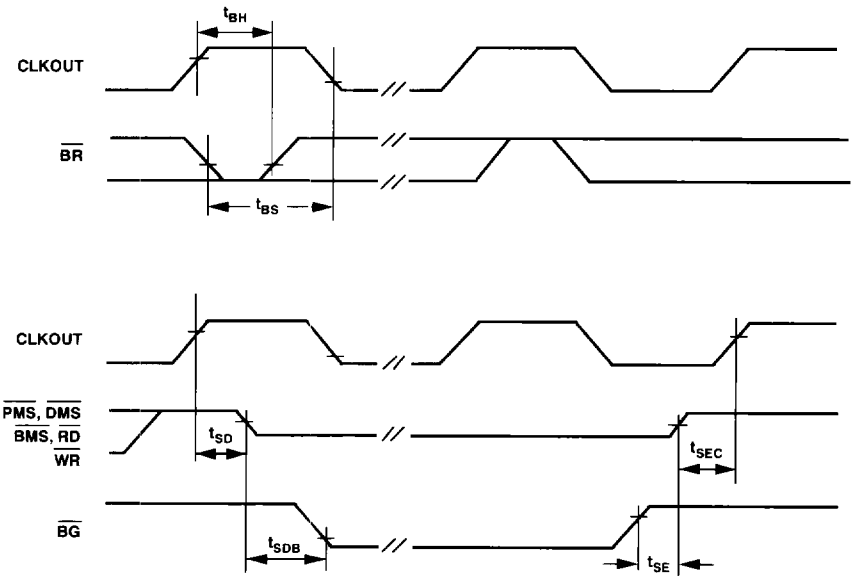


Figure 17. Bus Request – Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

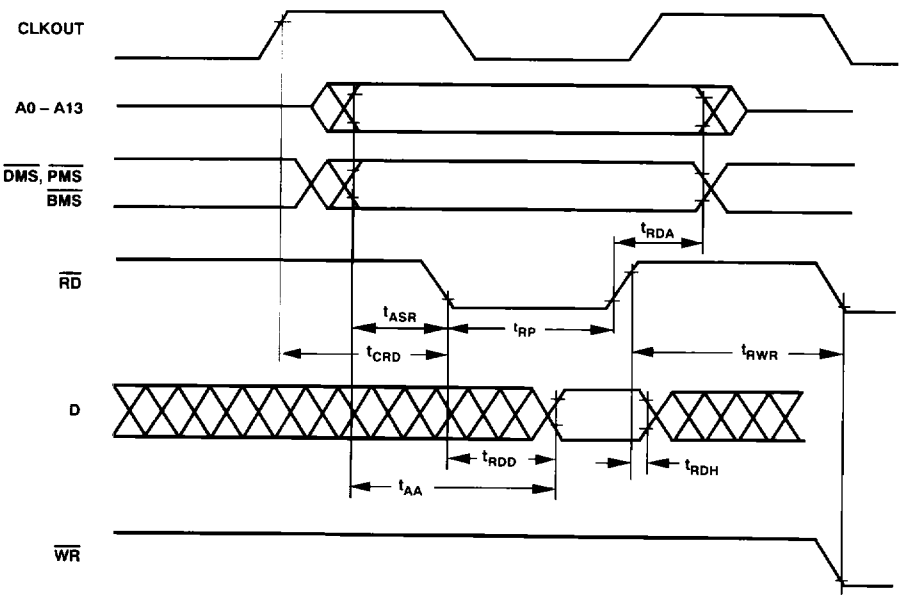


Figure 18. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

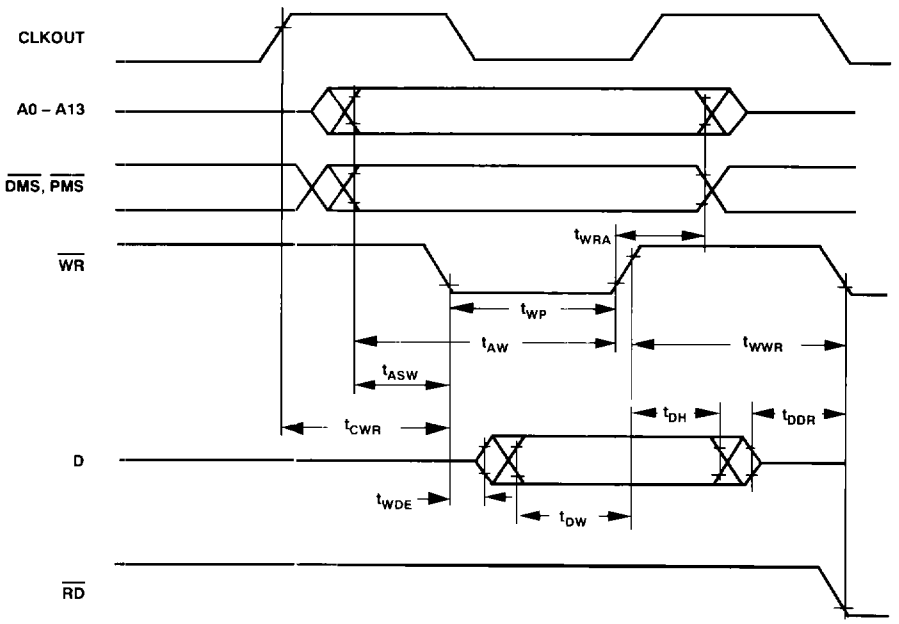


Figure 19. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	76.9		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		ns
t_{SCP}	$SCLK_{in}$ Width	28		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		20	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		20	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (alt) to DT Enable	0		ns
t_{TDV}	TFS (alt) to DT Valid		18	ns
t_{SCDD}	SCLK High to DT Disable		25	ns
t_{RDV}	RFS (multichannel, frame delay zero) to DT Valid		20	ns

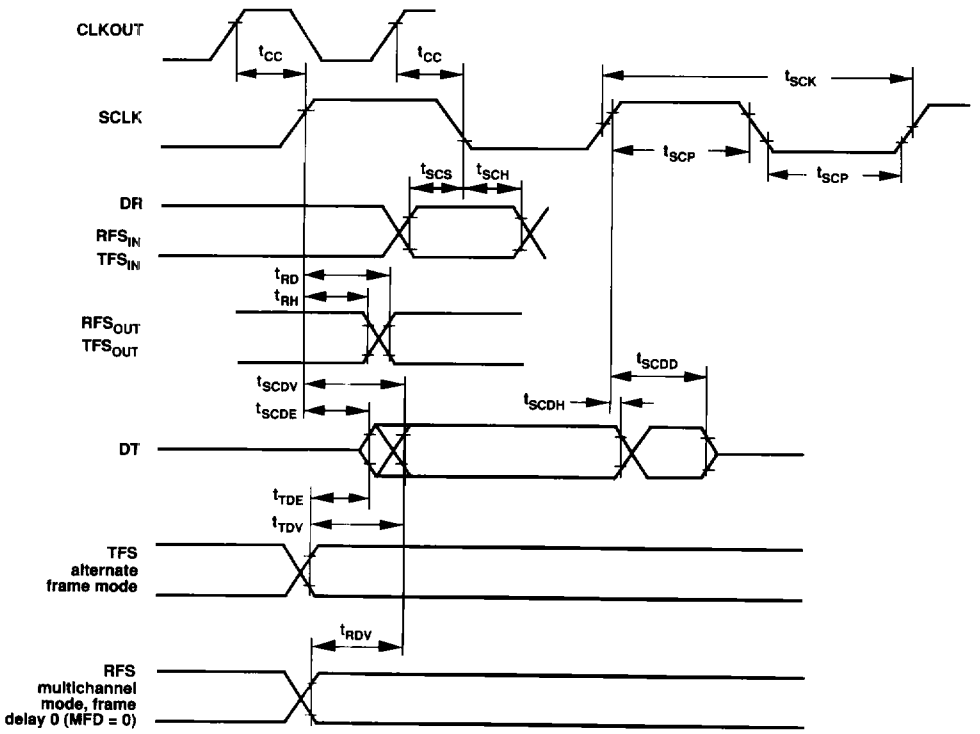
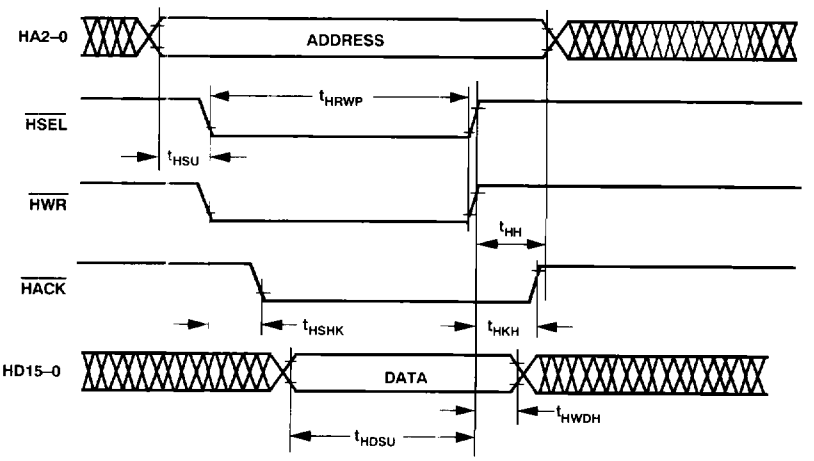


Figure 20. Serial Ports

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HSU}	HA2–0 Setup before Start of Write or Read[1, 2]	8		ns
t_{HDSU}	Data Setup before End of Write[3]	8		ns
t_{HWDH}	Data Hold after End of Write[3]	3		ns
t_{HH}	HA2–0 Hold after End of Write or Read[3, 4]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[2]	0		ns
t_{HDD}	Data Valid after Start of Read[2]		23	ns
t_{HRDH}	Data Hold after End of Read[4]	0		ns
t_{HRDD}	Data Disabled after End of Read[4]		10	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

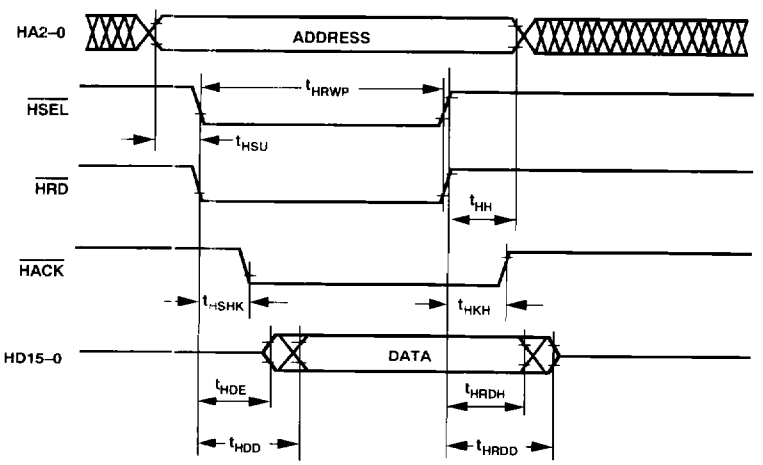
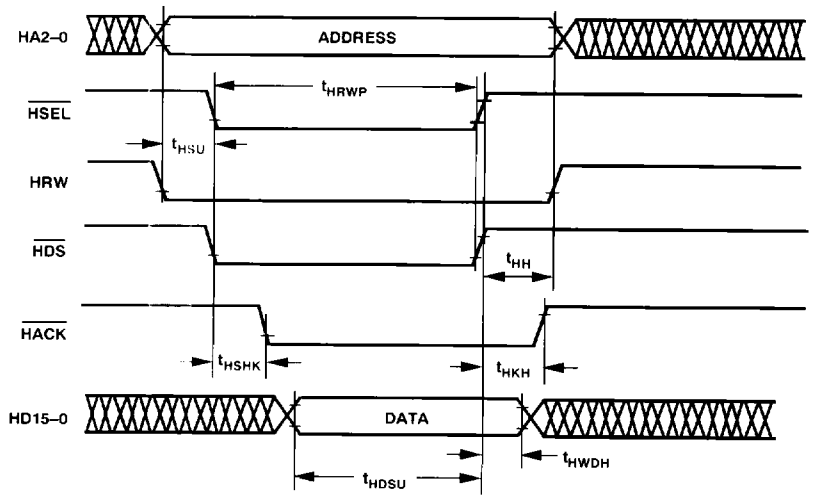


Figure 21. Host Interface Port (HMD1 = 0, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read/Write Strobe and Data Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	Data Setup before End of Write[2]	8		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		23	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		10	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High or $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

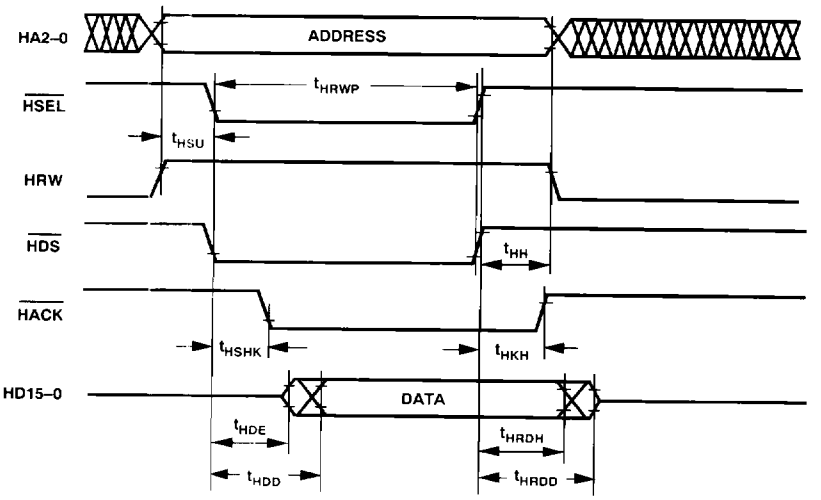


Figure 22. Host Interface Port (HMD1 = 0, HMD0 = 1)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	0		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	12		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	15		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[3]	8		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[4]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[4]		10	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

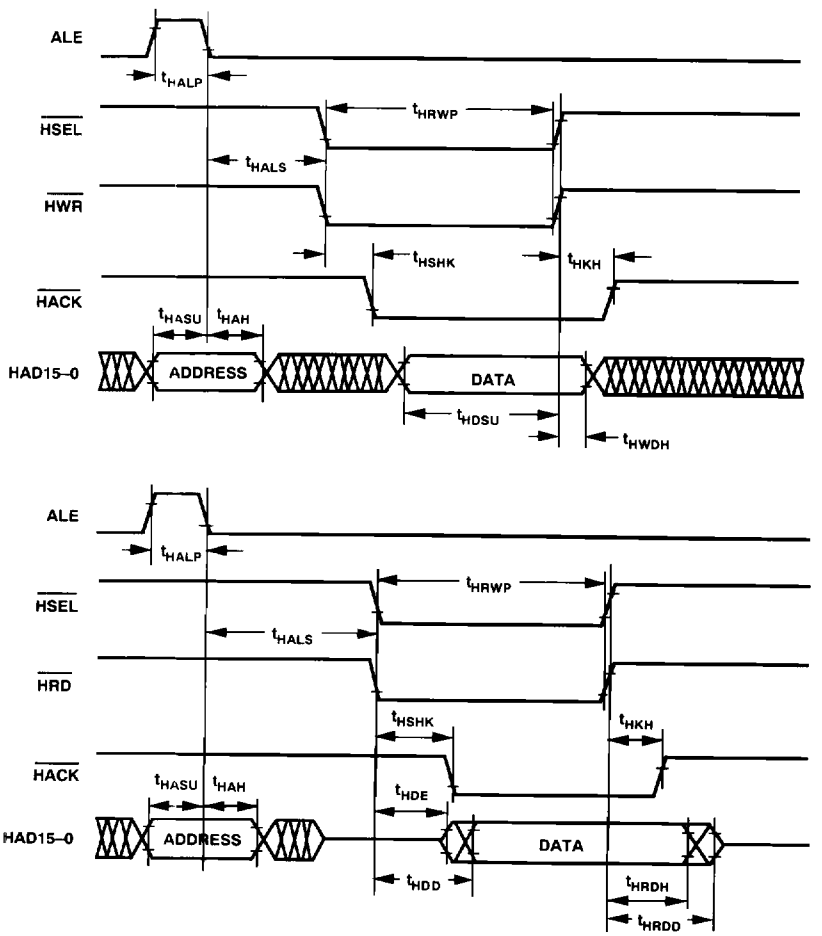
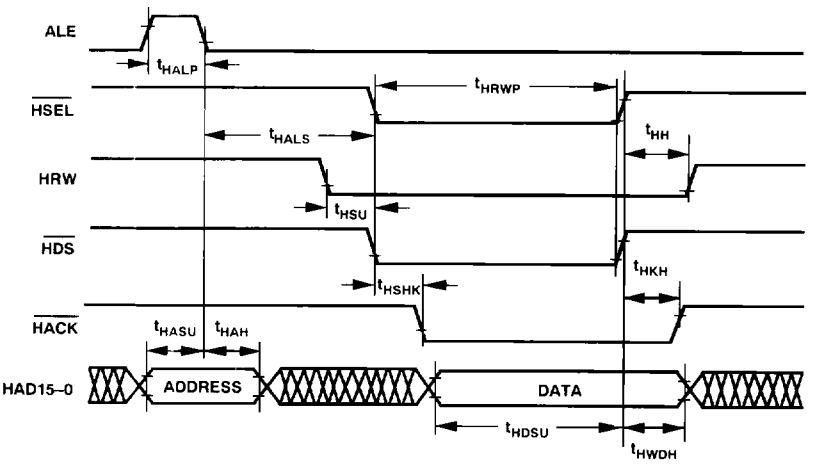


Figure 23. Host Interface Port (HMD1 = 1, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read/Write Strobe and Data Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	0		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	12		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	15		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		10	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High or $\overline{HSEL}$ High.
Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

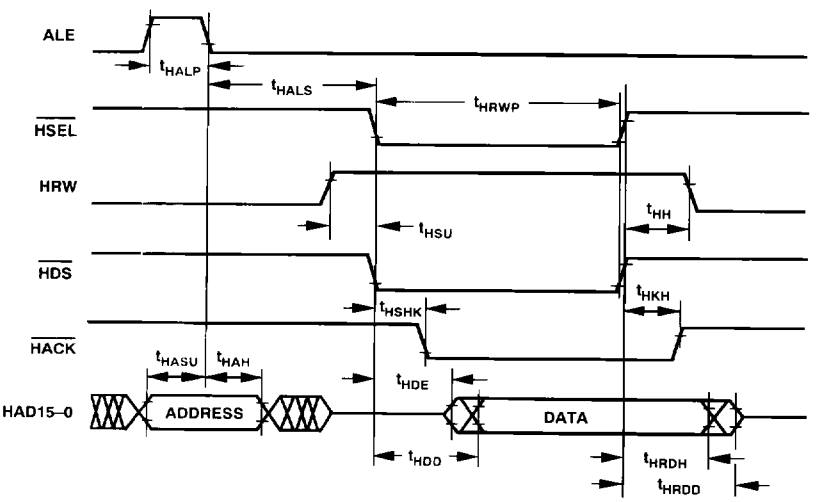


Figure 24. Host Interface Port (HMD1 = 1, HMD0 = 1)

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{amb} = T_{case} - (PD \times \theta_{CA})$

T_{case} = Case temp in °C
PD = Power dissipation in W
θ_{CA} = Thermal resistance (case-to-ambient)
θ_{JA} = Thermal resistance (junction-to-ambient)
θ_{JC} = Thermal resistance (junction-to-case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	20°C/W	6°C/W	14°C/W
PQFP-100 Lead	50°C/W	28°C/W	22°C/W

Power Dissipation

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows.

Assumptions:

- External data memory is accessed every cycle with 50% of address pins switching.
- External data memory writes occur every other cycle with 50% of address pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 76.9 ns.

Total Power Dissipation = P_{INT} + ($C \times V_{DD}^2 \times f$)

P_{INT} = internal power dissipation, from Power vs. Frequency graph. $C \times V_{DD}^2 \times f$ is calculated for each output:

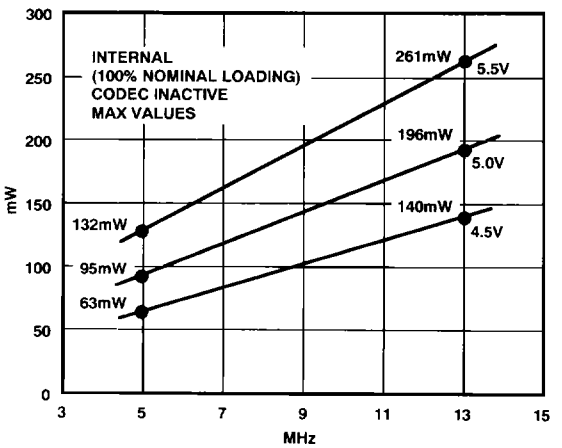
	# of Pins	× C	$\times V_{DD}^2$	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 13.0 MHz	=	26 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 6.5 MHz	=	15 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 6.5 MHz	=	2 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 13.0 MHz	=	3 mW
						46 mW

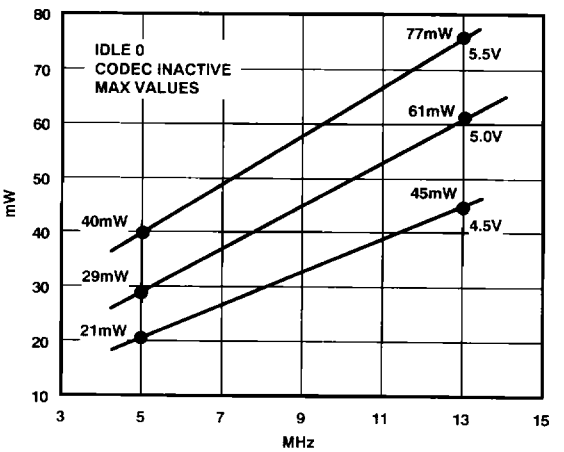
Total power dissipation for this example is P_{INT}+46 mW.

Typical Power Consumption

The typical power consumption can be calculated from the following data, taken at 5.0 V and +25°C executing 80% type 1 multifunction instructions, on random data.

Parameter	Typ
I_{DD} Digital Supply Current (IDLE, Codec Powered Up)	20 mA
I_{DD} Digital Supply Current (IDLE)	11 mA
I_{DD} Digital Supply Current (Dynamic, Codec Powered Up)	70 mA
I_{DD} Digital Supply Current (Powerdown)	10 µA
I_{CC}Analog Supply Current (Dynamic)	21 mA





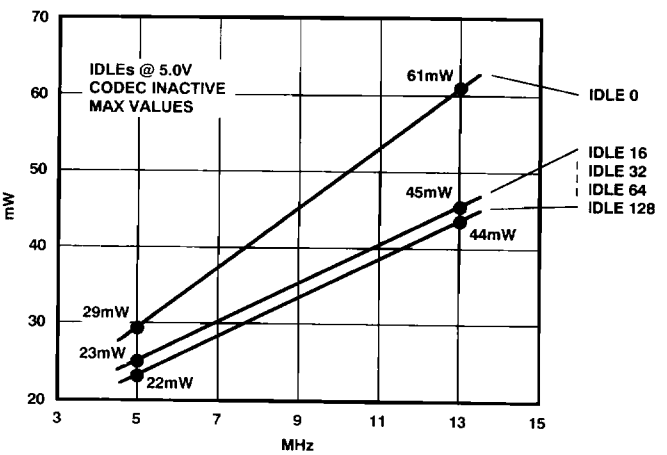


Figure 25. Power vs. Frequency

Analog Devices recommends that the ADSP-21msp5xA is used with a 13.0 MHz input clock. Below this input clock frequency, the codec performance will change and the performance specifications cannot be guaranteed. The codec filter characteristics will, however, scale approximately linearly with frequency.

If the codec is disabled, then the processor can be used at any allowed input clock frequency. The power consumption of the ADSP-21msp5xA at these frequencies is shown above.

CAPACITIVE LOADING

Figures 26 and 27 show capacitive loading characteristics for the ADSP-21msp5xA.

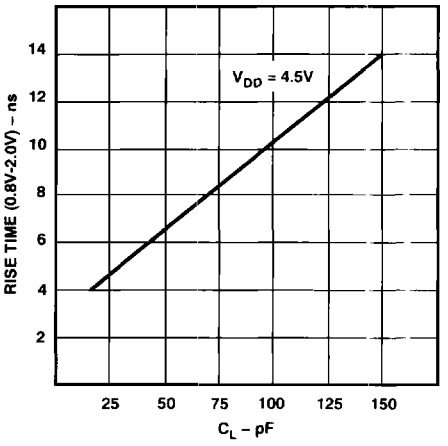


Figure 26. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

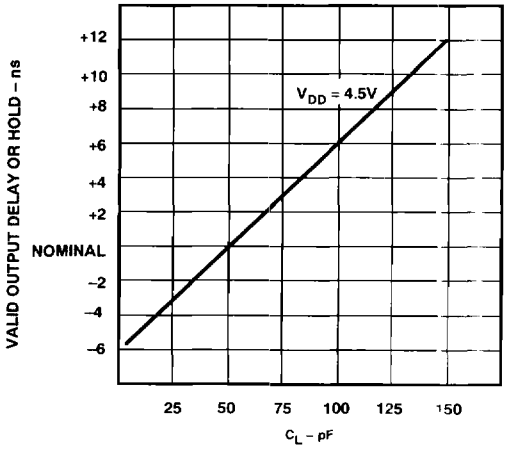


Figure 27. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Digital

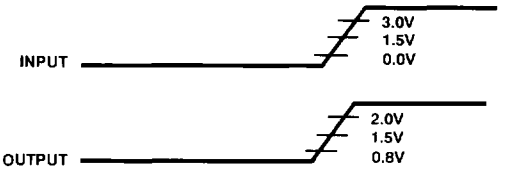


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Analog

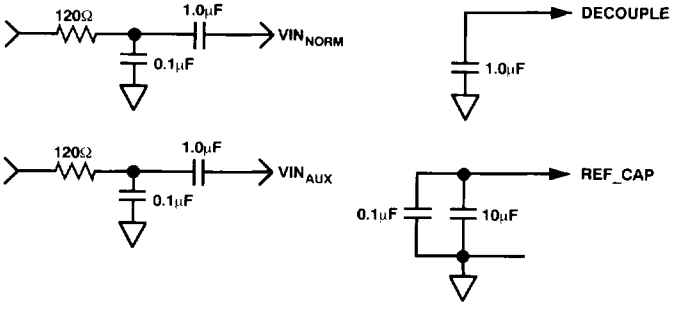


Figure 29. Analog Test Conditions

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time, $t_{MEASURED}$, is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

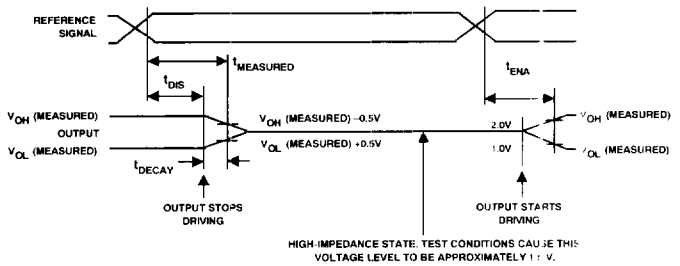


Figure 30. Output Enable/Disable

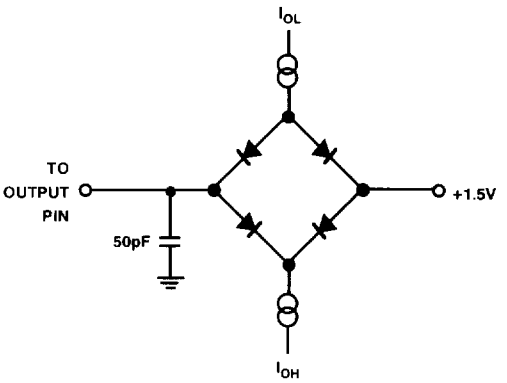
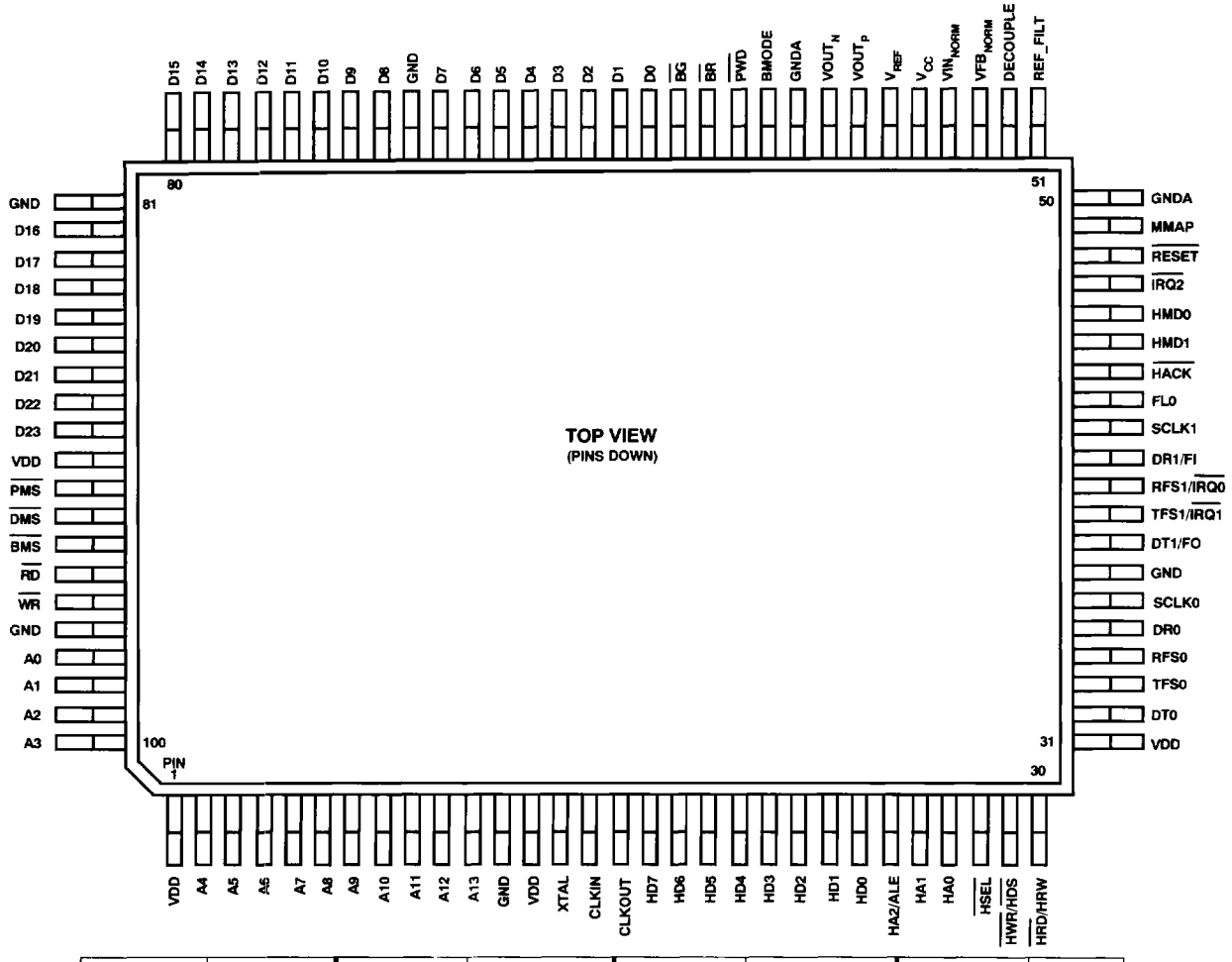


Figure 31. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

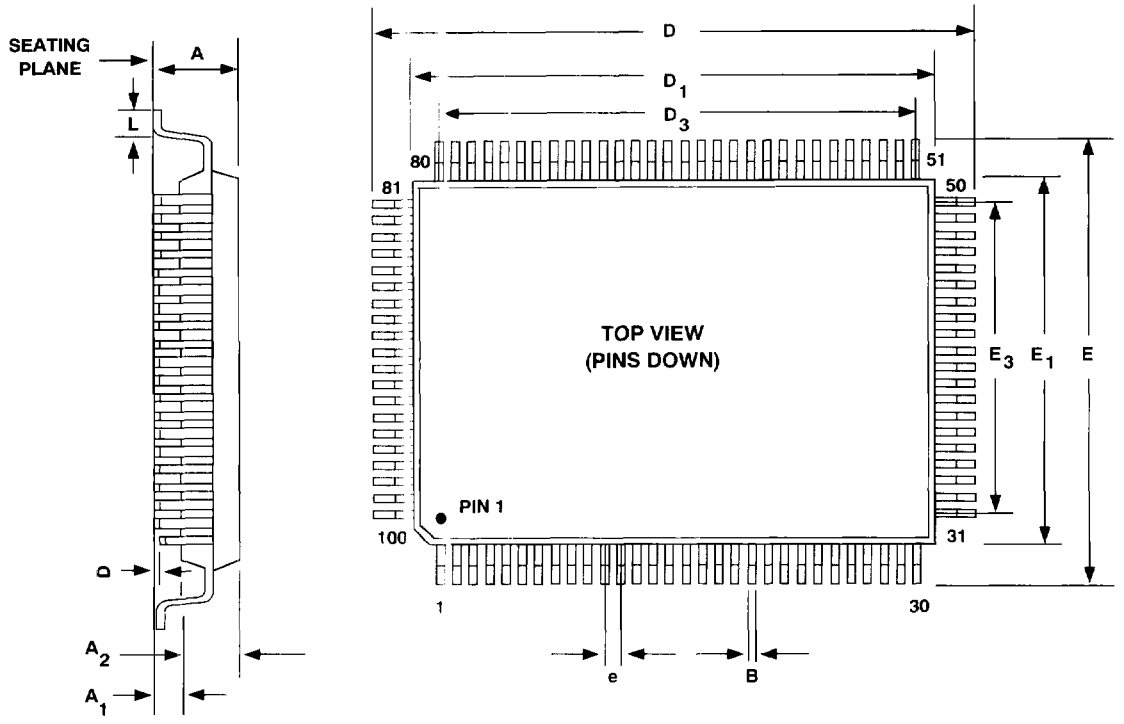
100-Lead PQFP Package Pinout



PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME
1	VDD	26	HA1	51	REF_FILT	76	D11
2	A4	27	HA0	52	VINAUX	77	D12
3	A5	28	$\overline{\text{HSEL}}$	53	DECOUPLE	78	D13
4	A6	29	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	54	VINNORM	79	D14
5	A7	30	$\overline{\text{HRD}}$/HRW	55	VCC	80	D15
6	A8	31	VDD	56	VREF	81	GND
7	A9	32	DT0	57	VOUTP	82	D16
8	A10	33	TFS0	58	VOUTN	83	D17
9	A11	34	RFS0	59	GNDA	84	D18
10	A12	35	DR0	60	BMODE	85	D19
11	A13	36	SCLK0	61	$\overline{\text{PWD}}$	86	D20
12	GND	37	GND	62	$\overline{\text{BR}}$	87	D21
13	VDD	38	DT1/FO	63	$\overline{\text{BG}}$	88	D22
14	XTAL	39	TFS1/$\overline{\text{IRQ1}}$	64	D0	89	D23
15	CLKIN	40	RFS1/$\overline{\text{IRQ0}}$	65	D1	90	VDD
16	CLKOUT	41	DR1/FI	66	D2	91	$\overline{\text{PMS}}$
17	HD7	42	SCLK1	67	D3	92	$\overline{\text{DMS}}$
18	HD6	43	FL0	68	D4	93	$\overline{\text{BMS}}$
19	HD5	44	$\overline{\text{HACK}}$	69	D5	94	$\overline{\text{RD}}$
20	HD4	45	HMD1	70	D6	95	$\overline{\text{WR}}$
21	HD3	46	HMD0	71	D7	96	GND
22	HD2	47	$\overline{\text{IRQ2}}$	72	GND	97	A0
23	HD1	48	$\overline{\text{RESET}}$	73	D8	98	A1
24	HD0	49	MMAP	74	D9	99	A2
25	HA2/ALE	50	GNDA	75	D10	100	A3

OUTLINE DIMENSIONS

100-Lead Metric Plastic Quad Flatpack (PQFP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.45			0.096
A_1	0.25			0.010		
A_2	1.90	2.00	2.10	0.075	0.079	0.083
D	22.95	23.20	23.45	0.903	0.913	0.923
D_1	19.90	20.00	20.10	0.783	0.787	0.791
D_3		18.85	18.92		0.742	0.745
E	16.95	17.20	17.45	0.667	0.677	0.687
E_1	13.90	14.00	14.10	0.547	0.551	0.555
E_3		12.35	12.42		0.486	0.489
L	0.65	0.80	0.95	0.026	0.031	0.037
e	0.57	0.65	0.73	0.023	0.026	0.029
B	0.25	0.30	0.35	0.009	0.012	0.015
Q			0.10			0.004

144-Lead PGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
R	REF_ FILT	VIN NORM	VREF	VOUT N	NC	NC	NC	NC	D0	D1	D5	D7	GND	D11	D15	R
P	NC	NC	DE-COUPLE	NC	VOUT P	B MODE	$\overline{PWD}$	$\overline{BR}$	D2	D3	D6	D8	D10	D14	NC	P
N	NC	MMAP	NC	VIN AUX	V_{CC}	GNDA	NC	$\overline{BG}$	NC	D4	D9	D12	D13	NC	NC	N
M	$\overline{IRQ2}$	$\overline{RESET}$	GNDA										NC	NC	D16	M
L	HMD1	HMD0	NC										PWD ACK	GND	D19	L
K	FL0	FL2	$\overline{HACK}$										D17	D18	D22	K
J	SCLK1	FL1	DR1/ FI										D21	D20	D23	J
H	$\overline{RFS1}$/ $\overline{IRQ0}$	NC	NC					PGA PACKAGE BOTTOM VIEW (PINS UP)					HSIZE	V_{DD}	V_{DD}	H
G	$\overline{TFS1}$/ $\overline{IRQ1}$	GND	DT1/ FO										$\overline{PMS}$	$\overline{RD}$	$\overline{DMS}$	G
F	NC	DR0	NC										GND	$\overline{WR}$	$\overline{BMS}$	F
E	SCLK0	TFS0	V_{DD}										HD13	HD15	GND	E
D	RFS0	NC	NC	INDEX (NC)									A3	A1	A0	D
C	DT0	NC	$\overline{HSEL}$	HA0	HD0	HD6	XTAL	V_{DD}	A11	A7	A5	NC	HD11	A2	HD14	C
B	NC	$\overline{HWR}$/ $\overline{HDS}$	HA2/ ALE	HD1	HD4	HD7	CLK OUT	GND	A10	A8	A6	HD10	V_{DD}	NC	HD12	B
A	$\overline{HRD}$/ HRW	HA1	HD2	HD3	HD5	CLKIN	NC	GND	A13	A12	A9	HD8	HD9	A4	NC	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
R	D15	D11	GND	D7	D5	D1	D0	NC	NC	NC	NC	VOUT N	VREF	VIN NORM	REF_ FILT	R
P	NC	D14	D10	D8	D6	D3	D2	$\overline{BR}$	$\overline{PWD}$	B MODE	VOUT P	NC	DE-COUPLE	NC	NC	P
N	NC	NC	D13	D12	D9	D4	NC	$\overline{BG}$	NC	GNDA	V_{CC}	VIN AUX	NC	MMAP	NC	N
M	D16	NC	NC										GNDA	$\overline{RESET}$	$\overline{IRQ2}$	M
L	D19	GND	PWD ACK										NC	HMD0	HMD1	L
K	D22	D18	D17										$\overline{HACK}$	FL2	FL0	K
J	D23	D20	D21										DR1/ FI	FL1	SCLK1	J
H	V_{DD}	V_{DD}	HSIZE					PGA PACKAGE TOP VIEW (PINS DOWN)					NC	NC	$\overline{RFS1}$/ $\overline{IRQ0}$	H
G	$\overline{DMS}$	$\overline{RD}$	$\overline{PMS}$										DT1/ FO	GND	$\overline{TFS1}$/ $\overline{IRQ1}$	G
F	$\overline{BMS}$	$\overline{WR}$	GND										NC	DR0	NC	F
E	GND	HD15	HD13										V_{DD}	TFS0	SCLK0	E
D	A0	A1	A3									INDEX (NC)	NC	NC	RFS0	D
C	HD14	A2	HD11	NC	A5	A7	A11	V_{DD}	XTAL	HD6	HD0	HA0	$\overline{HSEL}$	NC	DT0	C
B	HD12	NC	V_{DD}	HD10	A6	A8	A10	GND	CLK OUT	HD7	HD4	HD1	HA2/ ALE	$\overline{HWR}$/ $\overline{HDS}$	NC	B
A	NC	A4	HD9	HD8	A9	A12	A13	GND	NC	CLKIN	HD5	HD3	HD2	HA1	$\overline{HRD}$/ HRW	A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

NC = NO CONNECT

144-Pin PGA Pinout

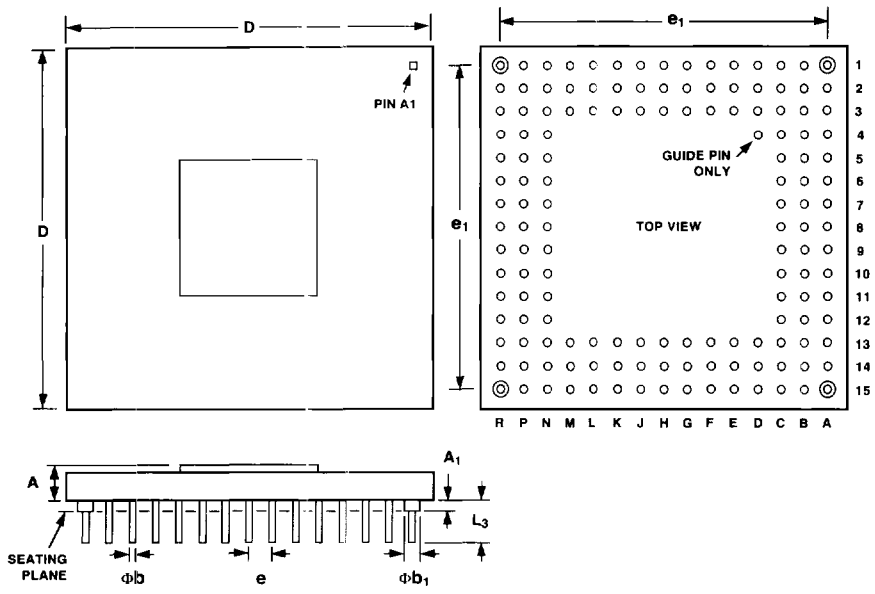
PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME
D3	NC	N4	VINAUX	M13	NC	C12	NC
C2	NC	P3	DECOUPLE	N14	NC	B13	VDD
B1	NC	R2	VINNORM	P15	NC	A14	A4
D2	NC	P4	NC	M14	NC	B12	HD10
E3	VDD	N5	VCC	L13	PWDACK	C11	A5
C1	DT0	R3	VREF	N15	NC	A13	HD9
E2	TFS0	P5	VOUTP	L14	GND	B11	A6
D1	RFS0	R4	VOUTN	M15	D16	A12	HD8
F3	NC	N6	GNDA	K13	D17	C10	A7
F2	DR0	P6	BMODE	K14	D18	B10	A8
E1	SCLK0	R5	NC	L15	D19	A11	A9
G2	GND	P7	$\overline{\text{PWD}}$	J14	D20	B9	A10
G3	DT1/FO	N7	NC	J13	D21	C9	A11
F1	NC	R6	NC	K15	D22	A10	A12
G1	TFS1/$\overline{\text{IRQ1}}$	R7	NC	J15	D23	A9	A13
H2	NC	P8	$\overline{\text{BR}}$	H14	VDD	B8	GND
H1	RFS1/$\overline{\text{IRQ0}}$	R8	NC	H15	VDD	A8	GND
H3	NC	N8	$\overline{\text{BG}}$	H13	HSIZE	C8	VDD
J3	DR1/FI	N9	NC	G13	$\overline{\text{PMS}}$	C7	XTAL
J1	SCLK1	R9	D0	G15	$\overline{\text{DMS}}$	A7	NC
K1	FL0	R10	D1	F15	$\overline{\text{BMS}}$	A6	CLKIN
J2	FL1	P9	D2	G14	$\overline{\text{RD}}$	B7	CLKOUT
K2	FL2	P10	D3	F14	$\overline{\text{WR}}$	B6	HD7
K3	$\overline{\text{HACK}}$	N10	D4	F13	GND	C6	HD6
L1	HMD1	R11	D5	E15	GND	A5	HD5
L2	HMD0	P11	D6	E14	HD15	B5	HD4
M1	$\overline{\text{IRQ2}}$	R12	D7	D15	A0	A4	HD3
N1	NC	R13	GND	C15	HD14	A3	HD2
M2	$\overline{\text{RESET}}$	P12	D8	D14	A1	B4	HD1
L3	NC	N11	D9	E13	HD13	C5	HD0
N2	MMAP	P13	D10	C14	A2	B3	HA2/ALE
P1	NC	R14	D11	B15	HD12	A2	HA1
M3	GNDA	N12	D12	D13	A3	C4	HA0
N3	NC	N13	D13	C13	HD11	C3	$\overline{\text{HSEL}}$
P2	NC	P14	D14	B14	NC	B2	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$
R1	REF_FILT	R15	D15	A15	NC	A1	$\overline{\text{HRD}}$/HWR

INDEX D4
NC = NO CONNECT

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

144-Pin Grid Array (PGA Package)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.841	0.859	21.36	21.82
A_1	0.045	0.055	1.14	1.40
D	1.559	1.591	39.60	40.41
e	0.100 TYP		2.54 TYP	
e_1	1.388	1.412	35.26	37.80
Φb_1	0.075 TYP		1.91 TYP	
Φb	0.050 TYP		1.27 TYP	
L_3	0.175	0.185	4.45	4.70