93425/93L425
1024 x 1-Bit Static
Random Access Memory

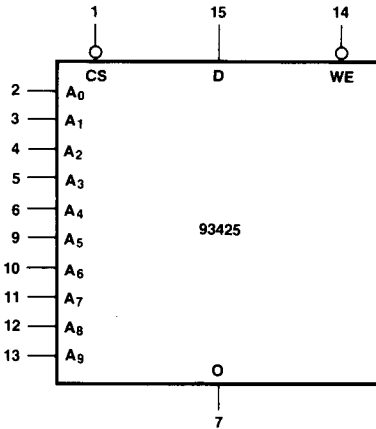Memory and High Speed Logic

Description

The 93425 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  953425 — 20 to 60 ns Max
- **Military Address Access Time**
  93425 — 30 to 70 ns Max
- **Low Power Version Also Available (93L425)**
- **Features Three State Output**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable (Active LOW)
D	Data Input
O	Data Output

Connection Diagram
16-Pin DIP (Top View)

Pin			Pin
$\overline{CS}$	1	16	V_{CC}
A_0	2	15	D
A_1	3	14	$\overline{WE}$
A_2	4	13	A_9
A_3	5	12	A_8
A_4	6	11	A_7
O	7	10	A_6
GND	8	9	A_5
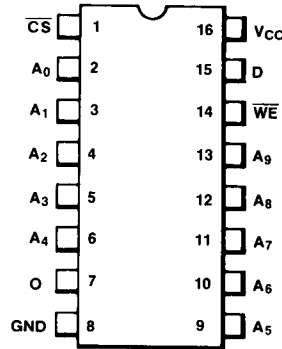
Note:
The 16 pin Flatpak version has the same pinout connections as the Dual In-line package.

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Logic Symbol

V_{CC} = Pin 16
GND = Pin 8

Logic Diagram

A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9
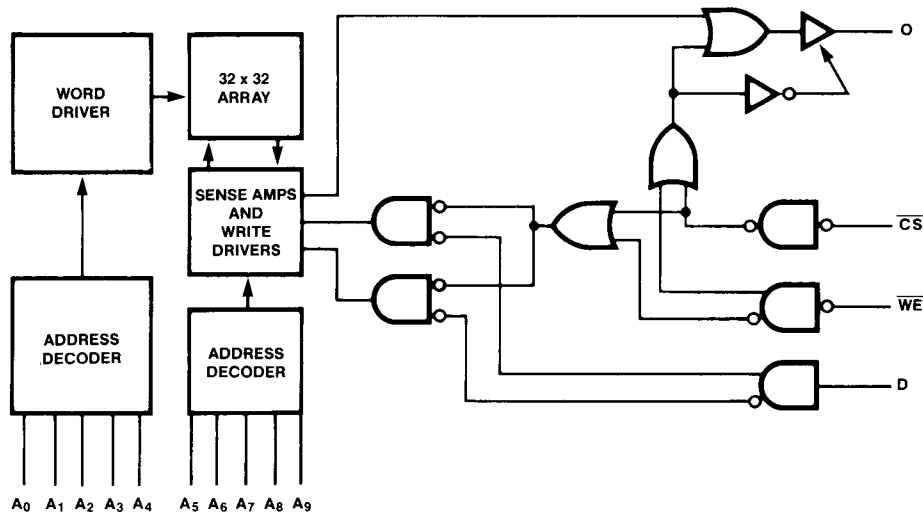
Functional Description

The 93425 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93425 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A_0 through A_9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

The 93425 has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D	O	Mode
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

DC Performance Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs[5]
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs[5]
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA
I_{IL}	Input LOW Current		−250	−400[7]	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground			−100	mA	V_{CC} = Max, Note 3
I_{CC}	Power Supply Current			65	mA	93L425-35, 93L425-45, 93L425-60 (commercial)
				75	mA	93L425-40, 93L425-50, 93L425-70 (military)
				125	mA	93425-25, 93425-30 (commercial)
				135	mA	93425-30, 93425-40 (military)
				155	mA	93425A, 93425-45 (commercial)
				170	mA	93425-60 (military) V_{CC} = Max, Note 6

Notes

1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.

4. t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.
5. Static condition only.
6. All inputs GND Output open
7. I_{IL} = −300 μA for 93L425

93425/93L425

Commercial
AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, $T_C = 0°$ C to $+75°$ C

Symbol	Characteristic	93425-20 93425-25 Min	Max	93425-30 93425A Min	Max	93425-45 Min	Max	Unit	Condition
	Read Timing								
t_{ACS}	Chip Select Access Time		15		20		35	ns	Figures 3a, 3b
t_{ZRCS}	Chip Select to HIGH Z		20		20		35	ns	
t_{AA}	Address Access Time[2]		20/25		30		45	ns	
	Write Timing								
t_{W}	Write Pulse Width to Guarantee Writing[4]	15		20		35		ns	Figure 4
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		5		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		15		20		35	ns	
t_{WR}	Write Recovery Time		15		20		40	ns	
t_{WR}	Write Recovery Time (93425A)				25			ns	

Military
AC Performance Characteristics: $V_{CC} = 5.0$ V $\pm 10\%$, GND = 0 V, $T_C = -55°$ C to $+125°$ C

Symbol	Characteristic	93425-30 Min	Max	93425-40 Min	Max	93425-60 Min	Max	Unit	Condition
	Read Timing								
t_{ACS}	Chip Select Access Time		20		25		45	ns	Figures 3a, 3b
t_{ZRCS}	Chip Select to HIGH Z		20		25		50	ns	
t_{AA}	Address Access Time[2]		30		40		60	ns	
	Write Timing								
t_{W}	Write Pulse Width to Guarantee Writing[4]	20		25		40		ns	Figure 4
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		10		15		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		20		25		45	ns	
t_{WR}	Write Recovery Time		20		25		50	ns	

Notes on preceding page

Commercial
AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, $T_C = 0°$ C to +75° C

Symbol	Characteristic	93L425-35		93L425-45		93L425-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		25		30		40	ns	*Figures 3a,*
t_{ZRCS}	Chip Select to HIGH Z		25		30		40	ns	*3b*
t_{AA}	Address Access Time[2]		35		45		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	30		35		45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		10		ns	*Figure 4a,*
t_{WHA}	Address Hold Time after Write	5		5		5		ns	*4b*
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		20		25		45	ns	
t_{WR}	Write Recovery Time		30		35		45	ns	

Military
AC Performance Characteristics: $V_{CC} = 5.0$ V $\pm$ 10%, GND = 0 V, $T_C = -55°$ C to +125° C

Symbol	Characteristic	93L425-40		93L425-50		93L425-70		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		30		35		45	ns	*Figures 3a,*
t_{ZRCS}	Chip Select to HIGH Z		25		30		50	ns	*3b*
t_{AA}	Address Access Time[2]		40		50		70	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		50		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		10		ns	
t_{WHD}	Data Hold Time after Write	5		5		10		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	10		10		10		ns	*Figure 4a,*
t_{WHA}	Address Hold Time after Write	5		5		10		ns	*4b*
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{ZWS}	Write Enable to HIGH Z		25		30		45	ns	
t_{WR}	Write Recovery Time		30		40		55	ns	

Notes on page 4-27

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Fig. 1   AC Test Output Load

LOAD A

LOAD B
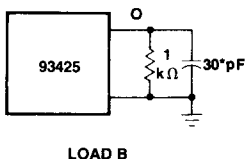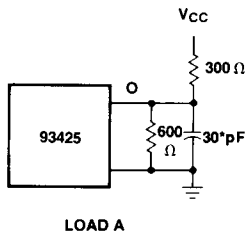
*Includes jig and probe capacitance

Note: Load A is used for all production testing.

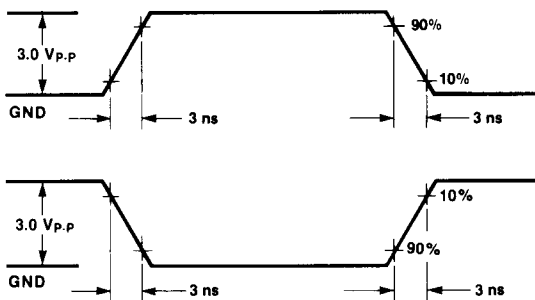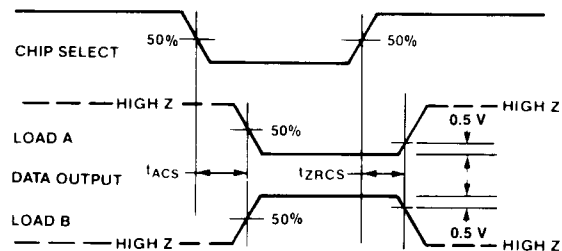## Fig. 2   AC Test Input Levels

Fig. 3   Read Mode Timing

3a   Read Mode Propagation Delay from Chip Select

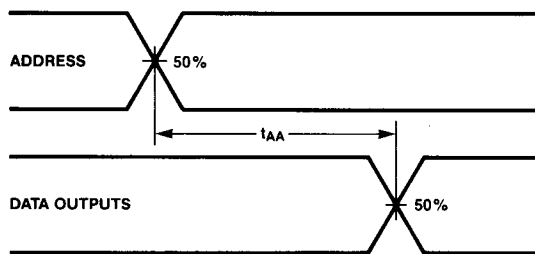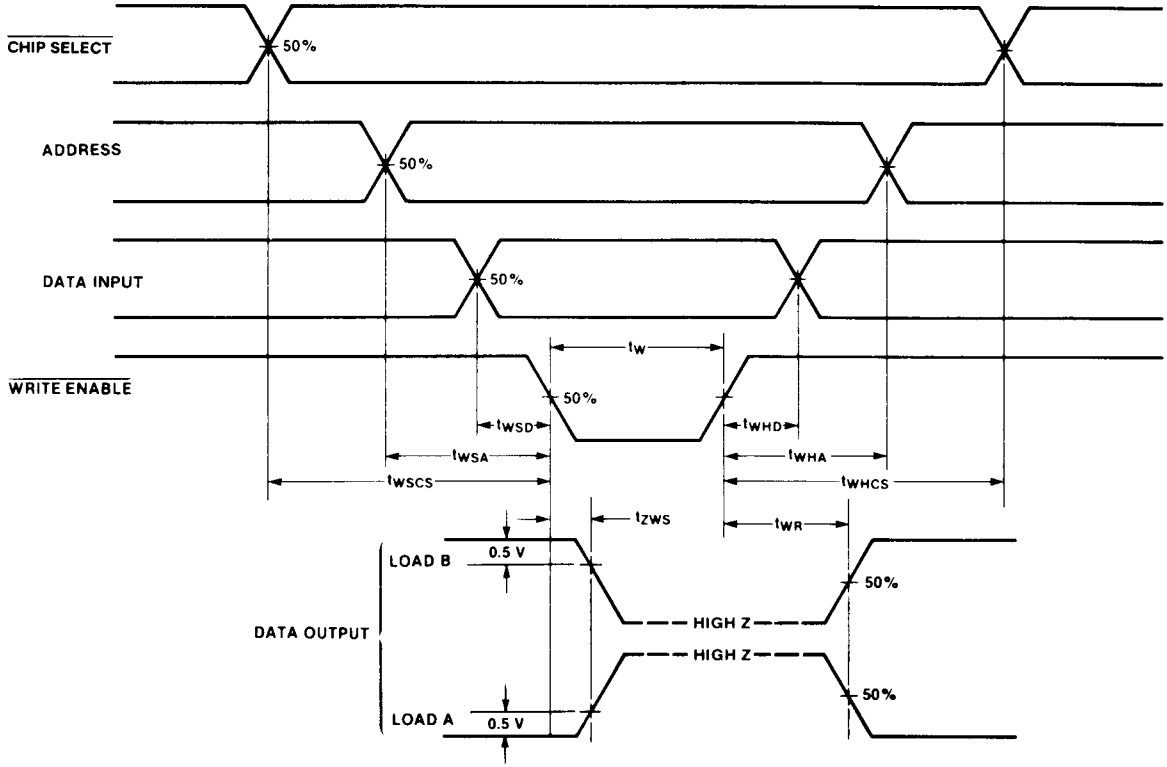### 3b   Read Mode Propagation Delay from Address

Fig. 4 Write Mode Timing

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Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

93425/93L425

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Ordering Information

Part Number	Access Time (ns)	Power (mA)	Temperature Range	Package	Order Code
93425-20	20	125	0°C to +75°C	XX	93425XX20
93425-25	25	125	0°C to +75°C	XX	93425XX25
93425A	30	155	0°C to +75°C	XX	93425AXX
93425-30	30	125	0°C to +75°C	XX	93425XX30
93425-30	30	135	−55°C to +125°C	YY	93425YY30
93L425-35	35	65	0°C to +75°C	XX	93L425XX35
93425-40	40	135	−55°C to +125°C	YY	93425YY40
93L425-40	40	75	−55°C to +125°C	YY	93L425YY40
93425-45	45	155	0°C to +75°C	XX	93425XX —
93L425-45	45	65	0°C to +75°C	XX	93L425XX45
93L425-50	50	75	−55°C to +125°C	YY	93L425YY50
93L425-60	60	65	0°C to +75°C	XX	93L425XX
93425-60	60	170	−55°C to +125°C	YY	93425YY
93L425-70	70	75	−55°C to +125°C	YY	93L425YY

Packages and Optional Processing (See Section 9)

XX — Commercial

Without Optional Processing	With Optional Processing	
DC	DCQR	— Ceramic Dip
FC	FCQR	— Cerpak
PC	PCQR	— Plastic Dip

YY — Military

Without Optional Processing	With Optional Processing	
DM	DMQB	— Ceramic Dip
FM	FMQB	— Cerpak

Optional Processing
QB = Mil Std 883
　　　Method 5004 and 5005, Level B
QR = Commercial Device with
　　　160 Hour Burn in or Equivalent

Note:
Because every combination of packaging, speed, temperature, and optional processing is not in stock, availability of some combinations is not on an immediate basis.