



## 2 x 2 Clock and Data Switch Buffer

### Features

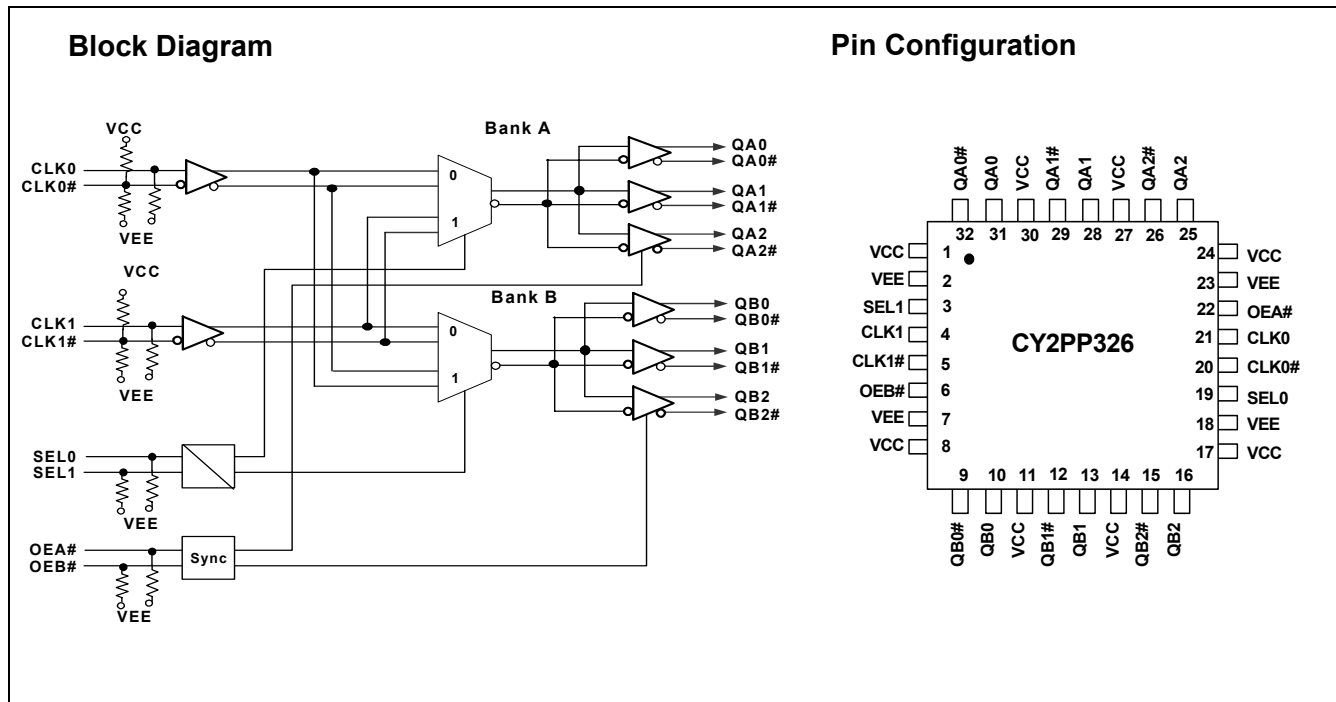
- Six ECL/PECL differential outputs
- Two ECL/PECL differential inputs
- Hot-swappable/-insertable
- 50 ps output-to-output skew
- 250 ps device-to-device skew
- 950 ps propagation delay (typical)
- 1.2 GHz Operation
- 2.8 ps RMS period jitter (max.)
- PECL mode supply range:  $V_{EE} = -2.5V \pm 5\%$  to  $-3.3V \pm 5\%$  with  $V_{EE} = 0V$
- ECL mode supply range:  $V_{CC} = 2.5V \pm 5\%$  to  $3.3V \pm 5\%$  with  $V_{EE} = 0V$
- Industrial temperature range:  $-40^{\circ}C$  to  $85^{\circ}C$
- 32-pin 1.4mm TQFP package
- Temperature compensation like 100K ECL
- Pin Compatible with MC100ES6254

### Functional Description

The CY2PP326 is a low-skew, low propagation delay 2 x 2 differential clock, data switch, and fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low-signal skews at operating frequencies of up to 1.5 GHz.

The device features two differential input paths which are multiplexed internally to six outputs grouped in two banks. The muxes are controlled by SEL(0:1) control inputs. The CY2PP326 may function as 1:6 or 2x 1:3 clock/data buffer and as a clock/data repeater or multiplexer.

Since the CY2PP326 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems and for switching data signals between different channels. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP326 delivers consistent, guaranteed performance over differing platforms.



**Pin Definitions**

Pin	Name	I/O <sup>[1]</sup>	Type <sup>[2]</sup>	Description
19,3	SEL0,SEL1	I	LVC MOS	<b>Clock/Data Switch Select.</b>
22,6	OEA#,OEB#	I	LVC MOS	<b>Output Enable.</b>
21,4	CLK(0:1)	I,PD	ECL/PECL	<b>True Differential Inputs.</b>
20,5	CLK(0:1)#	I,PD/PU	ECL/PECL	<b>Complement Differential Inputs.</b>
31,28,25 32,29,26	QA(0:2) QA(0:2)#	O	ECL/PECL	<b>Differential Outputs – Bank A.</b>
10,13,16 9,12,15	QB(0:2) QB(0:2)#	O	ECL/PECL	<b>Differential Outputs – Bank B.</b>
2,7,18,23,	VEE	–PWR	GND	<b>Negative Power Supply.</b>
1,8,11,14,17,24,27,30	VCC	+PWR	POWER	<b>Positive Power Supply.</b>

**Table 1. Function Table**

Control	Default	0	1
OAE#	0	QA(0–2), QX(0–2)# are active. Deassertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.	QA(0–2)= L, QX(0–2)# = H. Assertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.
OEB#	0	QA(0–2), QX(0–2) are active. Deassertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.	QA(0–2)= L, QX(0–2)# = H. Assertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.
SEL0,SEL1	00	See <i>Table 2</i>	

**Table 2. Clock Select Control**

SEL0	SEL1	CLK0 Routed to	CLK1 Routed to	Application Mode
0	0	QA(0:2) and QB(0:2)	–	1:6 fanout of CLK0
0	1	–	QA(0:2) and QB(0:2)	1:6 fanout of CLK1
1	0	QA(0:2)	QB(0:2)	Dual 1:3 buffer
1	1	QB(0:2)	QA(0:2)	Dual 1:3 buffer crossed

**Governing Agencies**

The following agencies provide specifications that apply to the CY2PP326. The agency name and relevant specification is listed below in *Table 3*.

**Table 3.**

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

**Notes:**

- In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power
- In ECL mode (negative power supply mode), V<sub>EE</sub> is either –3.3V or –2.5V and V<sub>CC</sub> is connected to GND (0V). In PECL mode (positive power supply mode), V<sub>EE</sub> is connected to GND (0V) and V<sub>CC</sub> is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V<sub>CC</sub>) and are between V<sub>CC</sub> and V<sub>EE</sub>.

**Absolute Maximum Ratings**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>CC</sub>	Positive Supply Voltage	Non-Functional	-0.3	4.6	V
V <sub>EE</sub>	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T <sub>S</sub>	Temperature, Storage	Non-Functional	-65	+150	°C
T <sub>J</sub>	Temperature, Junction	Non-Functional		150	°C
ESD <sub>h</sub>	ESD Protection	Human Body Model		2000	V
M <sub>SL</sub>	Moisture Sensitivity Level			3	N.A.
Gate Count	Total Number of Used Gates	Assembled Die		50	gates

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Operating Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
LU <sub>I</sub>	Latch Up Immunity	Functional, typical		100	mA
T <sub>A</sub>	Temperature, Operating Ambient	Functional	-40	+85	°C
∅ <sub>Jc</sub>	Dissipation, Junction to Case	Functional		29 <sup>[3]</sup>	°C/W
∅ <sub>Ja</sub>	Dissipation, Junction to Ambient	Functional		75 <sup>[3]</sup>	°C/W
I <sub>EE</sub>	Maximum Quiescent Supply Current	V <sub>EE</sub> pin		130 <sup>[4]</sup>	mA
C <sub>IN</sub>	Input pin capacitance			3	pF
L <sub>IN</sub>	Pin Inductance			1	nH
V <sub>IN</sub>	Input Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>	-0.3	V <sub>CC</sub> + 0.3	V
V <sub>TT</sub>	Output Termination Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>		V <sub>CC</sub> - 2	V
V <sub>OUT</sub>	Output Voltage	Relative to V <sub>CC</sub> <sup>[5]</sup>	-0.3	V <sub>CC</sub> + 0.3	V
I <sub>IN</sub>	Input Current <sup>[6]</sup>	V <sub>IN</sub> = V <sub>IL</sub> , or V <sub>IN</sub> = V <sub>IH</sub>		1150I	uA

**PECL DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>CC</sub>	Operating Voltage	2.5V ± 5%, V <sub>EE</sub> = 0.0V 3.3V ± 5%, V <sub>EE</sub> = 0.0V	2.375 3.135	2.625 3.465	V V
V <sub>CMR</sub>	Differential Cross Point Voltage <sup>[7]</sup>	Differential operation	1.2	V <sub>CC</sub>	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -30 mA <sup>[8]</sup>	V <sub>CC</sub> - 1.25	V <sub>CC</sub> - 0.7	V
V <sub>OL</sub>	Output Low Voltage V <sub>CC</sub> = 3.3V ± 5% V <sub>CC</sub> = 2.5V ± 5%	I <sub>OL</sub> = -5 mA <sup>[8]</sup>	V <sub>CC</sub> - 1.995 V <sub>CC</sub> - 1.995	V <sub>CC</sub> - 1.5 V <sub>CC</sub> - 1.3	V V
V <sub>IH</sub>	Input Voltage, High	Single-ended operation	V <sub>CC</sub> - 1.165	V <sub>CC</sub> - 0.880 <sup>[9]</sup>	V
V <sub>IL</sub>	Input Voltage, Low	Single-ended operation	V <sub>CC</sub> - 1.945 <sup>[9]</sup>	V <sub>CC</sub> - 1.625	V

**Notes:**

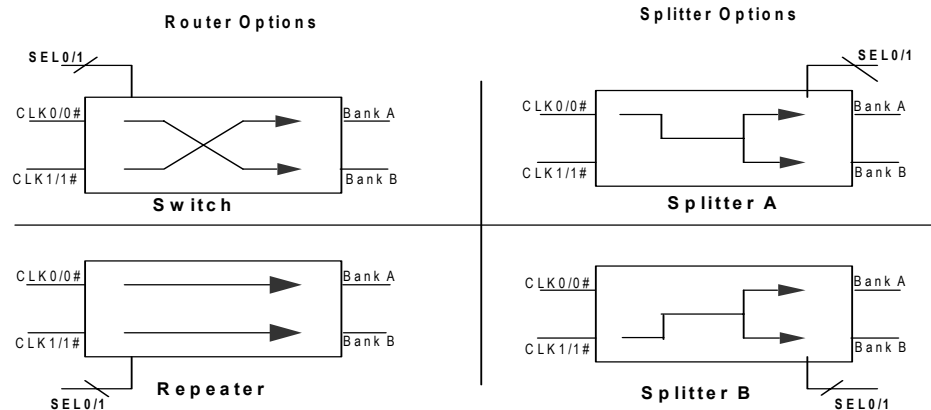
- Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
- Power Calculation: V<sub>CC</sub> \* I<sub>EE</sub> + 0.5 (I<sub>OH</sub> + I<sub>OL</sub>) (V<sub>OH</sub> - V<sub>OL</sub>) (number of differential outputs used); I<sub>EE</sub> does not include current going off chip.
- where V<sub>CC</sub> is 3.3V±5% or 2.5V±5%
- Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
- Refer to Figure 1
- Equivalent to a termination of 50Ω to V<sub>TT</sub>. I<sub>OHMIN</sub>=(V<sub>OHMIN</sub>-V<sub>TT</sub>)/50; I<sub>OHMAX</sub>=(V<sub>OHMAX</sub>-V<sub>TT</sub>)/50; I<sub>OLMIN</sub>=(V<sub>OLMIN</sub>-V<sub>TT</sub>)/50; I<sub>OLMAX</sub>=(V<sub>OLMAX</sub>-V<sub>TT</sub>)/50;
- V<sub>IL</sub> will operate down to V<sub>EE</sub>; V<sub>IH</sub> will operate up to V<sub>CC</sub>

**ECL DC Electrical Specifications**

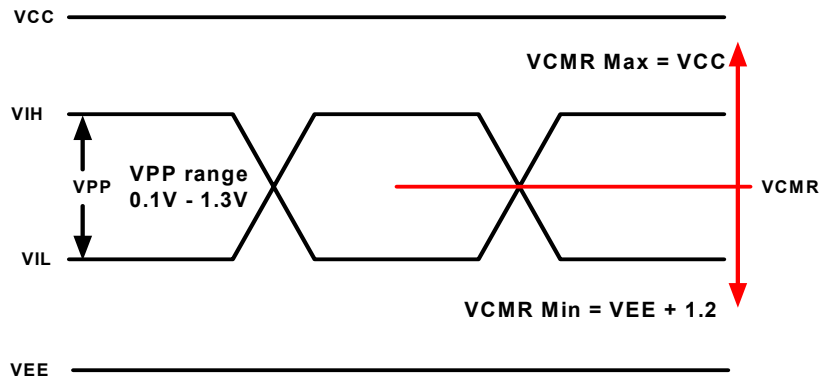
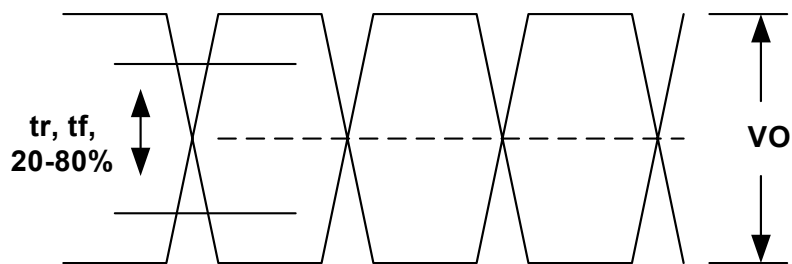
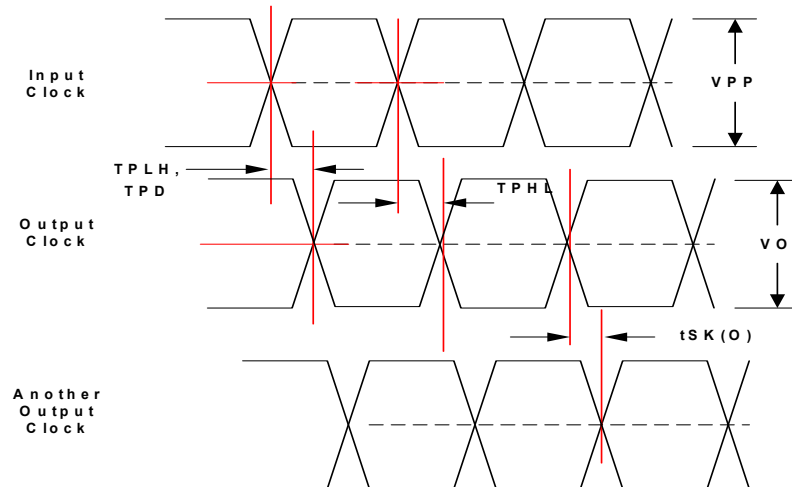
Parameter	Description	Condition	Min.	Max.	Unit
$V_{EE}$	Negative Power Supply	$-2.5V \pm 5\%$ , $V_{CC} = 0.0V$ $-3.3V \pm 5\%$ , $V_{CC} = 0.0V$	-2.625 -3.465	-2.375 -3.135	V
$V_{CMR}$	Differential cross point voltage <sup>[7]</sup>	Differential operation	$V_{EE} + 1.2$	0V	V
$V_{OH}$	Output High Voltage	$I_{OH} = -30 \text{ mA}$ <sup>[8]</sup>	-1.25	-0.7	V
$V_{OL}$	Output Low Voltage $V_{EE} = -3.3V \pm 5\%$ $V_{EE} = -2.5V \pm 5\%$	$I_{OL} = -5 \text{ mA}$ <sup>[8]</sup>	-1.995 -1.995	-1.5 -1.3	V
$V_{IH}$	Input Voltage, High	Single-ended operation	-1.165	-0.880 <sup>[9]</sup>	V
$V_{IL}$	Input Voltage, Low	Single-ended operation	-1.945 <sup>[9]</sup>	-1.625	V

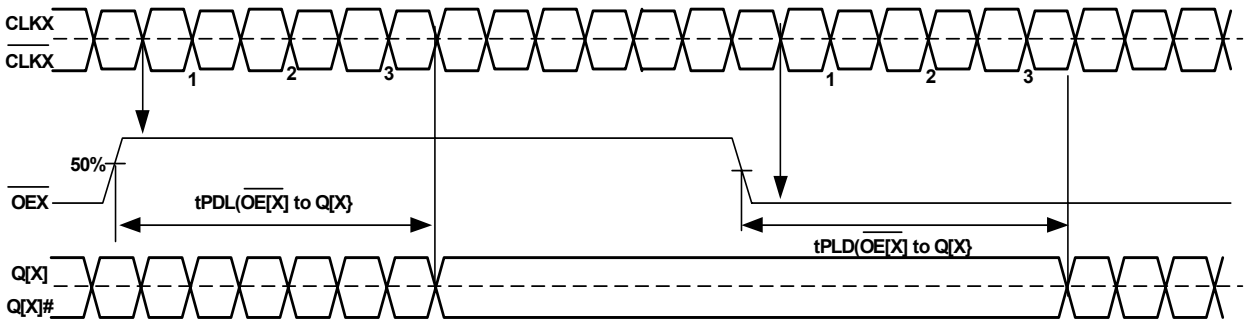
**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
$V_{PP}$	Differential Input Voltage <sup>[7]</sup>	Differential operation	0.1	1.3	V
$F_{CLK}$	Input Frequency	50% duty cycle Standard load	–	1.5	GHz
$T_{PD}$	Propagation Delay CLKA or CLKB to Output pair	< 1 GHz <sup>[10]</sup>	–	1200	ps
$V_o$	Output Voltage (peak-to-peak; see Figure 2)	< 1 GHz	0.375	–	V
$V_{CMRO}$	Output Common Voltage Range (typ.)		$V_{CC} - 1.425$		V
$tsk_{(0)}$	Output-to-output Skew	660 MHz <sup>[10]</sup> , See Figure 3	–	50	ps
$tsk_{(PP)}$	Part-to-Part Output Skew	660 MHz <sup>[10]</sup>	–	250	ps
$T_{PER}$	Output Period Jitter (rms) <sup>[11]</sup>	660 MHz <sup>[10]</sup>	–	2.8	ps
$tsk_{(P)}$	Output Pulse Skew <sup>[12]</sup>	660 MHz <sup>[10]</sup> , See Figure 3	–	75	ps
$T_R, T_F$	Output Rise/Fall Time (see Figure 2)	660 MHz 50% duty cycle Differential 20% to 80%	0.08	0.3	ns
$t_{PDL}$	Output disable time	$T = \text{CLK period}$	$2.5T + T_{PD}$	$3.5T + T_{PD}$	ns
$t_{PLD}$	Output enable time	$T = \text{CLK period}$	$3.0T + T_{PD}$	$4.0T + T_{PD}$	ns


**Figure 1. Channel Cross Point Switch/Mux Configurations**
**Notes:**

10. 50% duty cycle; standard load; differential operation
11. For 3.3V supplies. Jitter measured differentially using an Agilent 8133A Pulse Generator with an 8500A LeCroy Wavemaster Oscilloscope using at least 10,000 data points
12. Output pulse skew is the absolute difference of the propagation delay times:  $|t_{PLH} - t_{PHL}|$ .

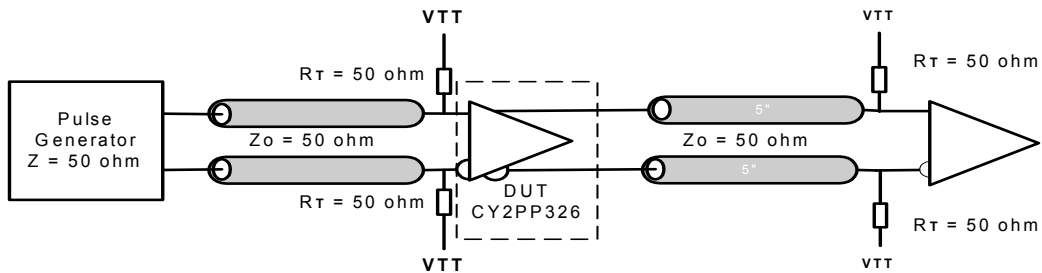
**Timing Definitions**

**Figure 2. PECL/ECL Input Waveform Definitions**

**Figure 3. ECL/LVPECL Output**

**Figure 4. Propagation Delay ( $T_{PD}$ ), output pulse skew ( $|t_{PLH} - t_{PHL}|$ ), and output-to-output skew ( $t_{SK(O)}$ ) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL**



**Figure 5. Output Disable/Enable Timing**

### Test Configuration

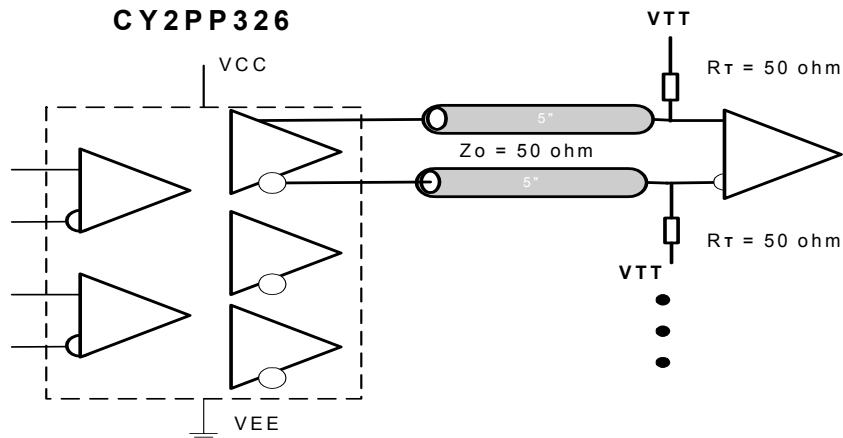
Standard test load using a differential pulse generator and differential measurement instrument.



**Figure 6. CY2PP326 AC Test Reference**

### Applications Information

#### Termination Examples



**Figure 7. Standard LVPECL – PECL Output Termination**

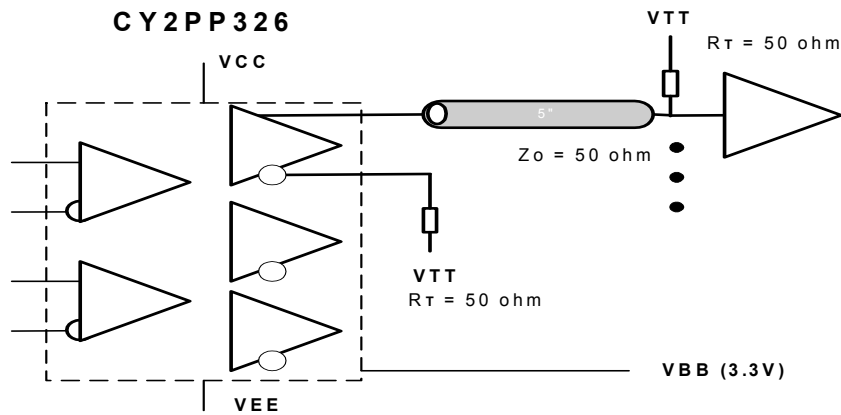


Figure 8. Driving a PECL/ECL Single-ended Input

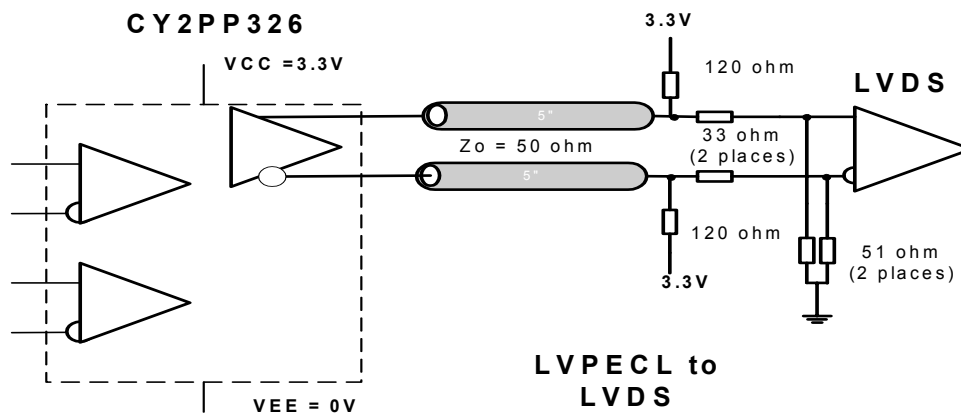
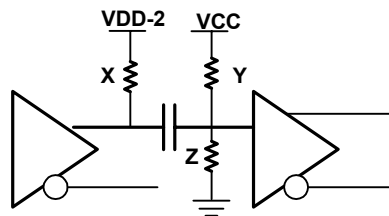


Figure 9. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface

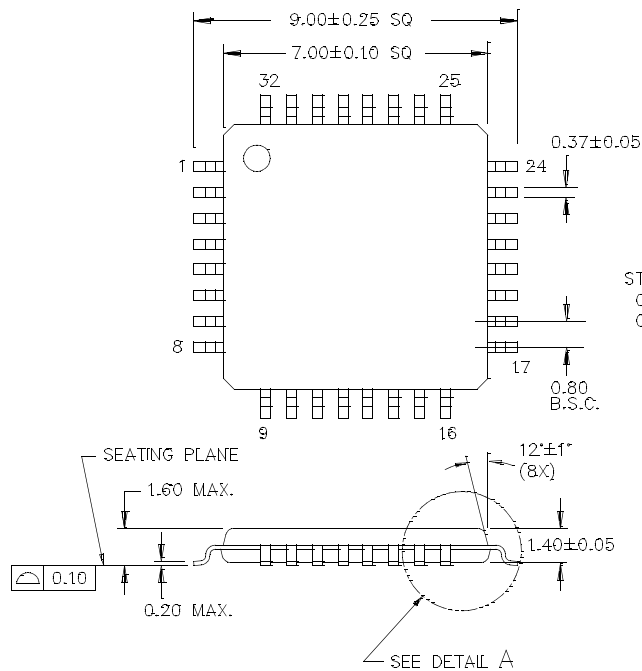
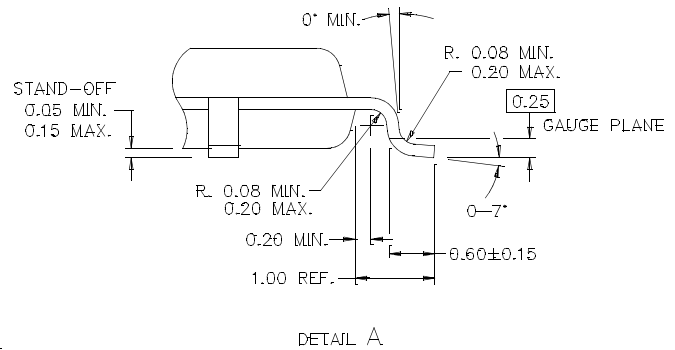


One output is shown for clarity

Figure 10. Termination for LVPECL to HTSL interface for VCC=2.5V would use X=50 Ohms, Y=2300 Ohms, and Z=1000 Ohms. See application note titled, "PECL Translation, SAW Oscillators, and Specs" for other signalling standards and supplies.

### Ordering Information

Part Number	Package Type	Product Flow
CY2PP326AI	32-pin TQFP	Industrial, -40° to 85°C
CY2PP326AIT	32-pin TQFP – Tape and Reel	Industrial, -40° to 85°C

**Package Drawing and Dimensions**
**32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14**

**Dimensions in mm.**


51-85088-B

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Document History Page

Document Title: CY2PP326 FastEdge™ Series 2 x 2 Clock and Data Switch Buffer				
Document Number: 38-07506				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	122361	02/12/03	RGL	New Data Sheet
*A	129269	09/09/03	RGL	Changed ComLink™ to FastEdge™ Added $t_{PLDg}$ and $t_{PDLf}$ specs in the AC specs table Added the Output disable/enabling timing diagram Deleted the output reference voltage in the absolute max. conditions Fixed the AC/DC Electrical specs to match the EROS
*B	131346	11/20/03	RGL	Posted to external web
*C	237751	See ECN	RGL	Supplied data to all TBD's to match the device.
*D	247620	See ECN	RGL/GGK	Changed $V_{OH}$ and $V_{OL}$ to match the Char Data