CY62148EV30LL Automotive

4-Mbit (512 K × 8) Static RAM

Features

- Very high speed: 55 ns
  - Wide voltage range: 2.20 V to 3.60 V
- Temperature range:
  - Automotive-E: –40 °C to +125 °C
- Pin compatible with CY62148DV30
- Ultra low standby power
  - Typical standby current: 3 μA
  - Maximum standby current: 20 μA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free, 32-pin thin small outline package (TSOP II).

Functional Description

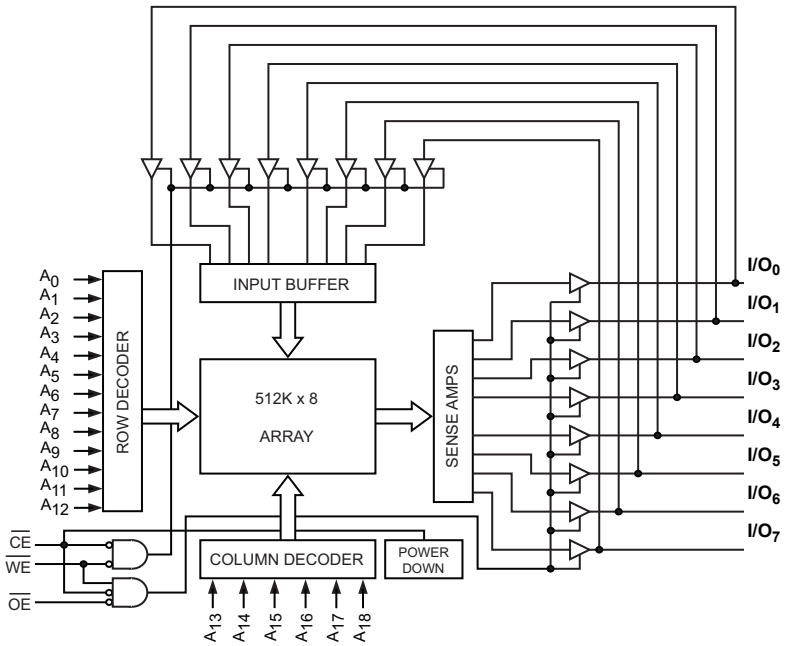
The CY62148EV30LL Automotive is a high performance CMOS static RAM organized as 512 K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, click here.

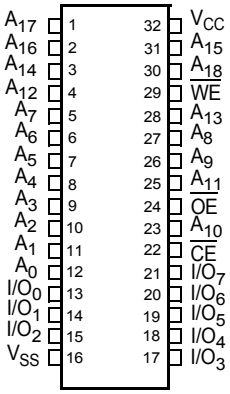
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 32-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product		Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
							Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
							f = 1 MHz		f = f_{max}			
			Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62148EV30LL	TSOP II	Automotive-E	2.2	3.0	3.6	55	2	3	15	30	3	20

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z State [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current .....> 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}[5]
CY62148EV30LL Automotive	Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		–55			Unit
				Min	Typ [6]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input low voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}		–5	–	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–5	–	+5	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	15	30	mA
		f = 1 MHz		–	2	3	
I_{SB1} [7]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	3	20	µA
I_{SB2} [7]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	3	20	µA

Notes

3. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

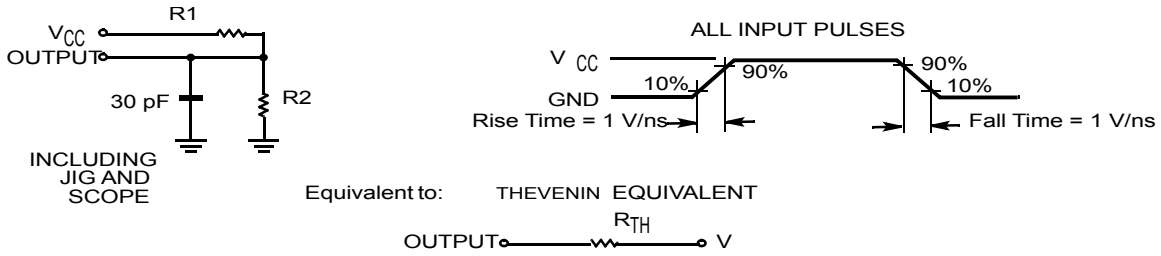
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	TSOP II Package	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	79.03	°C/W
θ_{JC}	Thermal resistance (junction to case)		17.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

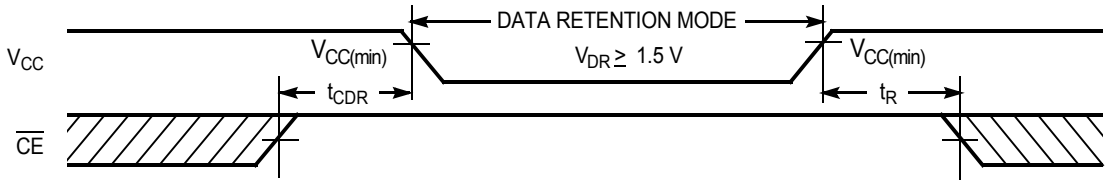
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Automotive-E	–	3	20	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[12]	Operation recovery time			55	–	–	–

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip Enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.

Switching Characteristics

Over the Operating Range

Parameter [13]	Description	-55		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [14]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [14, 15]	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [14]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [14, 15]	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power up	–	55	ns
Write Cycle [16]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [14, 15]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [14]	10	–	ns

Notes

13. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [17, 18]

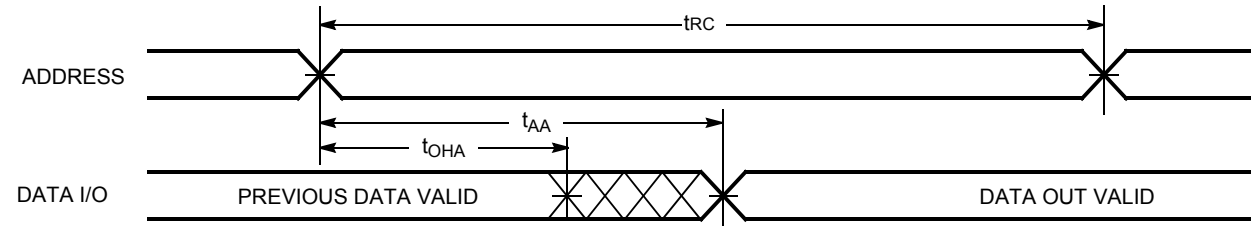
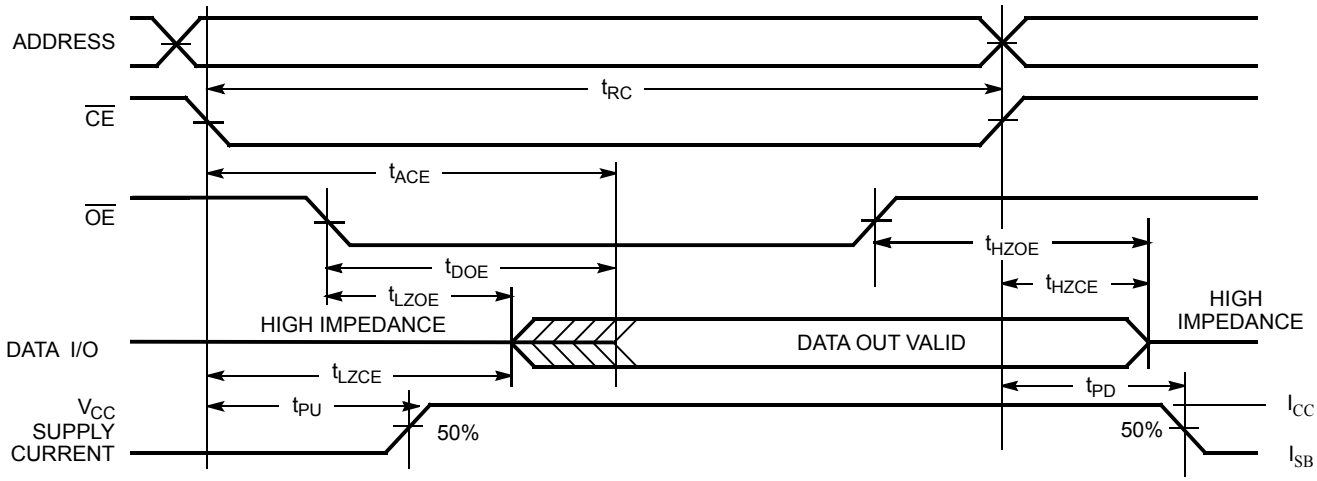


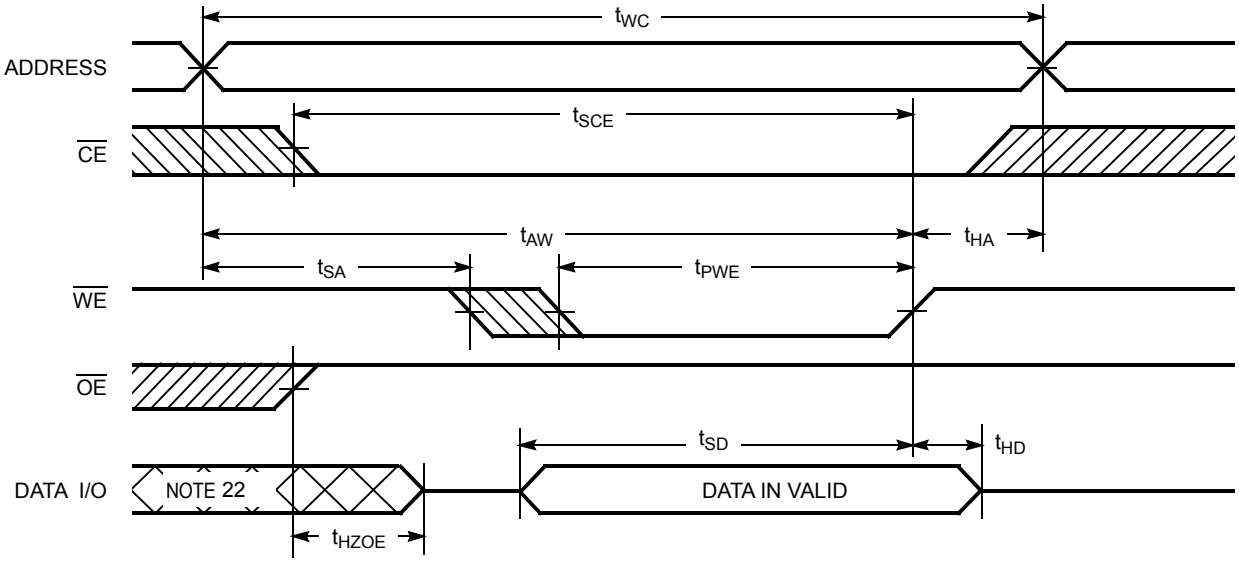
Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19]



Notes
17. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
18. $\overline{WE}$ is HIGH for read cycles.
19. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [20, 21]



Notes
20. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
22. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23, 24]

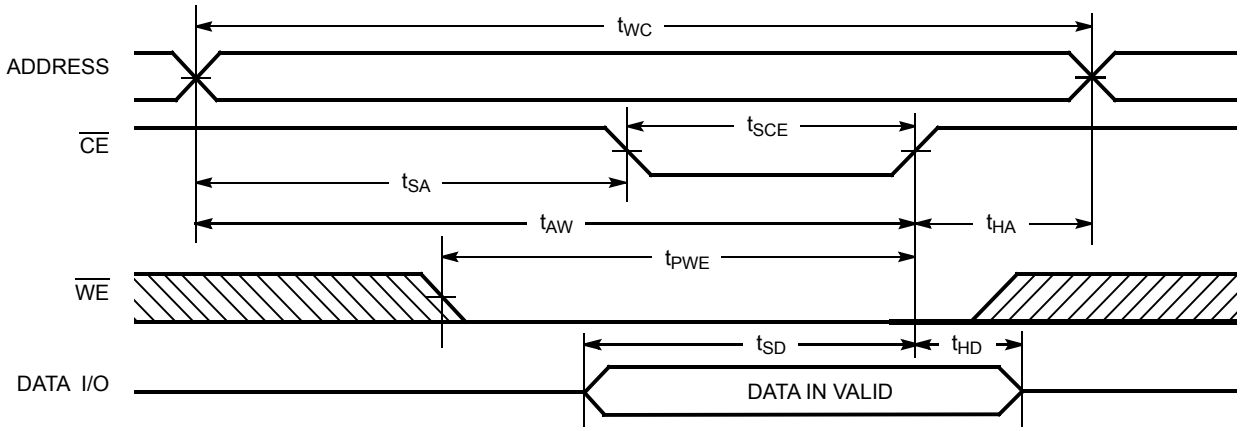
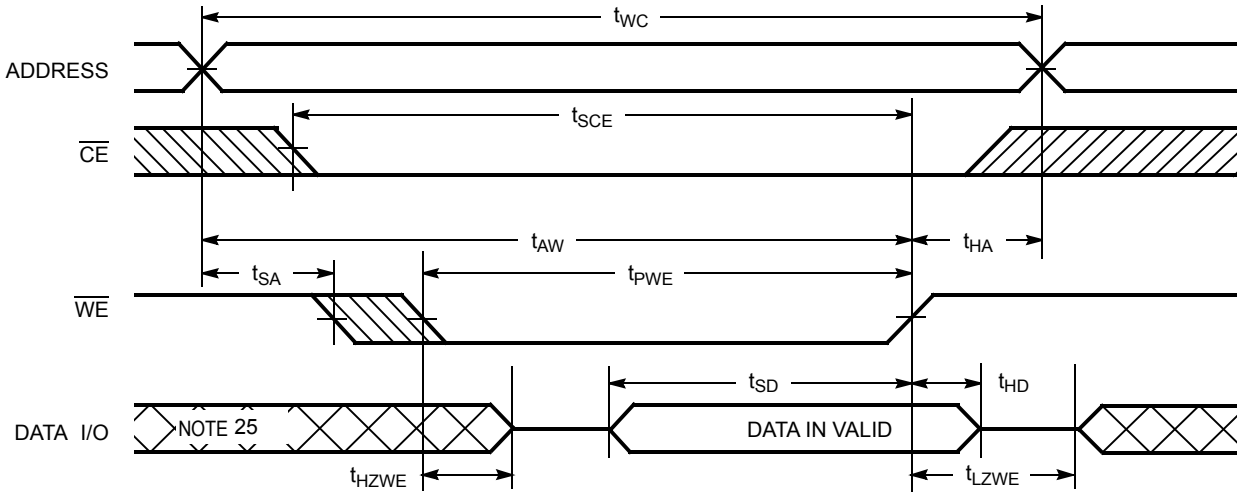


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [24]



Notes

23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$ [26]	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

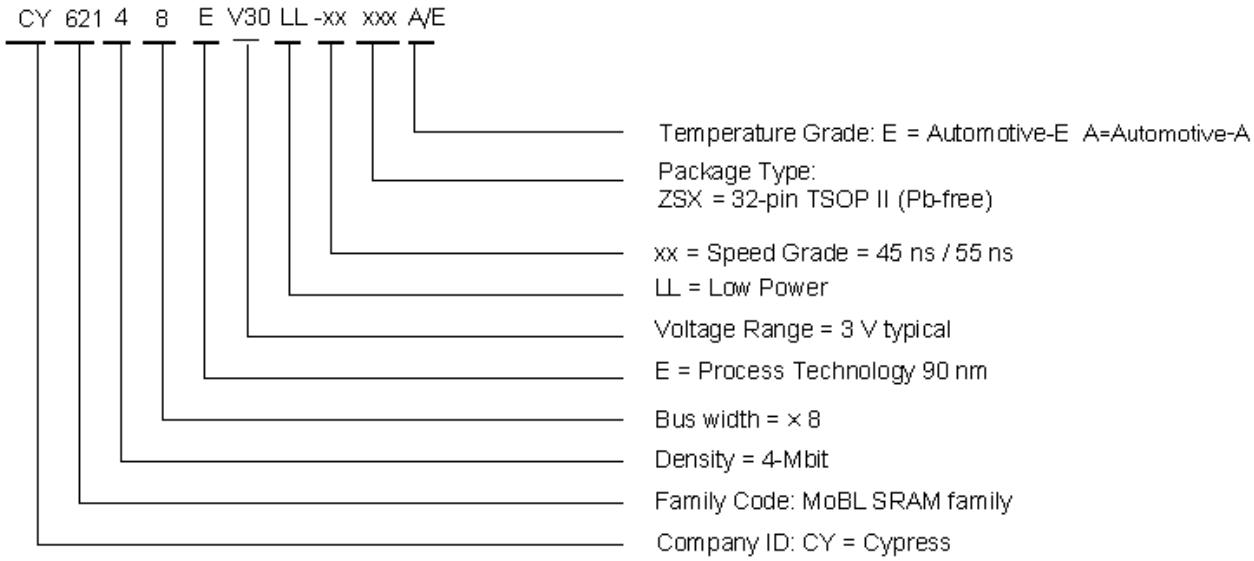
Notes
26. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148EV30LL-55ZSXE	51-85095	32-pin TSOP II	Automotive-E

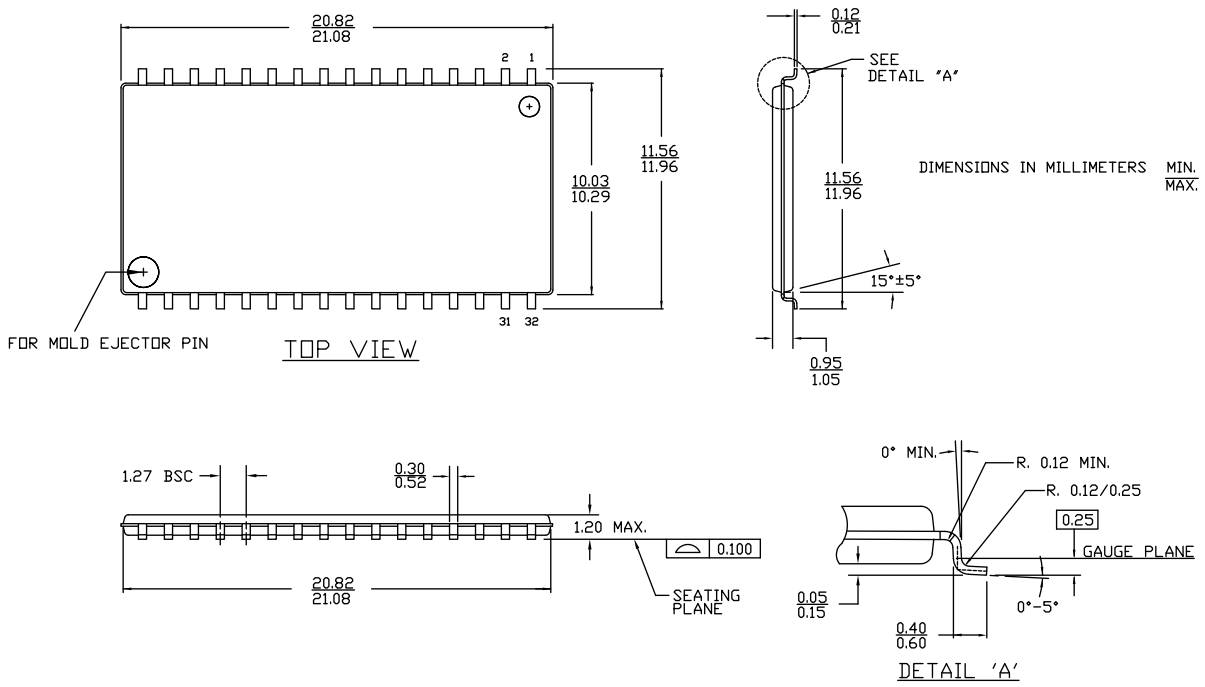
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) Package Outline, 51-85095



51-85095 *D

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148EV30LL Automotive, 4-Mbit (512 K × 8) Static RAM Document Number: 001-73042				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3406557	TAVA	10/03/2012	New data sheet
*A	4321736	MEMJ	03/26/2014	Updated Ordering Information: No change in part numbers. Replaced “51-85081” with “51-85095” in Package Diagram column. Updated to new template.
*B	4573200	MEMJ	11/18/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*C	4790712	NILE	06/08/2015	Updated Package Diagrams: spec 51-85095 – Changed revision from *B to *D. Updated to new template.
*D	4983120	NILE	10/26/2015	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Changed value of θ_{JA} parameter corresponding to “TSOP II Package” from 75.13 °C/W to 79.03 °C/W. Changed value of θ_{JC} parameter corresponding to “TSOP II Package” from 8.95 °C/W to 17.44 °C/W. Completing Sunset Review.
*E	6013872	AESATP12	01/04/2018	Updated logo and copyright.

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