



# High-Speed CMOS Synchronous Presettable 4-Bit Binary Counters

QS54/74FCT161T  
QS54/74FCT163T

QS54/74FCT2161T  
QS54/74FCT2163T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F161/3 74FCT 161/3 and 74FCT161T/3T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 161T, 163T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std through D speed grades with 5.0 ns tPD for D
- Iol = 48 mA Com., 32 mA Mil.

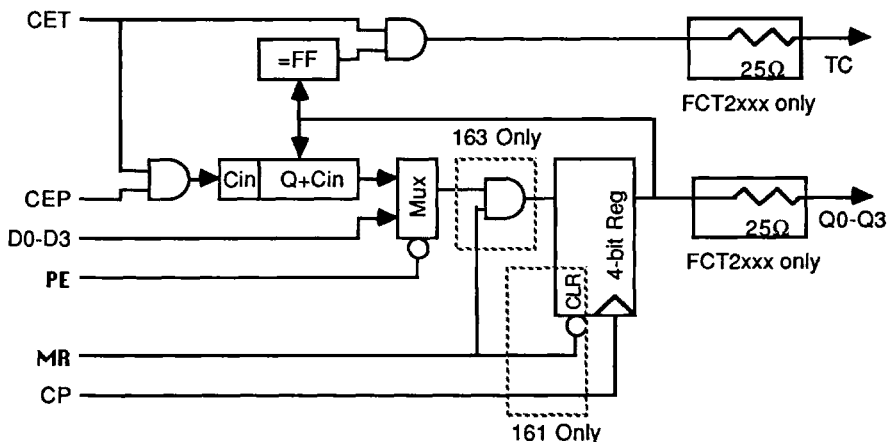
### FCT-T 2161T, 2163T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A & C speed grades with 5.6 ns tPD for C
- Iol = 12mA Com.

## DESCRIPTION

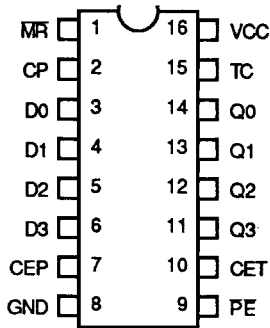
The QSFC161T and QSFC163T are high speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. The 2161 and 2163 are 25Ω resistor output versions of the 161 and 163, respectively, and are useful for driving transmission lines and reducing system noise. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM

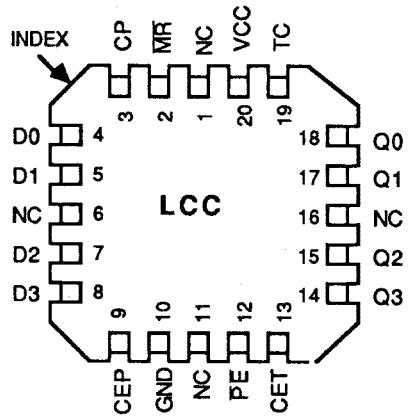
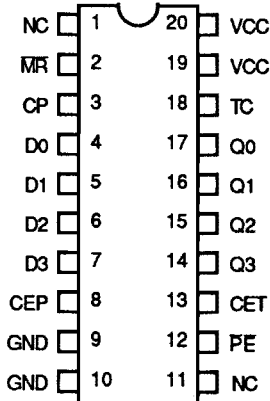


**PIN CONFIGURATIONS**

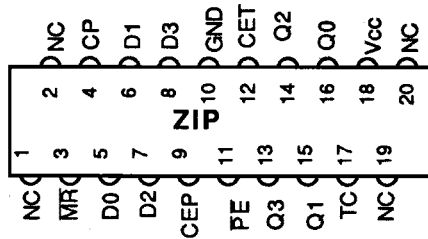
**PDIP, SOIC, QSOP**



**HQSOP**



**ALL PINS TOP**



Note: Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

**PIN DESCRIPTION**

Name	I/O	Description
D0-3	I	Data Inputs
Q0-3	O	Data Outputs
CP	I	Clock
MR	I	Master Reset

Name	I/O	Description
CEP	I	Count Enable
CET	I	Count and TC Enable
TC	O	Terminal Count
PE	I	Parallel Load Enable

**FUNCTION TABLE**

Inputs						Outputs			Function
MR	PE	CP	CEP	CET	Di	Q0-3		TC	
						161	163		
L	X	X	X	X	X	L	-	L	Clear 161
L	X	↑	X	X	X	-	L	L	Clear 163
H	L	↑	X	X	D0-3	D0-3	D0-3	X	Load Data
H	H	↑	H	H	X	Q+1	Q+1	X	Count
H	H	↑	L	X	X	Q	Q	X	Count Inhibit P
H	H	↑	X	L	X	Q	Q	X	Count Inhibit T
H	H	X	X	H	X	F	F	H	Count = 1111
H	H	X	X	H	X	0-E	0-E	L	Count ≠ 1111
H	H	X	X	L	X	X	X	L	TC Inhibit

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**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground..... -0.5V to +7.0V  
 DC Output Voltage  $V_O$  ..... -0.5V to 7.0V  
 DC Input Voltage  $V_I$  ..... -0.5V to 7.0V  
 AC Input Voltage (for a pulse width  $\leq 20$  ns)..... -3.0V  
 DC Input Diode Current with  $V_I < 0$ ..... -20 mA  
 DC Output Diode Current with  $V_O < 0$ ..... -50 mA  
 DC Output Current Max. sink current/pin..... 120 mA  
 Maximum Power Dissipation..... 0.5 watts  
 $T_{STG}$  Storage Temperature..... -65° to +165°C

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{in} = 0\text{V}$ ,  $V_{out} = 0\text{V}$

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1-7,9,10	4	4	5	7	pF
11-15	6	6	7	9	pF
-----	8	8	9	10	pF

Note: Capacitance is characterized but not tested

**QSFCT161T, 2161T, 163T, 2163T**

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$

Military  $T_A=-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
$\Delta V_t$	Input Hysteresis	$V_{th} - V_{tl}$ for All Inputs		-	0.2	-	
$i_{ih}$     $i_{il}$	Input Current Input HIGH or LOW	$V_{CC} = \text{MAX}$	$0 \leq V_{in} < V_{CC}$	-	-	5	$\mu\text{A}$
$i_{oz}$	Off State Output Current (Hi-Z)	$V_{CC} = \text{MAX}, 0 \leq V_{in} \leq V_{CC}$		-	-	5	
Ios	Short Circuit Current FCTXXX	$V_{CC} = \text{MAX}, V_o = \text{GND} (2,3)$		-60	-	-225	mA
Ior	Current Drive FCT2XXX	$V_{CC} = \text{Min}, V_o = 2.0\text{V} (3)$		50	-	-	mA
Vic	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{in} = 18 \text{ mA} (3)$		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	$V_{CC} = \text{MIN}$	$I_{oh} = 12 \text{ mA (MIL)}$	2.4	-	-	Volts
			$I_{oh} = 15 \text{ mA (COM)}$	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	$V_{CC} = \text{MIN}$	$I_{ol} = 32 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 48 \text{ mA (COM)}$	-	-	0.50	
	Output LOW Voltage FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	-	-	0.50	
			$I_{ol} = 12 \text{ mA (COM)}$	-	-	0.50	
Rout	Output Resistance FCT2XXX (25 $\Omega$ )	$V_{CC} = \text{MIN}$	$I_{ol} = 12 \text{ mA (MIL)}$	-	25	-	$\Omega$
			$I_{ol} = 12 \text{ mA (COM)}$	20	28	40	

**Notes:**

1. Typical values indicate  $V_{CC}=5.0\text{V}$  and  $T_A=25^{\circ}\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = MAX, freq = 0 0V ≤ V <sub>in</sub> ≤ 0.2V or V <sub>cc</sub> - 0.2V ≤ V <sub>in</sub> ≤ V <sub>cc</sub>	-	1.5	mA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = MAX, V <sub>in</sub> = 3.4 V, freq = 0 (2)	-	2.0	
Q <sub>ccd</sub>	Supply Current per input per mHz	V <sub>cc</sub> = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V <sub>cc</sub> (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>i</sub>=3.4V)
3. For flipflops Q<sub>ccd</sub> is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I<sub>c</sub> can be computed using the above parameters as explained in the Technical Overview section.

**QSFACT161T, 2161T, 163T, 2163T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%    Military TA = -55°C to 125° C, Vcc = 5.0V±10%  
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes (1)	161 163 2161 2163		161A 163A 2161A 2163A		161C 163C 2161C 2163C		161D 163D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
† CPQ	Propagation Delay CP to Qi, 161/3	COM	2	9.5	2	6.2	2	5.6	1.5	5.0	ns
		MIL	2	10	2	6.5	2	6.1			
	Propagation Delay CP to Qi, 2161/3	COM	2	9.5	2	6.2	2	5.6			
		MIL	2	10	2	6.5	2	6.1			
† MRQ	Propagation Delay MR to Qi, 161	COM	2	13	2	8.5	2	7.8	1.5	6.5	
		MIL	2	14	2	9.1	2	8.3			
	Propagation Delay MR to Qi, 2161	COM	2	14	2	9.1	2	7.8			
		MIL	2	13	2	8.5	2	8.3			
† CPTC	Propagation Delay CP to TC	COM	2	15	2	9.8	2	8.8	1.5	7.5	
		MIL	2	16.5	2	10.8	2	9.8			
† CETC	Propagation Delay CET to TC	COM	1.5	8.5	1.5	5.5	1.5	5.0	1.5	4.2	
		MIL	1.5	9	1.5	5.9	1.5	5.4			
† MRTC	Propagation Delay MR to TC	COM	1.5	11.5	1.5	7.5	1.5	6.8	1.5	6.2	
		MIL	1.5	12.5	1.5	8.2	1.5	7.4			

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**Notes:**

- 1) Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) See Test Circuit and Waveforms.

## QSFACT161T, 2161T, 163T, 2163T

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%    Military TA = -55°C to 125° C, Vcc = 5.0V±10%  
 Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	161 163 2161 2163		161A 163A 2161A 2163A		161C 163C		Unit
			Min	Max	Min	Max	Min	Max	
t DS	Data Setup Time Di to CP	COM	5		4		3.5		ns
		MIL	5.5		4.5		4.0		
t DH	Data Hold Time Di to CP	COM	1.5		1.5		1.5		
		MIL	2		2		2		
t CS	Count Enab. Setup Time CEP, CET to CP	COM	11.5		9.5		8.5		
		MIL	13		11		10		
t CH	Count Enable Hold Time CEP, CET to CP	COM	0		0		0		
		MIL	0		0		0		
t MRS t PES	Control Setup Time MR, PE to CP	COM	11.5		9.5		8.5		
		MIL	13.5		11.5		10.5		
t MRH t PEH	Control Hold Time MR, PE to CP	COM	1.5		1.5		1.5		
		MIL	1.5		1.5		1.5		
t CPW	Clock Pulse Width HIGH or LOW	COM	2	5	4		3		
		MIL	2	5	4		3		
t MRW	MR Reset Pulse Width 161, 2161	COM	2	5	4		3		
		MIL	2	5	4		3		
t MRW	Reset Recovery Time MR to CP, 161, 2161	COM	2	6	5		4		
		MIL	2	6	5		4		

**Notes:**

- 1) Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) See Test Circuit and Waveforms.