

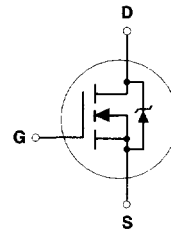
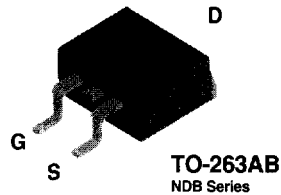
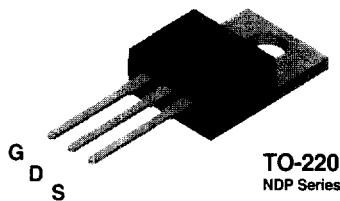
## NDP4050 / NDB4050 N-Channel Enhancement Mode Field Effect Transistor

### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 15A, 50V.  $R_{DS(ON)} = 0.10\Omega$  @  $V_{GS}=10V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	NDP4050	NDB4050	Units
$V_{DSS}$	Drain-Source Voltage		50	V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1\text{ M}\Omega$ )		50	V
$V_{GSS}$	Gate-Source Voltage - Continuous		$\pm 20$	V
	- Nonrepetitive ( $t_p < 50\ \mu\text{s}$ )		$\pm 40$	
$I_D$	Drain Current - Continuous		$\pm 15$	A
	- Pulsed		$\pm 45$	
$P_D$	Total Power Dissipation		50	W
	Derate above 25°C		0.33	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-65 to 175	°C
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		275	°C

Electrical Characteristics (T <sub>c</sub> = 25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE AVALANCHE RATINGS</b> (Note 1)						
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	V <sub>DD</sub> = 25 V, I <sub>D</sub> = 15 A			40	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current				15	A
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	50			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V			250	μA
		T <sub>J</sub> = 125°C			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
<b>ON CHARACTERISTICS</b> (Note 1)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
		T <sub>J</sub> = 125°C	1.4	2.4	3.6	
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A		0.078	0.1	Ω
		T <sub>J</sub> = 125°C		0.12	0.165	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V	15			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.5 A	3	5.7		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		370	450	pF
C <sub>oss</sub>	Output Capacitance			165	200	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50	100	pF
<b>SWITCHING CHARACTERISTICS</b> (Note 1)						
t <sub>D(on)</sub>	Turn - On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 15 A		8	20	ns
t <sub>r</sub>	Turn - On Rise Time	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 25 Ω		70	100	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			18	30	ns
t <sub>f</sub>	Turn - Off Fall Time			37	50	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 48 V		12.7	17	nC
Q <sub>gs</sub>	Gate-Source Charge	I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V		3.2		nC
Q <sub>gd</sub>	Gate-Drain Charge			7		nC

Electrical Characteristics ( $T_c = 25^\circ\text{C}$ unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				15	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				45	A	
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7.5\text{ A}$ (Note 1)			0.95	1.3	V
				$T_J = 125^\circ\text{C}$	0.88	1.2	
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 15\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	25	46	100	ns	
$I_{rr}$	Reverse Recovery Current		1.5	3.4	7	A	
<b>THERMAL CHARACTERISTICS</b>							
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	$^\circ\text{C}/\text{W}$	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	$^\circ\text{C}/\text{W}$	
Note: 1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$ , Duty Cycle $\leq 2.0\%$ .							

Typical Electrical Characteristics

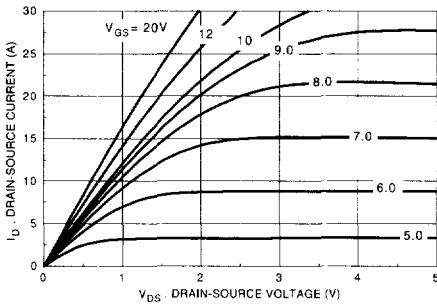


Figure 1. On-Region Characteristics.

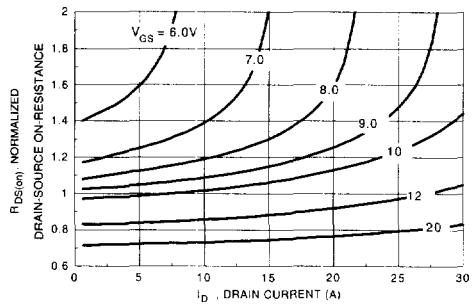


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

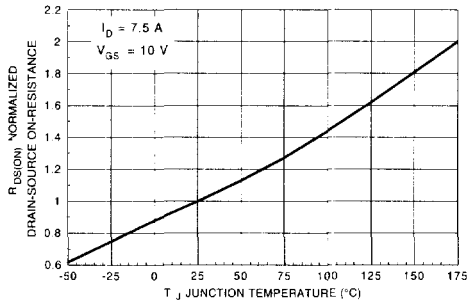


Figure 3. On-Resistance Variation with Temperature.

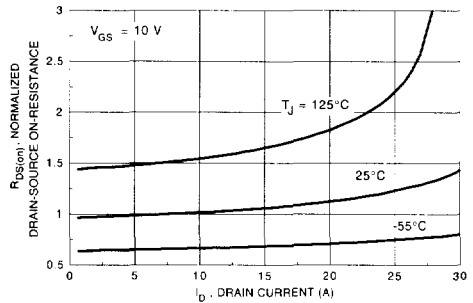


Figure 4. On-Resistance Variation with Drain Current and Temperature.

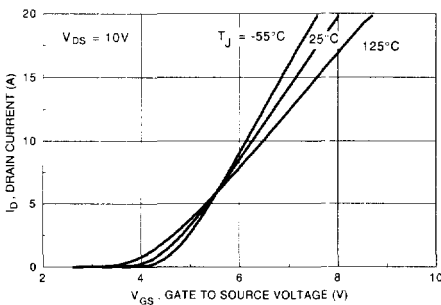


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

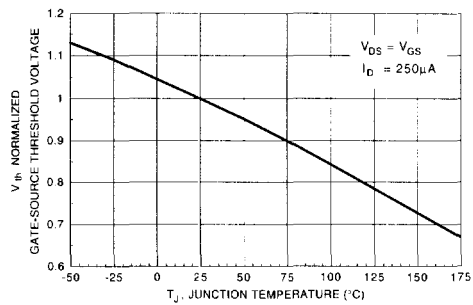
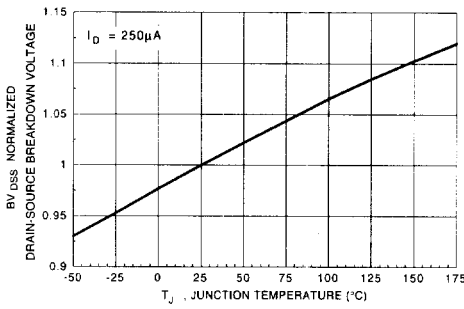


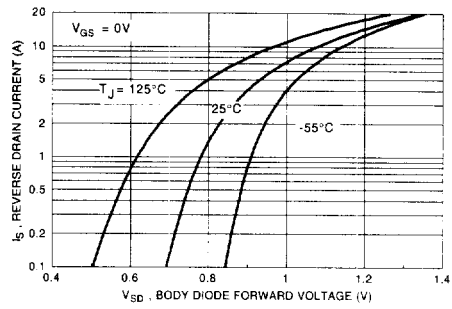
Figure 6. Gate Threshold Variation with Temperature.

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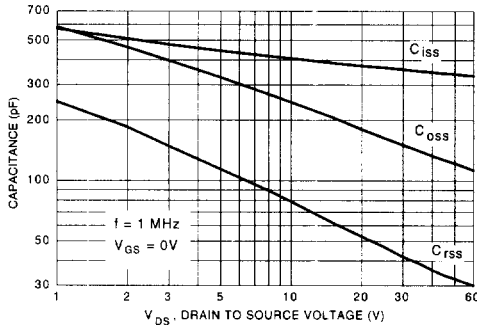
**Typical Electrical Characteristics (continued)**



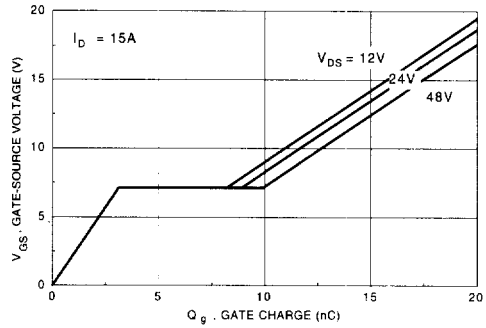
**Figure 7. Breakdown Voltage Variation with Temperature.**



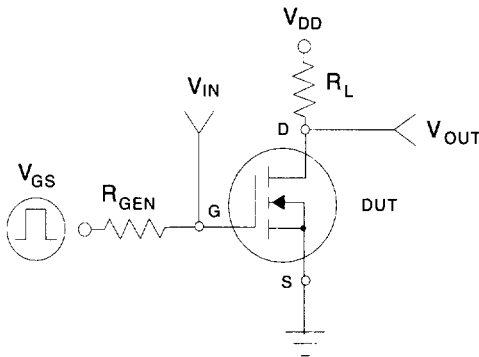
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



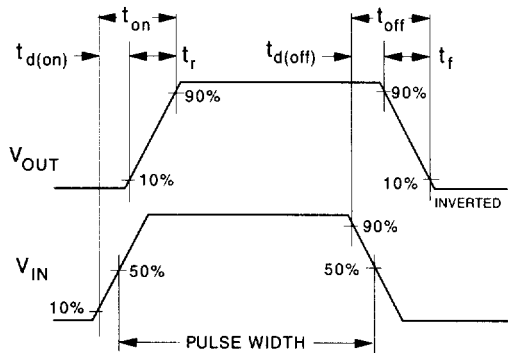
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**



**Figure 11. Switching Test Circuit.**



**Figure 12. Switching Waveforms.**

Typical Electrical Characteristics (continued)

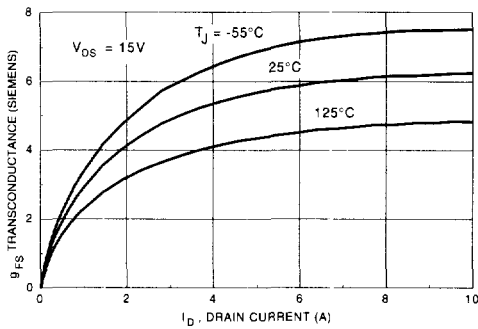


Figure 13. Transconductance Variation with Drain Current and Temperature.

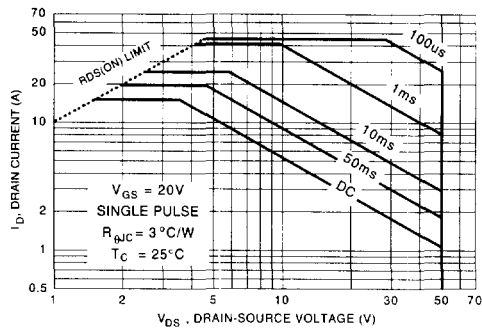


Figure 14. Maximum Safe Operating Area.

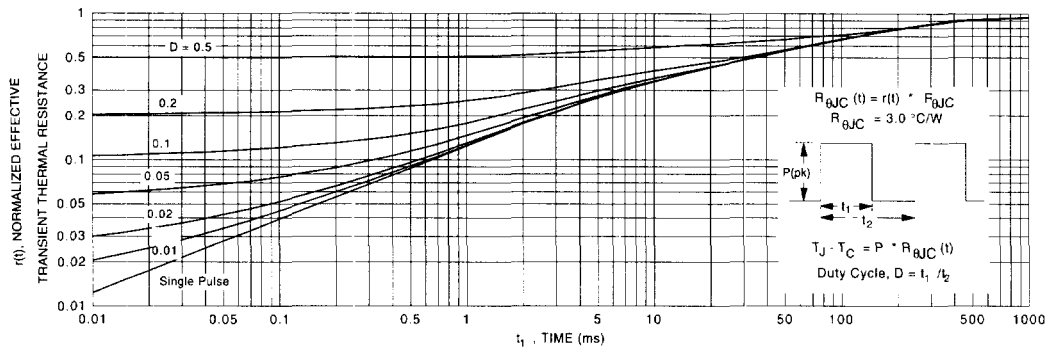


Figure 15. Transient Thermal Response Curve.