CY27022

Clock Generator for Net-MD System

Features

- Supports Clock Requirement for Mini Disc
- 16.9344 MHz Crystal or Clock Input
- 12.000 MHz for USB Clock Output
- 10.0352 MHz for Controller Clock Output
- 90.3168 MHz/180.6336 MHz Selectable Clock Output
- Load Capacitance for Crystal (Cl = 12.1 pF Typ)
- 3.3V Operation
- 8-pin SOIC Package

Description

The CY27022 is a clock generator that integrates clock requirements for a Net-MD system.

The CY27022 supports USB clock, Mini Disc, and CPU clock requirements.

Table 1. Frequency Table (Input = 16.9344 MHz)

Pin Number	Name	Output Frequency	FS
1	CLKC	12.000 MHz	x
5	CLKB	90.3168 MHz	0
5	CLKB	180.6336 MHz	1
6	CLKA	10.0352 MHz	x

Pinout

Figure 1. Pin Diagram - 8-Pin SOIC

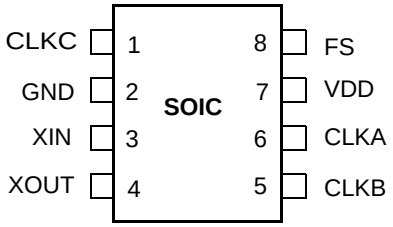


Table 2. Pin Definition - 8 SOIC

Pin Number	Pin Name	I/O	Description
1	CLKC	O	12.000 MHz clock output
2	GND	PWR	Device Ground
3	XIN	I	16.9344 MHz reference crystal or external clock input
4	XOUT	O	Reference crystal feedback (float if XIN is driven by external reference clock)
5	CLKB	O	Selectable clock output, see Table 1.
6	CLKA	O	10.0352 MHz clock output
7	VDD	PWR	+3.3V power supply
8	FS	I	Frequency selection input pin. This pin controls the frequency presented on CLKB. Internal pull up

Maximum Ratings

The voltage on any input or I/O pin cannot exceed the power pin during power up. These user guidelines are not tested.

Maximum Input Voltage Relative to GND: .....–0.3V

Maximum Input Voltage Relative to V_{DD}:.....V_{DD} + 0.3V

Storage Temperature: ..... –65° to +150°C

Operating Temperature:.....0°C to +70°C

Maximum ESD Protection 2KV

Maximum Power Supply:.....5.5V

Operating Voltage: 2.9V–3.6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, precautions are taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} are constrained to the range:

$GND < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs are always to an appropriate logic voltage level (either GND or V_{DD}).

DC Parameters

Table 3. DC Parameters[2] (V_{DD} = 3.3V ±10%, T_A = 0 to 70°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage	See Note 1			0.8	V
V_{IH}	Input high voltage	See Note 1	2.0			V
I_{IL}	Input low current	See Note 1	–72		-15	µA
IIH	Input high current	See Note 1			10	µA
Idd3.3V	Dynamic supply current	No output load, FS = 1 (180-MHz mode)		19	28	mA
V_{OL}	Output low voltage	I_{OL}= 4.0 mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = –4.0 mA	2.4			V
C_{XTAL}	Crystal pin capacitance	XIN, XOUT pin capacitance		23		pF

AC Parameters

Table 4. AC Parameters[3]

Parameter	Description	Comments	Min	Typ	Max	Unit
Tr1	Rise time	CLKA and CLKC at rated load[4, 5, 6, 7]		2	3	ns
Tf1	Fall time	CLKA and CLKC at rated load[4, 5, 6, 7]		2	3	ns
Tr2	Rise time	CLKB at rated load[4, 5, 6, 7]			1.5	ns
Tf2	Fall time	CLKB at rated load[4, 5, 6, 7]			1.5	ns
Tpu	Power up to stable output	All output clocks[5]			3	ms
Tdc	Clock duty cycle	All clocks at rated load[6, 7]	45	50	55	%
Tj1	Clock jitter	CLKA and CLKC at rated load[4, 5, 6, 7]			250	ps
Tj2	Clock jitter	CLKB at rated load[4, 5, 6, 7]			150	ps

Notes

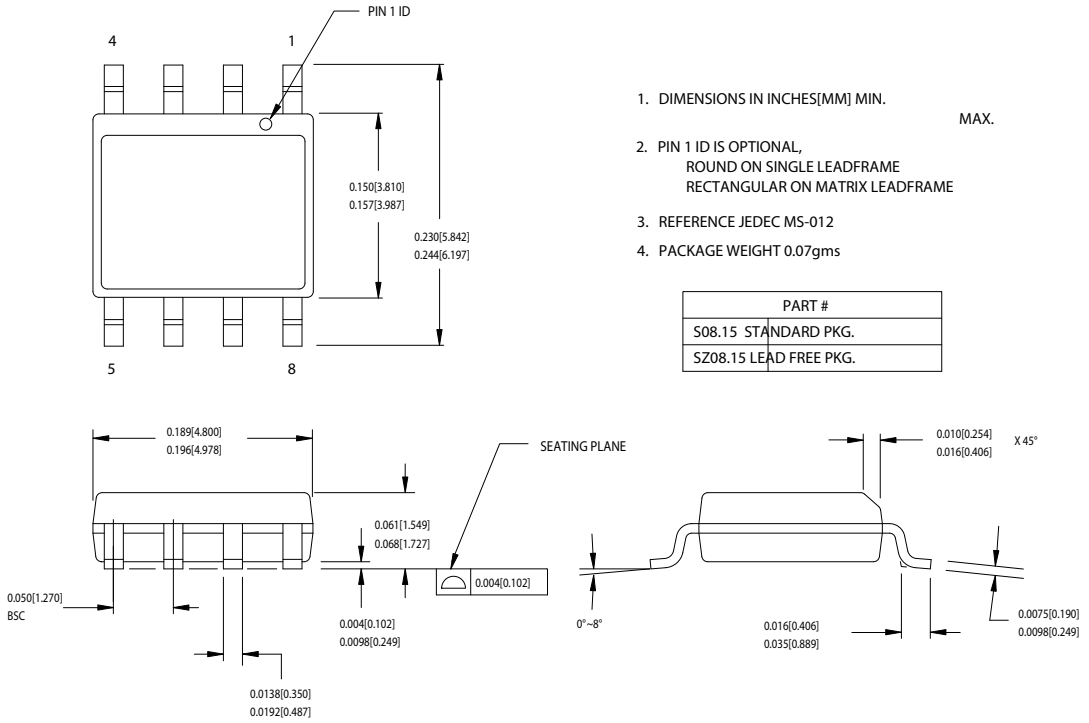
1. Applicable to input signal: FS. Internal pull up resistor value may vary between 70k and 170k.
2. The voltage on any input or IO pin cannot exceed the power pin during power up.
3. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs
4. Measured between 0.2*V_{DD} and 0.8*V_{DD} Volts.
5. Measured between 0.2*V_{DD} and 0.7*V_{DD} Volts.
6. Clocks trigger at 1.5 Volts.
7. All outputs have a 15 pF load.

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY27022SCT	8-pin SOIC - Tape and Reel	Commercial (0 to 70°C)	3.3V±10%
CY27022SXC	8-pin SOIC (Pb-free)	Commercial (0 to 70°C)	3.3V±10%
CY27022SXCT	8-pin SOIC (Pb-free) - Tape and Reel	Commercial (0 to 70°C)	3.3V±10%

Package Drawing and Dimensions

Figure 2. 8-Pin (150-Mil) SOIC



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Document History

Document Title: CY27022 Clock Generator for Net-MD System Document Number: 38-07293				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	116146	08/14/02	OSM	New Data Sheet
*A	122884	12/22/02	RBI	Added power up requirements to Maximum Ratings
*B	406494	See ECN	XHT/CFT	Obsolete specification. Sunset Review Clean up. Personalized clock chips for Japanese customer and no longer in use.
*C	1191263	See ECN	KVM	Revived the data sheet as the device is still active. Added Pb-free part numbers. Updated note 2 to remove mention of multiple supplies and voltage sequencing. Replaced instances of VSS with GND.
*D	2710266	05/22/09	KVM/PYRS	Remove obsolete part number from Ordering Information table: CY27022SC
*E	2748211	08/10/09	TSAI	Posting to external web.

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