Rochester Electronics

Datasheet

PART NUMBER

74174J-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

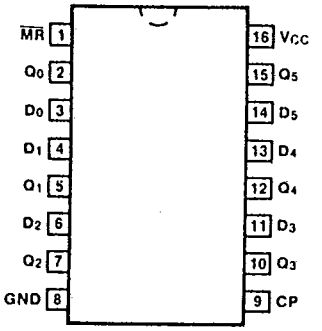
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54/74174
54S/74S174
54LS/74LS174
HEX D FLIP-FLOP

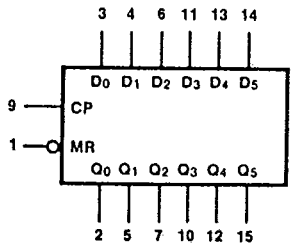
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '174 is a high speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74174PC, 74S174PC, 74LS174PC		9B
Ceramic DIP (D)	A	74174DC, 74S174DC, 74LS174DC	54174DM, 54S174DM, 54LS174DM	6B
Flatpak (F)	A	74174FC, 74S174FC, 74LS174FC	54174FM, 54S174FM, 54LS174FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_0 - D_5$	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_5$	Flip-Flop Outputs	20/10	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The '174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ t_{n+1}
D_n	Q_n
H	H
L	L

t_n = Bit time before positive-going clock transition
t_{n+1} = Bit time after positive-going clock transition
H = HIGH Voltage Level
L = LOW Voltage Level

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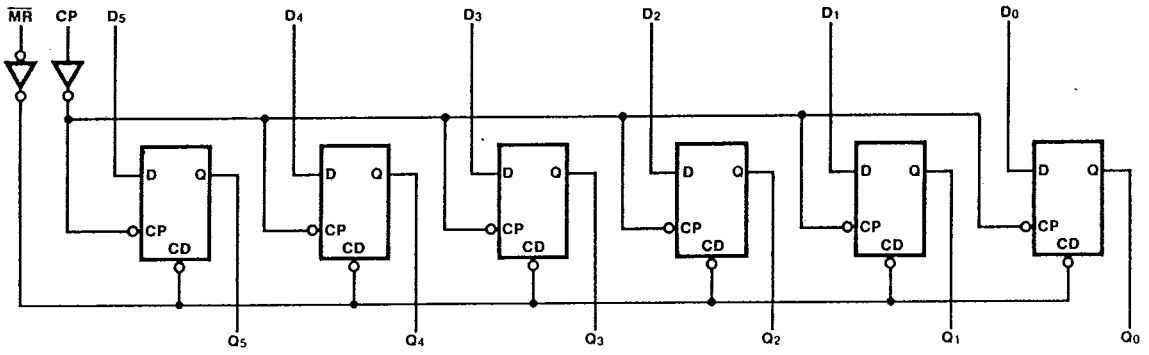
LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		65		144		26	mA	V_{CC} = Max D_n = $\overline{MR}$ = 4.5 V CP = ⎍⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		30 35		12 17		25 22	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35		22		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		5.0 5.0		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		3.0 3.0		5.0 5.0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		18		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		7.0		18		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		12		ns	