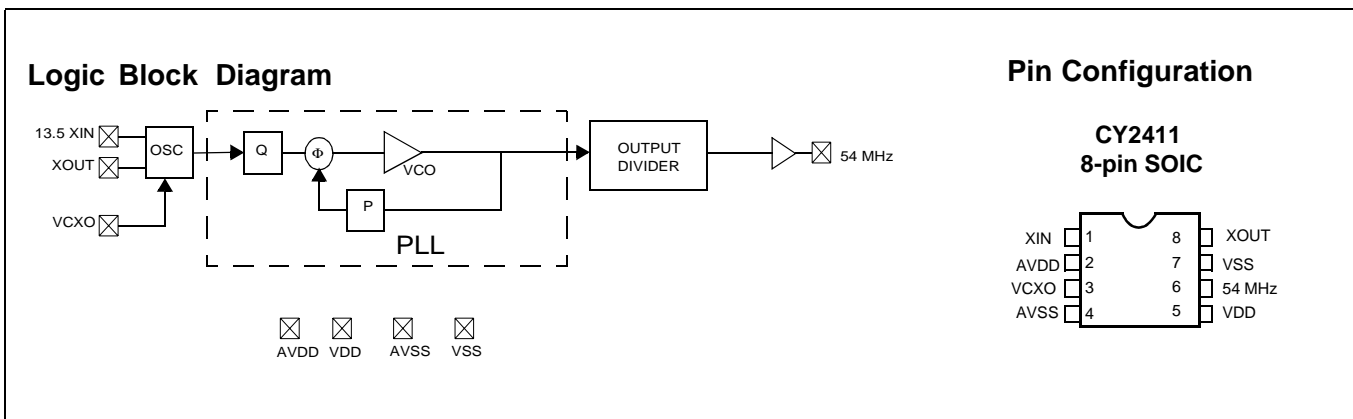




# MediaClock™ MPEG Clock Generator with VCXO

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large $\pm 150$ ppm range, better linearity
• 3.3V operation	

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY2411-1	1	13.5-MHz Pullable Crystal per Cypress Specification	1 copy of 54 MHz (3.3V)



### Pin Summary

Pin Name	Pin Number	Pin Description
$A_{VDD}$	2	Analog Voltage Supply
$V_{DD}$	5	Output Voltage Supply
$A_{VSS}$	4	Analog Ground
$V_{SS}$	7	Output Ground
$X_{IN}$	1	Reference Crystal Input
$V_{CXO}$	3	Analog Control for $V_{CXO}$
$X_{OUT}^{[1]}$	8	Reference Crystal Output
54 MHz	6	54-MHz clock output

**Note:**

1. Float  $X_{OUT}$  if  $X_{IN}$  is externally driven.

**Absolute Maximum Conditions**

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[2]</sup>	-65	125	°C
T <sub>J</sub>	Junction Temperature		125	°C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs Referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electro-Static Discharge	2000		V

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating Voltage	3.15	3.3	3.45	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency	13.5	13.5	13.5	MHz
t <sub>PU</sub>	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**Pullable Crystal Specifications**

Parameter	Description	Min.	Typ.	Max.	Unit
CR <sub>load</sub>	Crystal Load Capacitance		12.4		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T <sub>o</sub>	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT <sub>s</sub>	Stability over Temperature and Aging		± 20	± 50	ppm

**DC Electrical Characteristics**

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3 V (source)	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3 V (sink)	12	24		mA
C <sub>IN</sub>	Input Capacitance				7	pF
I <sub>Iz</sub>	Input Leakage Current			5		μA
f <sub>Δx0</sub>	V <sub>CXO</sub> Pullability Range		-150		+150	ppm
V <sub>VCXO</sub>	V <sub>CXO</sub> Input Range		0		AV <sub>DD</sub>	V
I <sub>DD</sub>	Supply Current	V <sub>DD</sub> = 3.45V, Cload = 15pF		15	20	mA

**AC Electrical Characteristics (V<sub>DD</sub> = 3.3V)**

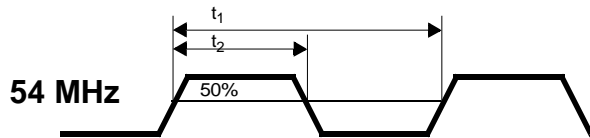
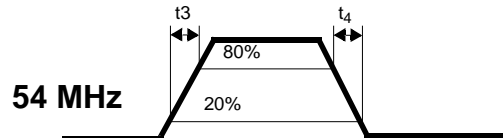
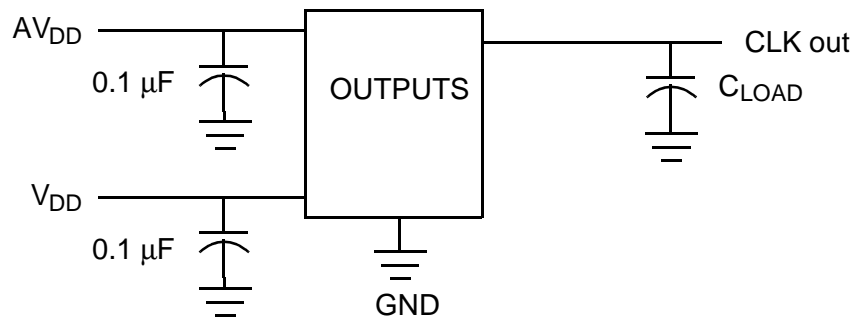
Parameter <sup>[3]</sup>	Description	Conditions	Min.	Typ.	Max.	Unit
DC = t <sub>2</sub> /t <sub>1</sub>	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V <sub>DD</sub>	45	50	55	%
ER <sub>0</sub>	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V <sub>DD</sub> , Cload = 15 pF (see <i>Figure 2</i> )	0.8	1.4		V/ns
EF <sub>0</sub>	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V <sub>DD</sub> , Cload = 15 pF (see <i>Figure 2</i> )	0.8	1.4		V/ns
t <sub>g</sub>	Clock Jitter	Peak to Peak period jitter			200	ps

**AC Electrical Characteristics ( $V_{DD} = 3.3V$ )**

Parameter <sup>[3]</sup>	Description	Conditions	Min.	Typ.	Max.	Unit
$t_{10}$	PLL Lock Time				3	ms

**Notes:**

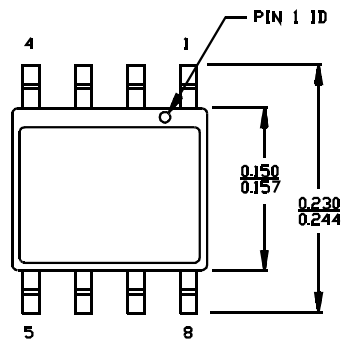
2. Rated for 10 years.
3. Not 100% tested.


**Figure 1. Duty Cycle Definition;  $DC = t_2/t_1$** 

**Figure 2. Rise and Fall Time Definitions:  
 $ER = 0.6 \times V_{DD}/t_3$ ,  $EF = 0.6 \times V_{DD}/t_4$** 
**Test Circuit**

**Ordering Information**

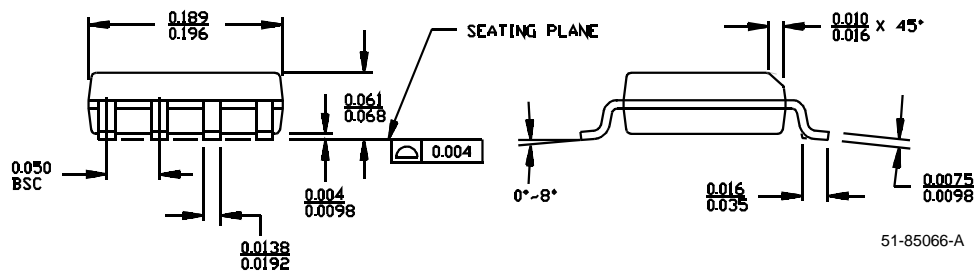
Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2411SC-1	S8	8-pin SOIC	Commercial	3.3V
CY2411SC-1T	S8	8-pin SOIC-Tape and Reel	Commercial	3.3V

Pin Diagrams

8-lead (150-mil) SOIC S8



1. DIMENSIONS IN INCHES MIN. MAX.
2. PIN 1 ID IS OPTIONAL. ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME



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Document Number: 38-07193

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110594	11/07/01	DSG	Change from Spec number: 38-00957 to 38-07193
*A	111572	04/30/02	CKN	Changed title to "MPEG Clock Generator with VCXO" Added -1 data on pp. 1 and 3
*B	121875	12/14/02	RBI	Power up requirements added to Operating Conditions Information