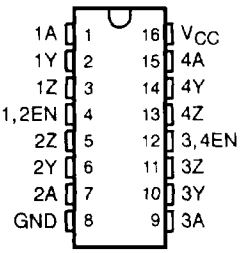
SLLS098A – MAY 1980 – REVISED MAY 1995

- **Meets or Exceeds Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**
- **Designed to Be Interchangeable With Motorola MC3487**

D OR N PACKAGE
(TOP VIEW)




## description

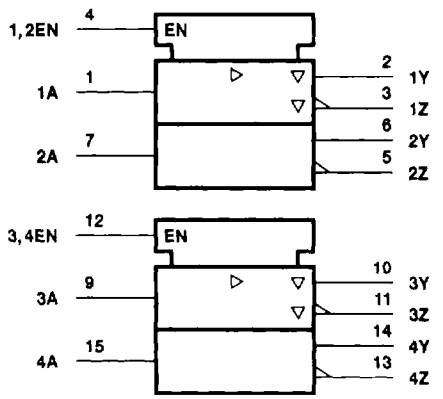
The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI EIA/TIA-422-B and ITU Recommendation V.11. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

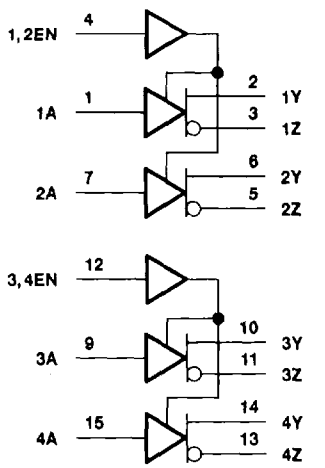
The MC3487 is characterized for operation from 0°C to 70°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

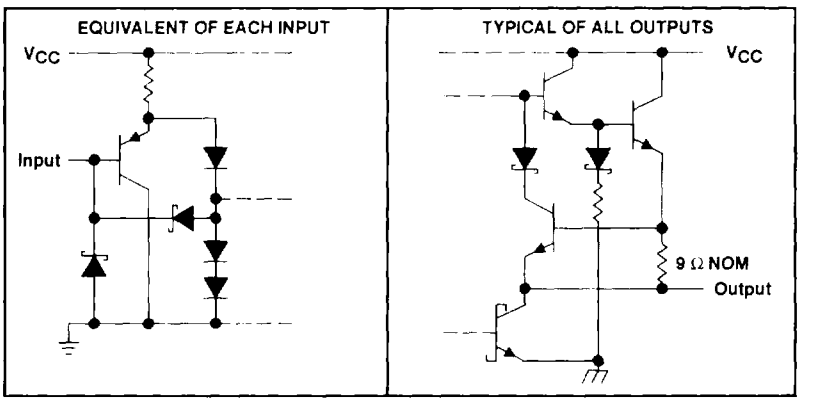


**FUNCTION TABLE**
**(each driver)**

| INPUT | OUTPUT ENABLE | OUTPUTS | |
|---|---|---|---|
| | | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

H = TTL high level, L = TTL low level, X = irrelevant, Z = High impedance

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) ..... 8 V
Input voltage, $V_I$ ..... 5.5 V
Output voltage, $V_O$ ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, $T_A$ ..... 0°C to 70°C
Storage temperature range, $T_{stg}$ ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage, $V_{OD}$, are with respect to the network ground terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, | $I_{OH}$ = −20 mA | 2.5 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, | $I_{OL}$ = 48 mA | | 0.5 | V |
| $\lvert V_{OD}\rvert$ | Differential output voltage | $R_L$ = 100 Ω, | See Figure 1 | | 2 | | |
| $\Delta\lvert V_{OD}\rvert$ | Change in magnitude of differential output voltage† | $R_L$ = 100 Ω, | See Figure 1 | | | ±0.4 | V |
| $V_{OC}$ | Common-mode output voltage‡ | $R_L$ = 100 Ω, | See Figure 1 | | | 3 | V |
| $\Delta\lvert V_{OC}\rvert$ | Change in magnitude of common-mode output voltage† | $R_L$ = 100 Ω, | See Figure 1 | | | ±0.4 | V |
| $I_O$ | Output current with power off | $V_{CC}$ = 0 | $V_O$ = 6 V | | | 100 | µA |
| | | | $V_O$ = −0.25 V | | | −100 | |
| $I_{OZ}$ | High-impedance-state output current | Output enables at 0.8 V | $V_O$ = 2.7 V | | | 100 | µA |
| | | | $V_O$ = 0.5 V | | | −100 | |
| $I_I$ | Input current at maximum input voltage | $V_I$ = 5.5 V | | | | 100 | µA |
| $I_{IH}$ | High-level input current | $V_I$ = 2.7 V | | | | 50 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0.5 V | | | | −400 | µA |
| $I_{OS}$ | Short-circuit output current§ | $V_I$ = 2 V | | | −40 | −140 | mA |
| $I_{CC}$ | Supply current (all drivers) | Outputs disabled | | | | 105 | mA |
| | | Outputs enabled, | No load | | | 85 | |

† $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from a high level to a low level.

‡ In ANSI Standard EIA/TIA-422-B, $V_{OC}$, which is the average of the two output voltages with respect to ground, is called output offset voltage, $V_{OS}$.

§ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 15 pF, | See Figure 2 | | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 20 | ns |
| | Skew time | | | | 6 | ns |
| $t_{t(OD)}$ | Differential-output transition time | $C_L$ = 15 pF, | See Figure 3 | | 20 | ns |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 50 pF, | See Figure 4 | | 30 | ns |
| $t_{PZL}$ | Output enable time to low level | | | | 30 | ns |
| $t_{PHZ}$ | Output disable time from high level | | | | 25 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | | 30 | ns |

## PARAMETER MEASUREMENT INFORMATION

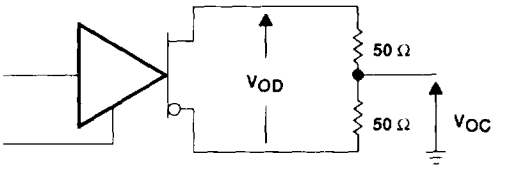



Figure 1. Differential and Common-Mode Output Voltages

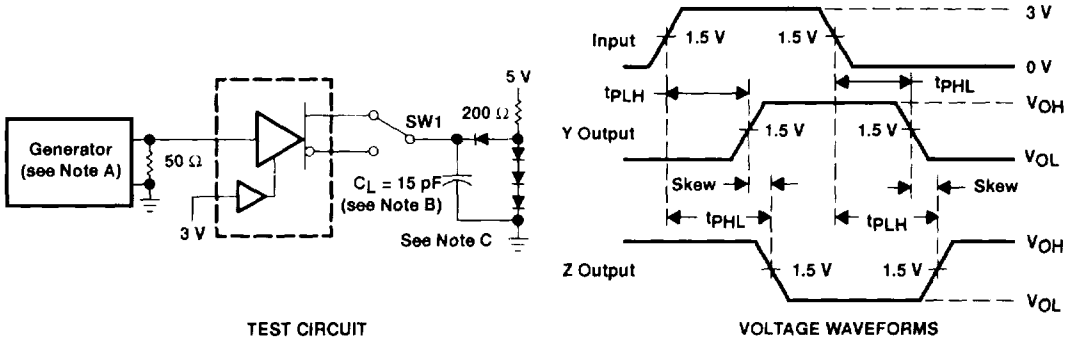



Figure 2. Test Circuit and Voltage Waveforms

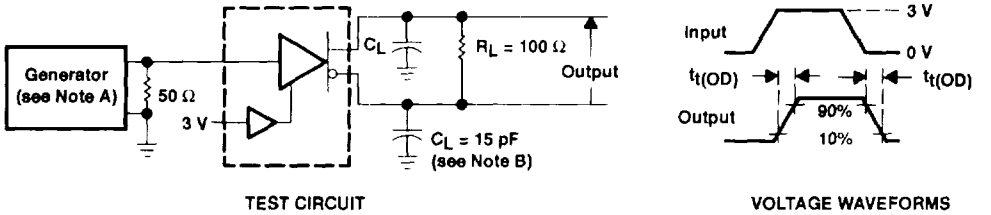
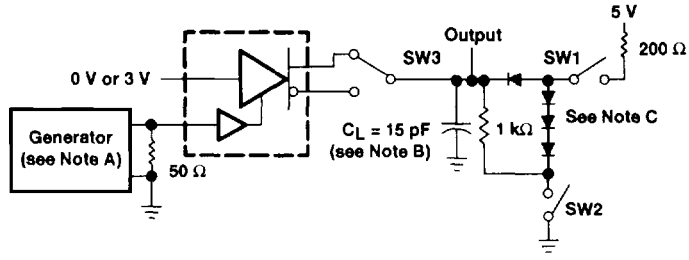


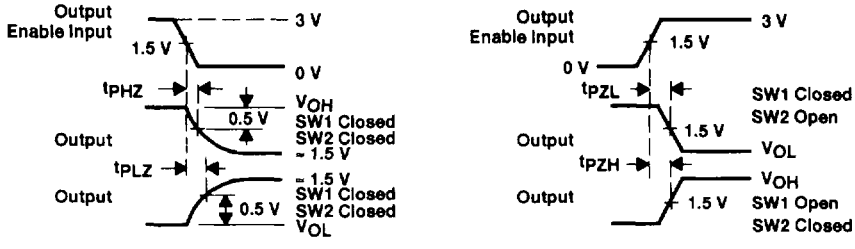

Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. $C_L$ includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

**Figure 4. Driver Test Circuit and Voltage Waveforms**

NOTES: D. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≈ 50%, $Z_O \approx 50\ \Omega$.
E. $C_L$ includes probe and stray capacitance.
F. All diodes are 1N916 or 1N3064.