

✓ 54LS/74LS540 010686  
 ✓ 54LS/74LS541 010698

**OCTAL BUFFER/LINE DRIVER**  
 (With 3-State Outputs)

**DESCRIPTION** — The 'LS540 and 'LS541 are similar in function to the 'LS240 and 'LS241, respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGIN
- PNP INPUTS REDUCE LOADING
- 3-STATE OUTPUTS DRIVE BUS LINES
- INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIER INTERFACE TO MICROPROCESSORS
- FULLY TTL AND CMOS COMPATIBLE

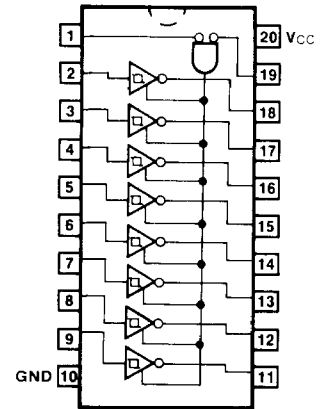
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0° C to +70° C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55° C to +125° C	
Plastic DIP (P)	A	74LS540PC		9Z
	B	74LS541PC		
Ceramic DIP (D)	A	74LS540DC	54LS540DM	4E
	B	74LS541DC	54LS541DM	
Flatpak (F)	A	74LS540FC	54LS540FM	4F
	B	74LS541FC	54LS541FM	

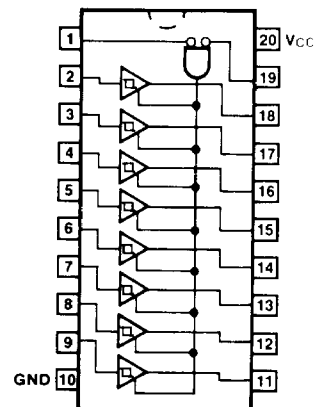
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

**CONNECTION DIAGRAMS**  
 PINOUT A



**PINOUT B**



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TRUTH TABLE

INPUTS			OUTPUTS	
E <sub>1</sub>	E <sub>2</sub>	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## DC AND AC CHARACTERISTICS: See Section 3\*

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current	'LS540	50	mA	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0 V V <sub>E</sub> = 4.5 V
		'LS541	54		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output ('LS540)		14 18	ns	Figs. 3-1, 3-4, C <sub>L</sub> = 50 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output ('LS541)		18 18	ns	Figs. 3-1, 3-5, C <sub>L</sub> = 50 pF
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		23 30	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 50 pF
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF

\*DC limits apply over operating temperature range; AC limits apply at T<sub>A</sub> = +25° C and V<sub>CC</sub> = +5.0 V.