

QS3253 Advanced Information



**High-Speed CMOS  
QuickSwitch®  
Dual 4:1 Mux / Demux**

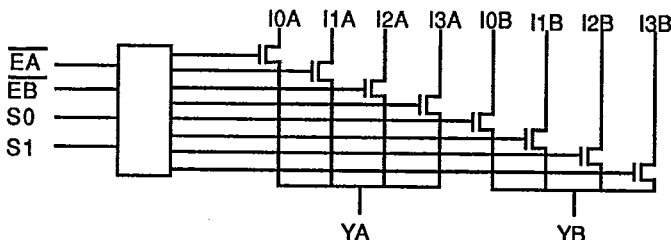
QS3253

**FEATURES/BENEFITS**

- 5Ω switches connect inputs to outputs
- Pin compatible to the 74F253, 74FCT253, and 74FCT253T
- Undershoot clamp diodes on all I/Os
- Low power CMOS proprietary technology
- Zero propagation delay
- TTL-compatible control inputs
- Zero ground bounce in flow-through mode
- TTL compatible control inputs
- Available in 16-pin DIP, SOIC, & QSOP

**DESCRIPTION**

The QS3251 is a high speed CMOS TTL-compatible dual 4:1 multiplexer/demultiplexer. The QS3253 has 3-state outputs. The QS3253 is function and pinout compatible QuickSwitch version of the 74F251, 74FCT253 and the 74ALS/AS/LS253 dual 4:1 multiplexers. The low on resistance (5 ohms) of the 3251 allows inputs to be connected outputs without adding propagation delay and without generating additional ground bounce noise.

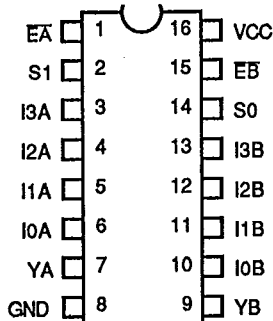


7

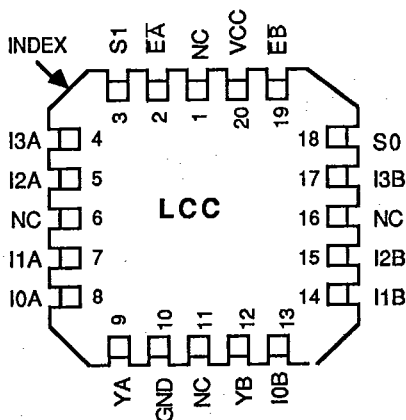
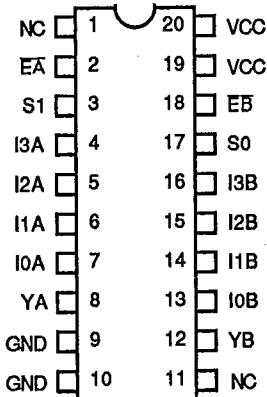
**QS3253 Advanced Information**

**QS3253 PINOUT**

**PDIP, SOIC, QSOP**



**HQSOP**



**ALL PINS TOP VIEW**

Note: Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code S0).

**PIN DESCRIPTION**

Name	I/O	Description
Ixx	I	Data In
S0-1	I	Select
EA, EB	I	Enable
YA, YB	O	Data Out

**FUNCTION TABLE**

Enable		Select		253		Function
EA	EB	S1	S0	YA	YB	
H	X	X	X	Hi-Z	X	Disable A
X	H	X	X	X	Hi-Z	Disable B
L	L	L	L	I0A	I0B	S1-0 = 0
L	L	L	H	I1A	I1B	S1-0 = 1
L	L	H	L	I2A	I2B	S1-0 = 2
L	L	H	H	I3A	I3B	S1-0 = 3

**QS3253 Advanced Information**

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground..... -0.5V to +7.0V  
 DC Switch Voltage  $V_S$  ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage  $V_I$  ..... -0.5V to  $V_{CC} + 0.5V$   
 AC Input Voltage (for a pulse width  $\leq 20$  ns)..... -3.0V  
 DC Input Diode Current with  $V_I < 0$ ..... -20 mA  
 DC Channel Current Max. current/pin..... 120 mA  
 Maximum Power Dissipation..... 0.5 watts  
 $T_{STG}$  Storage Temperature..... -65° to +165°C

**CAPACITANCE**

$T_A = 25^\circ C$ ,  $f = 1$  MHz,  $V_{in} = 0V$ ,  $V_{out} = 0V$

Pins	SOIC		QSOP		PDIP		Unit
	Typ	Max	Typ	Max	Typ	Max	
Controls	3		3		4		pF
QuickSwitch Channels	7		7		8		pF

Note: Capacitance is characterized but not tested

**QS3253 Advanced Information**

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

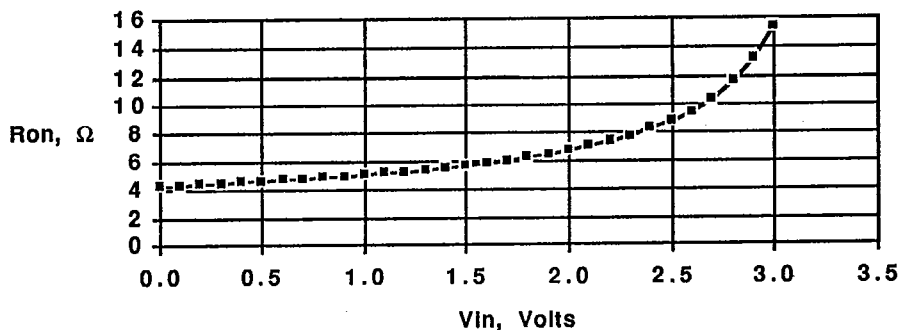
Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$  Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	-	-	0.8	Volts
Iin	Input Leakage Current	$0 \leq V_{in} \leq V_{CC}$	-	-	5	$\mu\text{A}$
Ioz	Off State Current (Hi-Z)	$0 \leq I, Y \leq V_{CC}$	-	-	5	$\mu\text{A}$
Ios	Short Circuit Current (2)	$I(Y) = 0\text{V}, Y(I) = V_{CC}$	-	300	-	mA
Vic	Clamp Diode Voltage	$V_{CC} = \text{Min}, I_{in} = -18\text{ mA}$	-	-0.7	-1.2	Volts
Ron	Switch On Resistance (Note 3)	$V_{CC} = \text{Min}, V_{in} = 0.0\text{ Volts}$ $I_{on} = 30\text{ mA}$	-	5	7	$\Omega$
		$V_{CC} = \text{Min}, V_{in} = 2.4\text{ Volts}$ $I_{on} = 15\text{ mA}$	-	10	15	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be used to test this high power condition, and the duration is 1 second.
3. Measured by voltage drop between A and Y pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two pins.
4. During input/output leakage testing all pins are at a High or Low state, and the  $\overline{OE}$  control is High.

**On Resistance vs Vin @ 4.75 Vcc (338X Only)**



---



---

**QS3253 Advanced Information**


---



---

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = MAX, V <sub>I</sub> = GND or V <sub>cc</sub> , f = 0	-	-	2.5	mA
ΔI <sub>cc</sub>	Pwr Supply Current, per Input High (2)	V <sub>cc</sub> = MAX, Input = 3.4 V, f = 0 Per control input	-	-	3.5	mA
Q <sub>ccd</sub>	Dynamic Pwr Supply Current per MHz (3)	V <sub>cc</sub> = MAX, I & Y pins open, Control input toggling @ 50% duty cycle	-	-	0.25	mA/ MHz

**Notes:**

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (V<sub>I</sub>=3.4V, control inputs only). I and Y pins do not contribute to I<sub>cc</sub>.
3. Guaranteed by design. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition.

---



---

**QS3253 Advanced Information**


---



---

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$  Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$   
 $C_{load} = 50\text{ pF}$ ,  $R_{load} = 500\Omega$  unless otherwise noted.

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t <sub>IY</sub>	Data Propagation Delay In to Y	2,3		0.25		0.25	ns
t <sub>SY</sub>	Switch Turn On Delay S <sub>n</sub> to Y	1	0.5	6.6	0.5	7.6	ns
t <sub>EY</sub>	Switch Turn On Delay E <sub>n</sub> to Y	1,2	0.5	6.0	0.5	7.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Switch Turn Off Delay E <sub>n</sub> to Y	1	0.5	6.0	0.5	7.0	ns

**Notes:**

- See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.