9401

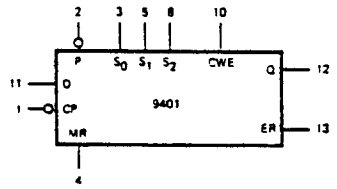
CRC GENERATOR/CHECKER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disc and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is fully compatible with all TTL families.

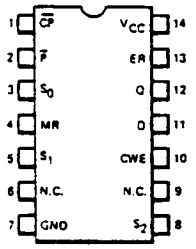
- GUARANTEED 10 MHz DATA RATE
- EIGHT SELECTABLE POLYNOMIALS
- ERROR INDICATOR
- SEPARATE PRESET AND CLEAR CONTROLS
- AUTOMATIC RIGHT JUSTIFICATION
- FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES
- 14-PIN PACKAGE
- TYPICAL APPLICATIONS:
  - FLOPPY AND OTHER DISC STORAGE SYSTEMS
  - DIGITAL CASSETTE AND CARTRIDGE SYSTEMS
  - DATA COMMUNICATION SYSTEMS

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

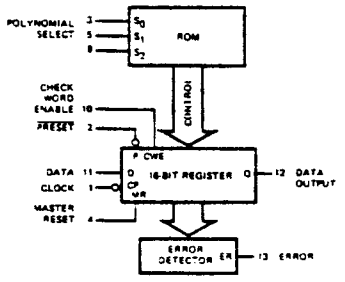
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	1.0 U.L.	0.23 U.L.
$\overline{D}$	Data Input	1.0 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH-to-LOW Transition) Input	1.0 U.L.	0.23 U.L.
CWE	Check Word Enable Input	1.0 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	1.0 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	1.0 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FUNCTIONAL DESCRIPTION – The 9401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in *Table 1* by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates *(Figure 1)*. The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating *(Figure 2)*.

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

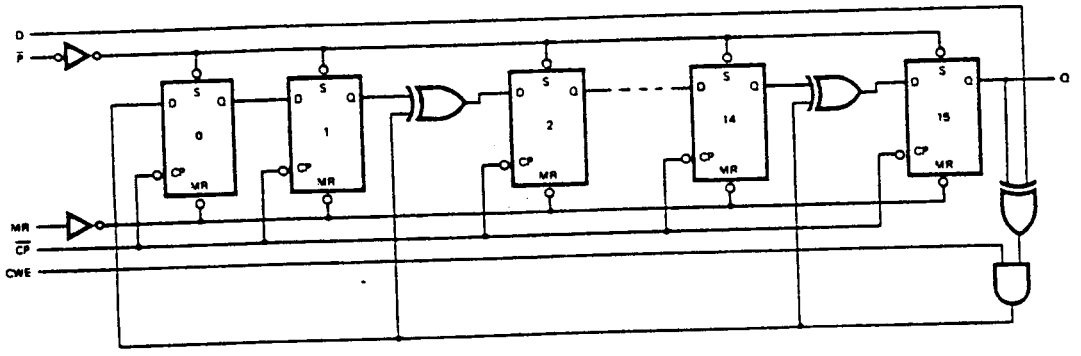


Fig. 1
EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage	XM & XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	40	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current			−0.22	−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70	110	mA	V_{CC} = MAX, Inputs Open

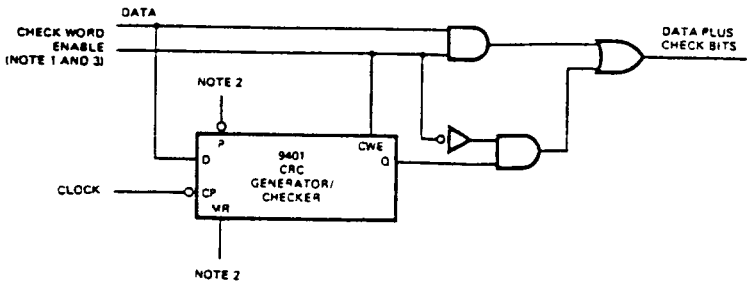
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 2)	LIMITS MAX	UNITS	CONDITIONS	
f_{max}	Maximum Clock Frequency	10	18		MHz	Fig. 3, 4, 5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation Delay, Preset to Data Output		40	60	ns		
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR or Preset to Error Output		40	60	ns		

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
$t_w\overline{CP}$ (L)	Clock Pulse Width (LOW)	35			ns	Fig. 2	C_L = 15 pF
t_sD	Set-up Time, Data to Clock	55	35		ns	Fig. 6	
t_sCWE	Set-up Time, CWE to Clock	55	35		ns		
t_h	Hold Time, Data and CWE to Clock	0	−10		ns		
t_wP (L)	Preset Pulse Width (LOW)	40	30		ns	Fig. 4	
t_wMR (H)	Master Reset Pulse Width (HIGH)	35	25		ns	Fig. 6	
t_{rec}	Recovery Time, MR and Preset to Clock	50	25		ns	Fig. 4, 5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Fig. 2
CHECK WORD GENERATION

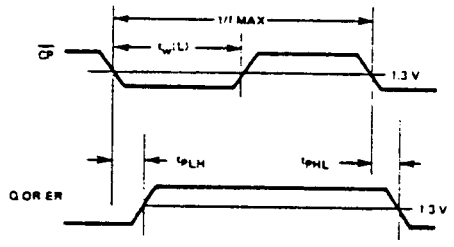


Fig. 3
PROPAGATION DELAYS, $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

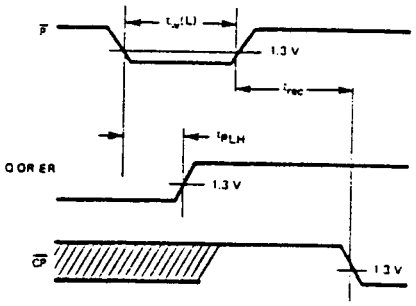


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME $\overline{P}$ TO $\overline{CP}$

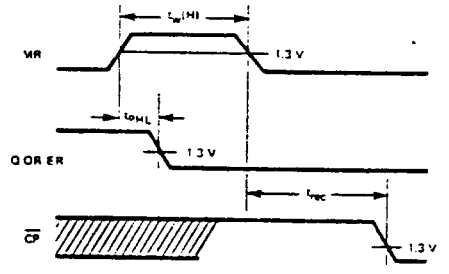


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

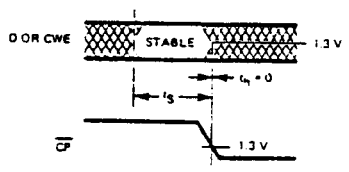


Fig. 6
SET-UP AND HOLD TIMES, D TO $\overline{CP}$ AND CWE TO $\overline{CP}$