Data Sheet | October 2000 | File Number 1924.5

4MHz, BiMOS Microprocessor Operational Amplifier with MOSFET Input/CMOS Output

CA5160 is an integrated circuit operational amplifier that combines the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5160 is a frequency compensated version of the popular CA5130 series. It is designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5160 operates at supply voltages ranging from +5V to +16V, or ±2.5V to ±8V when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage. It has guaranteed specifications for 5V operation over the full military temperature range of -55^{o}C to 125^{o}C.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA5160E	-55 to 125	8 Ld PDIP	E8.3
CA5160M96 (5160)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15

Features

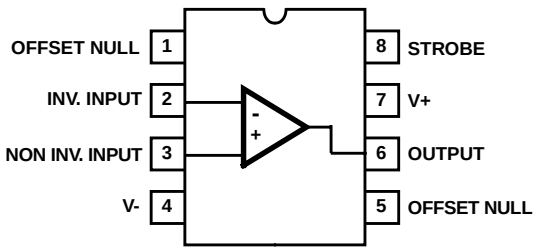
- MOSFET Input Stage
  - Very High Z_I; 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I; at 15V Operation . . . . . 5pA (Typ)
    at 5V Operation . . . . . 2pA (Typ)
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5160 Has Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5160 is Guaranteed to Operate Down to 4.5V for A_{OL}
- CA5160 is Guaranteed Up to ±7.5V

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface With Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Pinout

CA5160 (PDIP, SOIC)
TOP VIEW



NOTE: CA5160 devices have an on-chip frequency compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Absolute Maximum Ratings

Supply Voltage (V+ to V-) 16V
Differential Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 2). . . . . Indefinite

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	120	N/A
SOIC Package	165	N/A

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Pkg dept will choose one of following:

NOTE #1 θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2. Short circuit may be applied to ground or to either supply.

Electrical Specifications

$T_A = 25^oC$, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		V_{IO}	V_O = 2.5V	-	2	10	mV
Input Offset Current		I_{IO}	V_O = 2.5V	-	0.1	10	pA
Input Current		I_I	V_O = 2.5V	-	2	15	pA
Common Mode Rejection Ratio		CMRR	V_{CM} = 0 to 1V	70	80	-	dB
			V_{CM} = 0 to 2.5V	60	69	-	dB
Common Mode Input Voltage Range		V_{ICR}+		2.5	2.8	-	V
		V_{ICR}-		-	-0.5	0	V
Power Supply Rejection Ratio		PSRR	$\Delta V+ = 1V; \Delta V- = 1V$	55	67	-	dB
Large Signal Voltage Gain (Note 3)	V_O = 0.1 to 4.1V	A_{OL}	$R_L = \infty$	95	117	-	dB
	V_O = 0.1 to 3.6V		R_L = 10kΩ	85	102	-	dB
Source Current		I_{SOURCE}	V_O = 0V	1.0	3.4	4.0	mA
Sink Current		I_{SINK}	V_O = 5V	1.0	2.2	4.8	mA
Maximum Output Voltage	V_{OM}+	V_{OUT}	$R_L = \infty$	4.99	5	-	V
	V_{OM}-			-	0	0.01	V
	V_{OM}+		R_L = 10kΩ	4.4	4.7	-	V
	V_{OM}-			-	0	0.01	V
	V_{OM}+		R_L = 2kΩ	2.5	3.3	-	V
	V_{OM}-			-	0	0.01	V
Supply Current		I_{SUPPLY}	V_O = 0V	-	50	100	µA
		I_{SUPPLY}	V_O = 2.5V	-	320	400	µA

NOTE:

3. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications T_A = -55°C to 125°C, V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		V_{IO}	V_O = 2.5V	-	3	15	mV
Input Offset Current		I_{IO}	V_O = 2.5 V	-	0.1	10	nA
Input Current		I_I	V_O = 2.5V	-	2	15	nA
Common Mode Rejection Ratio		CMRR	V_{CM} = 0 to 1V	60	80	-	dB
			V_{CM} = 0 to 2.5V	50	75	-	dB
Common Mode Input Voltage Range		V_{ICR}+		2.5	2.8	-	V
		V_{ICR}-		-	-0.5	0	V
Power Supply Rejection Ratio		PSRR	ΔV+ = 2V	40	60	-	dB
Large Signal Voltage Gain (Note 4)	V_O = 0.1 to 4.1V	A_{OL}	R_L = ∞	90	110	-	dB
	V_O = 0.1 to 3.6V		R_L = 10kΩ	75	100	-	dB
Source Current		I_{SOURCE}	V_O = 0V	0.6	-	5.0	mA
Sink Current		I_{SINK}	V_O = 5V	0.6	-	6.2	mA
Maximum Output Voltage	V_{OM}+	V_{OUT}	R_L= ∞	4.99	5	-	V
	V_{OM}-			-	0	0.01	V
	V_{OM}+		R_L = 10kΩ	4.0	4.3	-	V
	V_{OM}-			-	0	0.01	V
	V_{OM}+		R_L = 2kΩ	2.0	2.5	-	V
	V_{OM}-			-	0	0.01	V
Supply Current	V_O = 0V	I_{SUPPLY}		-	170	220	µA
	V_O = 2.5V	I_{SUPPLY}		-	410	500	µA

NOTE:

4. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at R_L = 10kΩ.

Electrical Specifications T_A = 25°C, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		V_{IO}	V_S = ±7.5V	-	6	15	mV
Input Offset Current		I_{IO}	V_S = ±7.5V	-	0.5	30	pA
Input Current		I_I	V_S = ±7.5V	-	5	50	pA
Large Signal Voltage Gain		A_{OL}	V_O = 10V_{P-P}, R_L = 2kΩ	50	320	-	kV/V
				94	110	-	dB
Common Mode Rejection Ratio		CMRR		70	90	-	dB
Common Mode Input Voltage Range		V_{ICR}		10	-0.5 to 12	0	V
Power Supply Rejection Ratio		PSRR	ΔV+ = 1V; ΔV- = 1V, V_S = ±7.5V	-	32	320	µV/V
Maximum Output Voltage	V_{OM}+	V_{OUT}	R_L = 2kΩ	12	13.3	-	V
	V_{OM}-			-	0.002	0.01	V
	V_{OM}+		R_L = ∞	14.99	15	-	V
	V_{OM}-			-	0	0.1	V
Maximum Output Current	I_{OM}+ (Source)	I_O	V_O = 0V	12	22	45	mA
	I_{OM}- (Sink)		V_O = 15V	12	20	45	mA

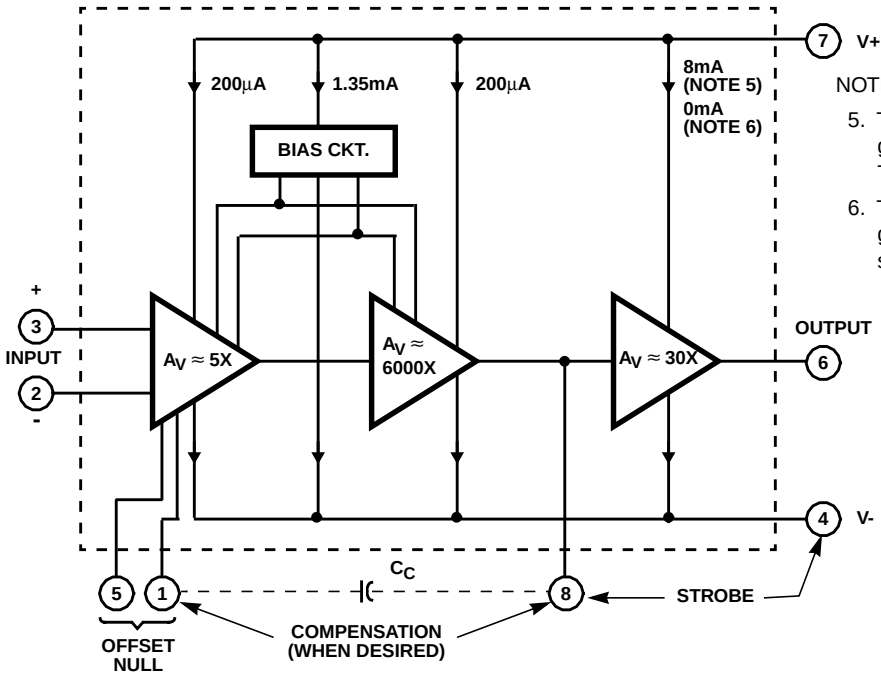
Electrical Specifications $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I+	$R_L = \infty$, V_O = 7.5V	-	10	15	mA
		$R_L = \infty$, V_O = 0V	-	2	3	mA
Input Offset Voltage Temperature Drift		$\Delta V_{IO}/\Delta T$	-	8	-	$\mu V/^oC$

Electrical Specifications For Design Guidance, At $T_A = 25^oC$, $V_{SUPPLY} = \pm 7.5V$, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	UNITS
Input Offset Voltage Adjustment Range			10kΩ Across Terminals 4 and 5 or 4 and 1	±22	mV
Input Resistance		R_I		1.5	TΩ
Input Capacitance		C_I	f = 1MHz	4.3	pF
Equivalent Input Noise Voltage		e_N	BW = 0.2MHz, R_S = 1MΩ	40	μV
			BW = 0.2MHz, R_S = 10MΩ	50	μV
Equivalent Input Noise Voltage		e_N	R_S = 100Ω, 1kHz	72	$nV/\sqrt{Hz}$
			R_S = 100Ω, 10kHz	30	$nV/\sqrt{Hz}$
Unity Gain Crossover Frequency		f_T		4	MHz
Slew Rate		SR		10	V/μs
Transient Response	Rise Time	t_R	C_C = 25pF, R_L = 2kΩ (Voltage Follower)	0.09	μs
	Overshoot	OS		10	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)		t_S	C_C = 25pF, R_L = 2kΩ, (Voltage Follower)	1.8	μs

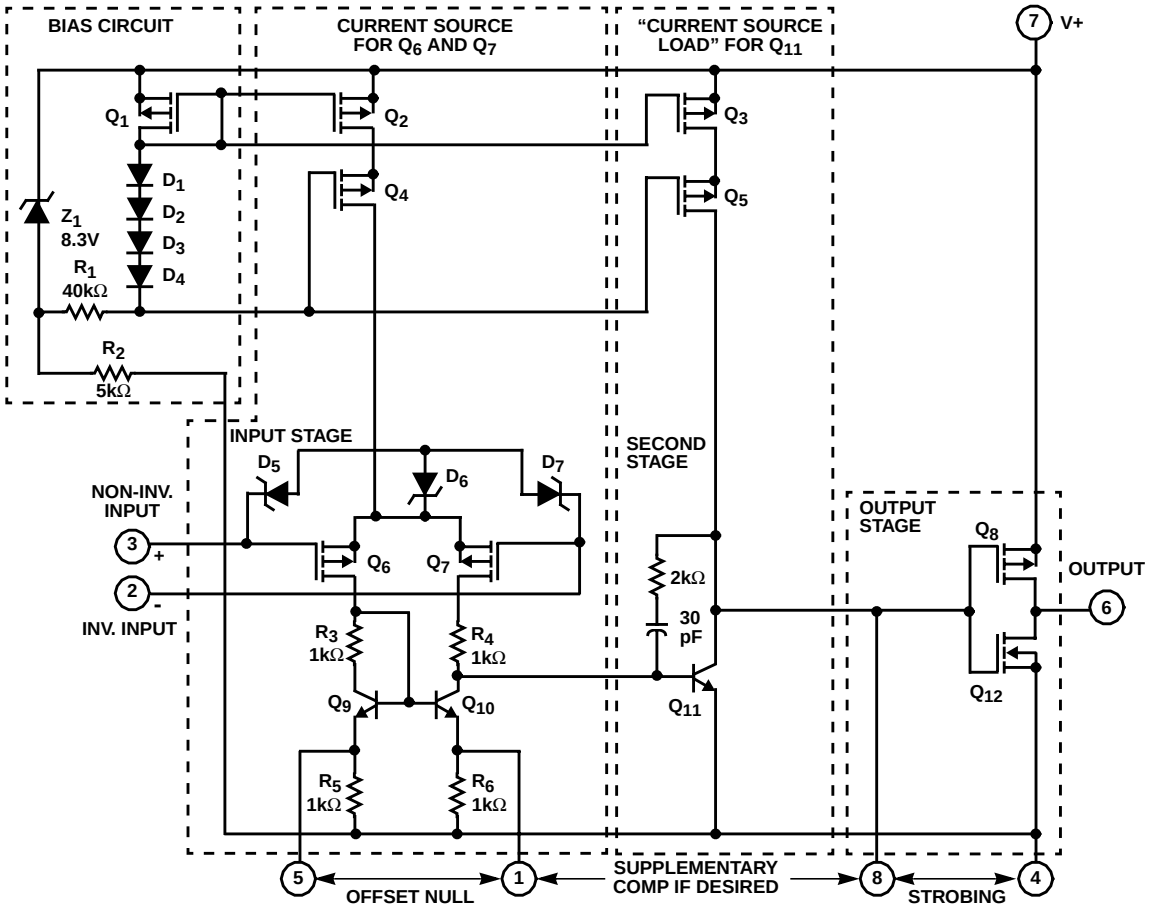
Block Diagram



NOTES:

5. Total supply voltage (for indicated voltage gains) = 15V with input terminals biased so that Terminal 6 potential is +7.5V above Terminal 4.
6. Total supply voltage (for indicated voltage gains) = 15V with output terminal driven to either supply rail.

Schematic Diagram



NOTE: Diodes D_5 through D_7 provide gate oxide protection for MOSFET Input Stage.

Application Information

Circuit Description

Refer to the block diagram of the CA5160 CMOS Operational Amplifier. The input terminals may be operated down to 0.5V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5160 circuit is ideal for single supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in the block diagram, provide the total gain of the CA5160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages

The circuit of the CA5160 is shown in the schematic diagram. It consists of a differential input stage using PMOS field effect transistors (Q_6, Q_7) working into a mirror pair of bipolar transistors (Q_9, Q_{10}) functioning as load resistors together with resistors R_3 through R_6. The mirror pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q_{11}). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4.

Cascode-connected PMOS transistors Q_2, Q_4, are the constant current source for the input stage. The biasing circuit for the constant current source is subsequently described. The small diodes D_5 through D_7 provide gate-oxide protection against high voltage transients, including static electricity during handling for Q_6 and Q_7.

Second Stage

Most of the voltage gain in the CA5160 is provided by the second amplifier stage, consisting of bipolar transistor Q_{11} and its cascode-connected load resistance provided by PMOS transistors Q_3 and Q_5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30pF capacitor and 2kΩ resistor connected between the base and collector of transistor Q_{11}. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit

At total supply voltages, somewhat above 8.3V, resistor R_2 and zener diode Z_1 serve to establish a voltage of 8.3V across the series connected circuit, consisting of resistor R_1, diodes D_1 through D_4, and PMOS transistor Q_1. A tap at the junction of resistor R_1 and diode D_4 provides a gate bias potential of about 4.5V for PMOS transistors Q_4 and Q_5 with respect to Terminal 7. A potential of about 2.2V is developed across diode connected PMOS transistor Q_1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q_2 and Q_3. It should be noted that Q_1 is “mirror connected” to both Q_2 and Q_3. Since transistors Q_1, Q_2 and Q_3 are designed to be identical, the approximately 200µA current in Q_1 establishes a similar current in Q_2 and Q_3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3V, zener diode Z_1 becomes non-conductive and the potential, developed across series connected R_1, D_1-D_4, and Q_1 varies directly with variations in supply voltage. Consequently, the gate bias for Q_4, Q_5 and Q_2, Q_3 varies in accordance with supply voltage variations. This variation results in deterioration of the power supply rejection ration (PSRR) at total supply voltages below 8.3V. Operation at total supply voltages below about 4.5V results in seriously degraded performance.

Output Stage

The output stage consists of a drain loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 20. Typical op-amp loads are readily driven by the output stage. Because large signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01% accuracy levels, including the negative supply rail.

Offset Nulling

Offset voltage nulling is usually accomplished with a 100,000Ω potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset null adjustment usually can be affected with the slider arm positioned in the mid point of the potentiometer’s total range.

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Specifications, the input current for the CA5160 Series Op Amps is typically 5pA at $T_A = 25^oC$ when Terminals 2 and 3 are at a common-mode potential of +7.5V with respect to negative supply Terminal 4. Figure 1 contains data showing the variation of input current as a function of common-mode input voltage at $T_A = 25^oC$. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2V. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the metal can package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the metal can case of the CA5160 is also internally tied to Terminal 4, input terminal 3 is essentially “guarded” from spurious leakage currents.

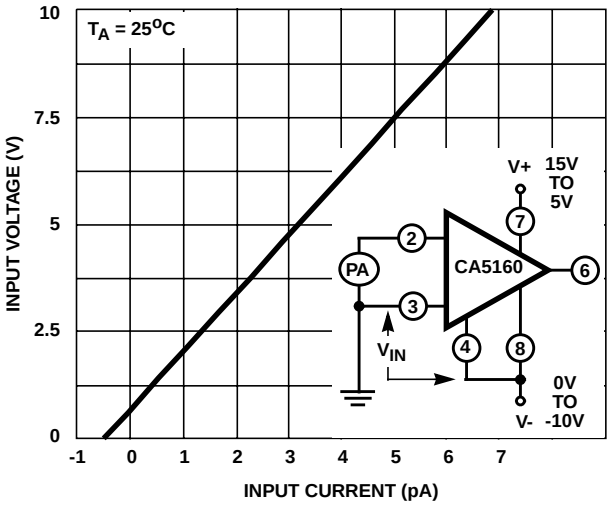


FIGURE 1. CA5160 INPUT CURRENT vs COMMON MODE VOLTAGE

Input Current Variation with Temperature

The input current of the CA5160 series circuits is typically 5pA at 25^oC. The major portion of this input current is due to leakage current through the gate protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10^oC increase in temperature. Figure 2 provides data on the

typical variation of input bias current as a function of temperature in the CA5160.

In applications requiring the lowest practical input current and incremental increases in current because of “warm-up” effects, it is suggested that an appropriate heat sink be used with the CA5160. In addition, when “sinking” or “sourcing” significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

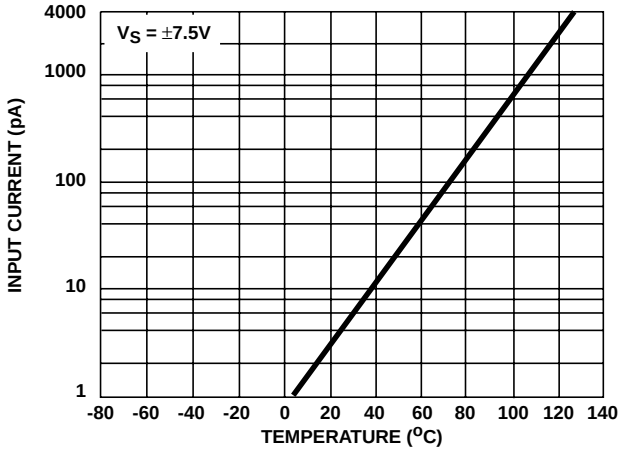


FIGURE 2. INPUT CURRENT vs TEMPERATURE

Input Offset Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a DC gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential DC bias voltage applied across Terminals 2 and 3. Figure 3 shows typical data pertinent to shifts in offset voltage encountered with CA5160 devices in metal can packages during life testing. At lower temperatures (metal can and plastic) for example at 85^{O}C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The $2V_{DC}$ differential voltage example represents conditions when the amplifier output state is “toggled”, e.g., as in comparator applications.

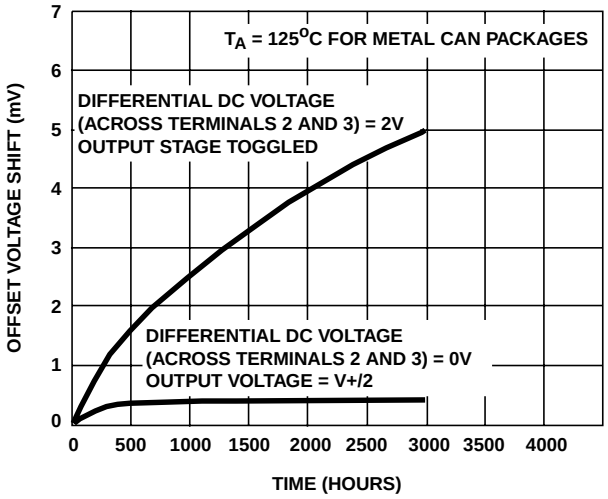


FIGURE 3. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Power Supply Considerations

Because the CA5160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 4A and 4B show the CA5160 connected for both dual and single-supply operation.

Dual-supply Operation: When the output voltage at Terminal 6 is 0V, the currents supplied by the two power supplies are equal. When the gate terminals of Q_8 and Q_{12} are driven increasingly positive with respect to ground, current flow through Q_{12} (from the negative supply) to the load is increased and current flow through Q_8 (from the positive supply) decreases correspondingly. When the gate terminals of Q_8 and Q_{12} are driven increasingly negative with respect to ground, current flow through Q_8 is increased and current flow through Q_{12} is decreased accordingly.

Single Supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (Number 6) voltage is at V+/2, i.e., the voltage-drops across Q_8 and Q_{12} are of equal magnitude. Figure 21 shows typical quiescent supply-current vs supply-voltage for the CA5160 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage transfer characteristics (see Figure 20). If either Q_8 or Q_{12} are swung out of their linear regions toward cutoff (a nonlinear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q_{12} is completely cut off and the supply-current to series-connected transistors Q_8, Q_{12} goes essentially to zero. The two preceding stages in the CA5160, however, continue

to draw modest supply-current (see the lower curve in Figure 21) even through the output stage is strobed off. Figure 4A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2kΩ) is connected between Terminal 6 and ground in the circuit of Figure 4B. Let it further be assumed again that the input terminal bias (Terminals 2 and 3) is such that the output terminal (Number 6) voltage is V+/2. Since PMOS transistor Q_8 must now supply quiescent current to both R_L and transistor Q_{12}, it should be apparent that under these conditions the supply current must increase as an inverse function of the R_L magnitude. Figure 27 shows the voltage drop across PMOS transistor Q_8 as a function of load current at several supply voltages. Figure 20 shows the voltage transfer characteristics of the output stage for several values of load resistance.

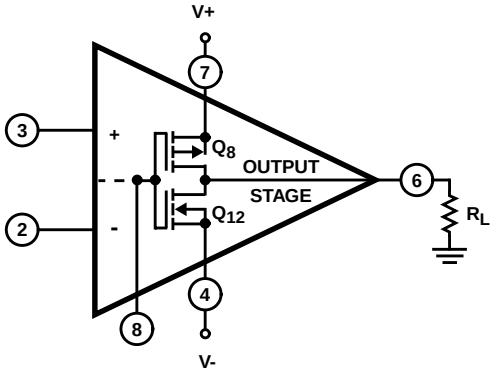


FIGURE 4A. DUAL POWER-SUPPLY OPERATION

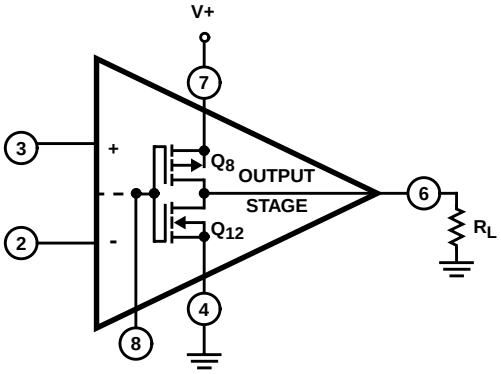


FIGURE 4B. SINGLE POWER-SUPPLY OPERATION

FIGURE 4. CA5160 OUTPUT STAGE IN DUAL AND SINGLE POWER SUPPLY OPERATION

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5160 is most advantageous in applications where in the source resistance of the input signal is on the order of 1MΩ or more. In this case, the total input-referred noise voltage is typically only 40μV when the test-circuit amplifier of Figure 5 is operated at a total supply voltage of 15V. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1MΩ, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

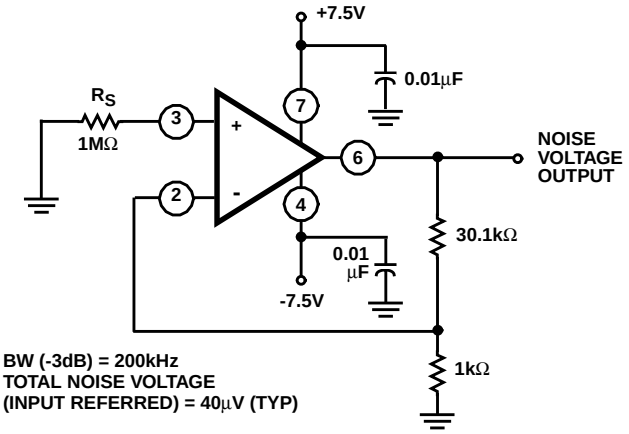


FIGURE 5. TEST-CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA5160, are particularly suited to service as voltage followers. Figure 6 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5160 in a split supply-configuration.

A voltage follower, operated from a single-supply, is shown in Figure 7 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 7B with input signal ramping. The waveforms in Figure 7C show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5V below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 7C also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5160 in a single-supply voltage follower application.

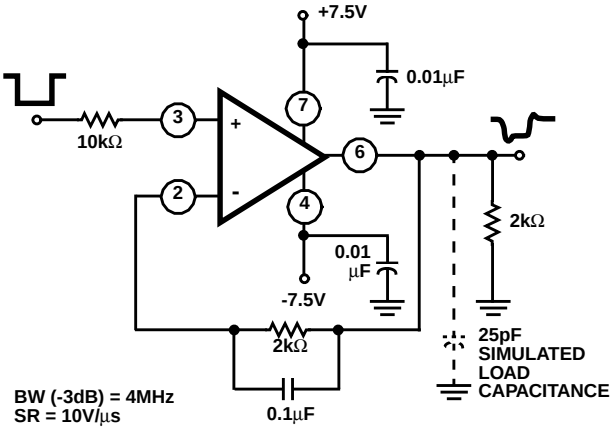
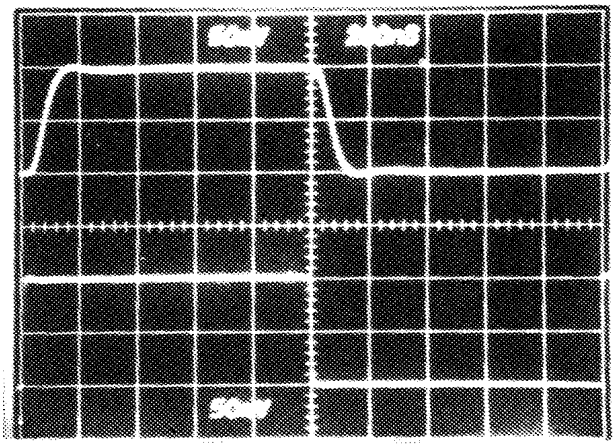
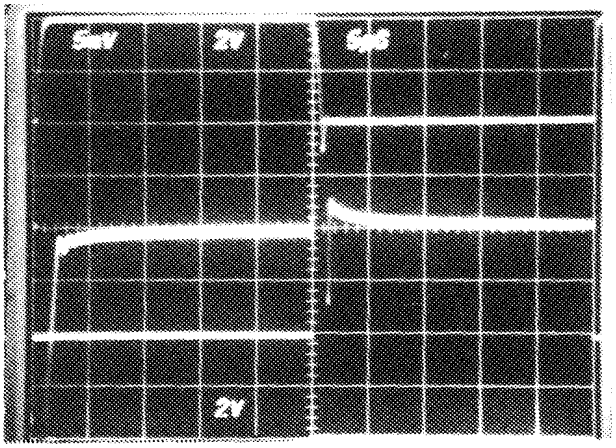


FIGURE 6A. DUAL SUPPLY FOLLOWER



Top Trace: Output
Bottom Trace: Input

FIGURE 6B. SMALL SIGNAL RESPONSE



Top Trace: Output Signal
Center Trace: Difference Signal 5mV/Div.
Bottom Trace: Input Signal

FIGURE 6C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 6. SPLIT SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS

9 Bit CMOS DAC

A typical circuit of a 9 bit Digital-to-Analog Converter (DAC) (see Note) is shown in Figure 8. This system combines the concepts of multiple-switch CMOS ICs, a low cost ladder network of discrete metal-oxide-film resistors, a CA5160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10V logic levels are used in the circuit of Figure 8.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three “inverters”, each “inverter” functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of 1% tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000Ω resistors from the same manufacturing lot.

A single 15V supply provides a positive bus for the CA5160 follower amplifier and feeds the CA3085 voltage regulator. A “scale-adjust” function is provided by the regulator output control, set to a nominal 10V level in this system. The line-voltage regulation (approximately 0.2%) permits a 9 bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error Amplifier in Regulated Power Supplies

The CA5160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach 0V.

The circuit shown in Figure 9 uses a CA5160 as an error amplifier in a continuously adjustable 1A power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero with only one DC power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents “turn-on overshoot”, a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have influence on the regulator performance.

NOTE: “Digital-to-Analog Conversion Using the Intersil CD4007A CMOS IC”, Application Note AN6080.

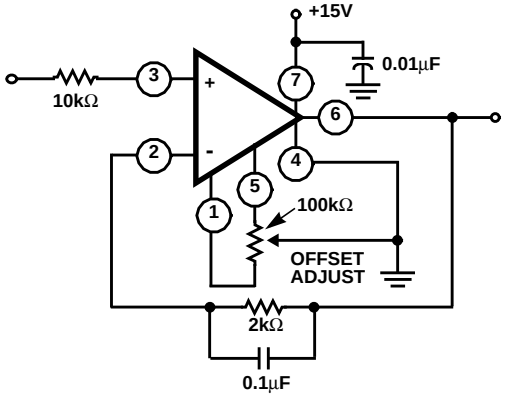


FIGURE 7A. SINGLE SUPPLY FOLLOWER

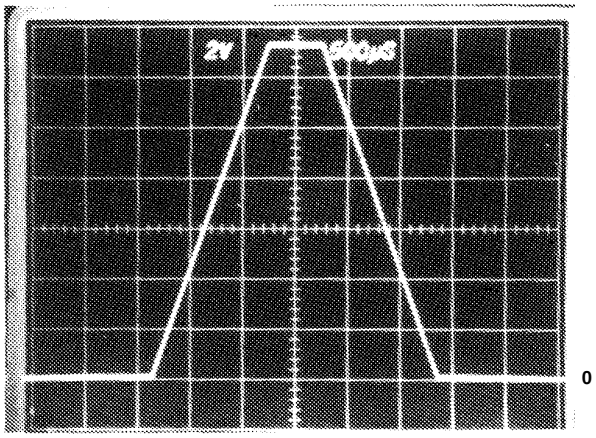
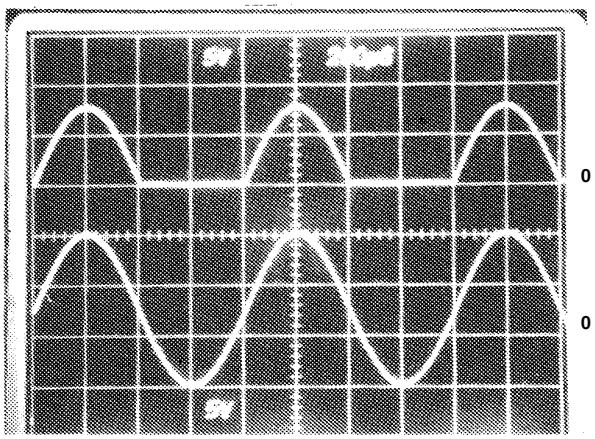


FIGURE 7B. OUTPUT SIGNAL WITH INPUT SIGNAL RAMPING



Top Trace: Output
Bottom Trace: Input

FIGURE 7C. OUTPUT-WAVEFORM WITH GROUND-REFERENCE SINE-WAVE INPUT

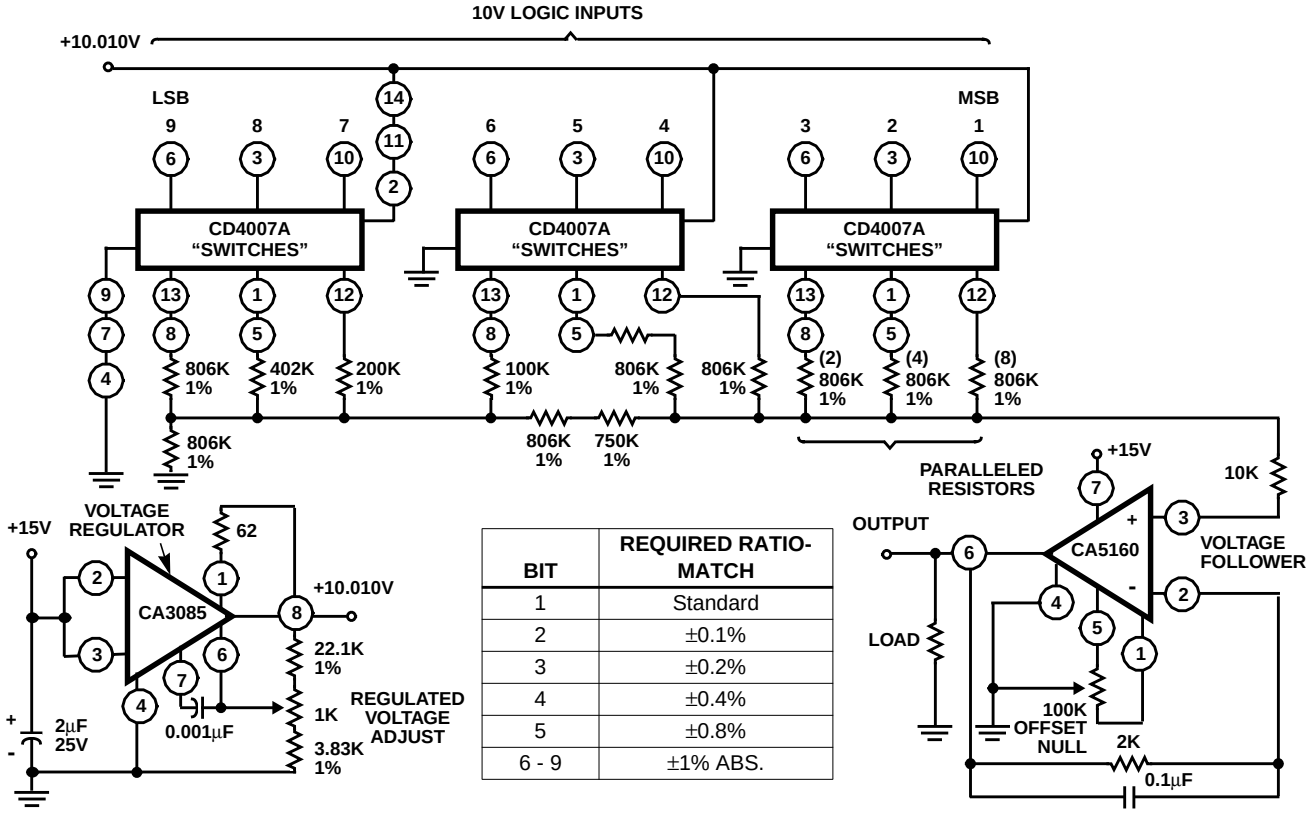
FIGURE 7. SINGLE SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS (e.g., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Figure 10. The oscillator operates with a tracking error on the order of 0.02% and a temperature coefficient of 0.01%/^{o}C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (Terminal 6) of A_1 (a CA5130) can swing within about 10mV of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{AVG} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 (a CA5160) via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{AVG} = V_1$. This circuit condition is accomplished by feeding an output signal from Terminal 6 of A_2 through R_4, D_4 to the inverting terminal (Terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

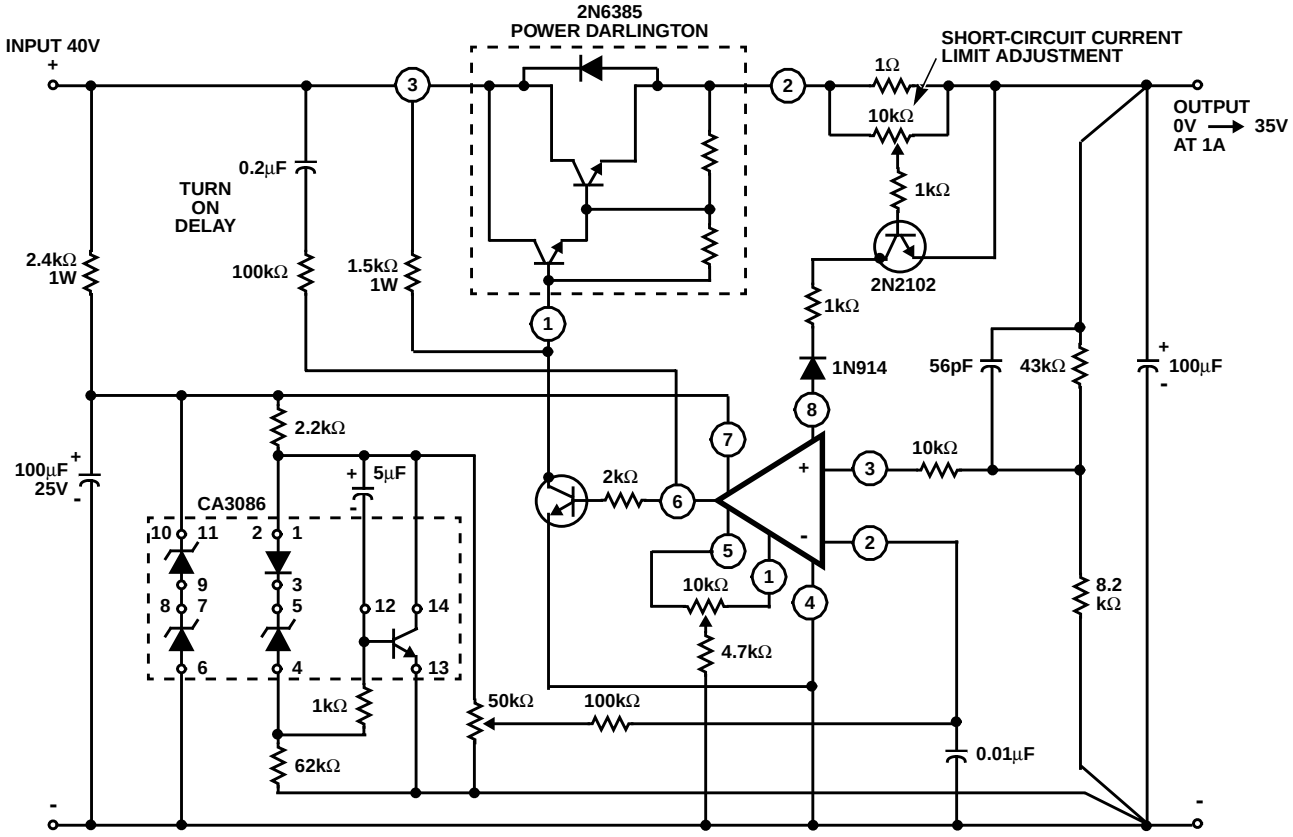
Voltmeter With High Input Resistance

The voltmeter circuit shown in Figure 11 illustrates an application in which a number of the CA5160 characteristics are exploited. Range-switch SW_1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10kΩ current-limiting resistor. The circuit is powered by a single 8.4V mercury battery. With zero input signal, the circuit consumes somewhat less than 500µA plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500µA.



BIT	REQUIRED RATIO-MATCH
1	Standard
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS.

FIGURE 8. 9 BIT DAC USING CMOS DIGITAL SWITCHES AND CA5160



Hum and Noise Output <250µV_{RMS}; Regulation (No Load to Full Load) <0.005%; Input Regulation <0.01%/V

FIGURE 9. CA5160 VOLTAGE REGULATOR CIRCUIT (0.1 TO 35V AT 1A)

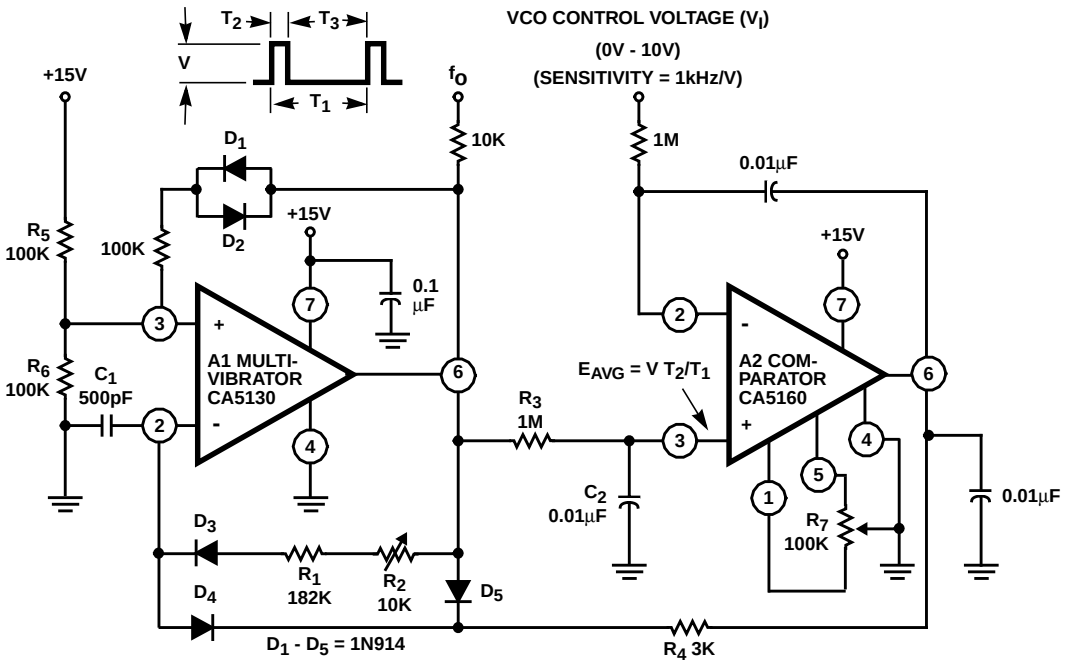


FIGURE 10. VOLTAGE CONTROLLED OSCILLATOR

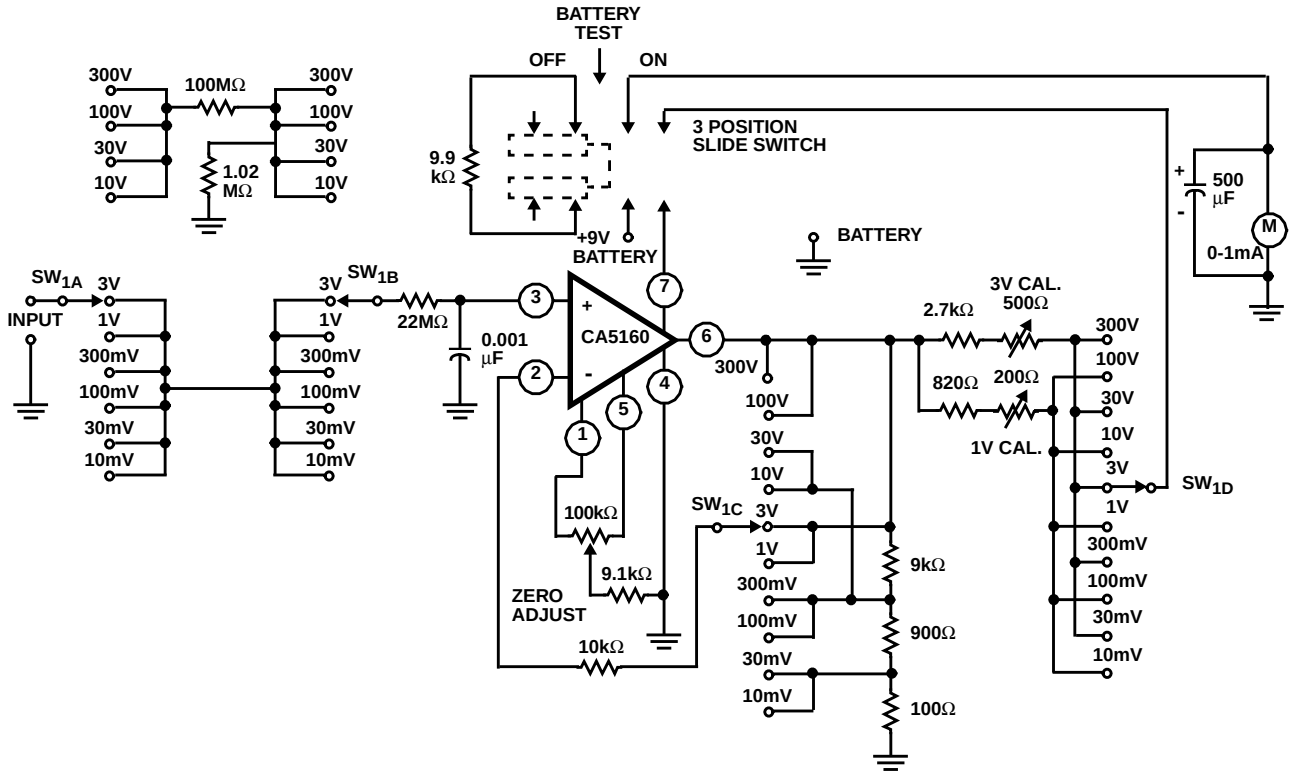


FIGURE 11. CA5160A HIGH INPUT RESISTANCE DC VOLTMETER

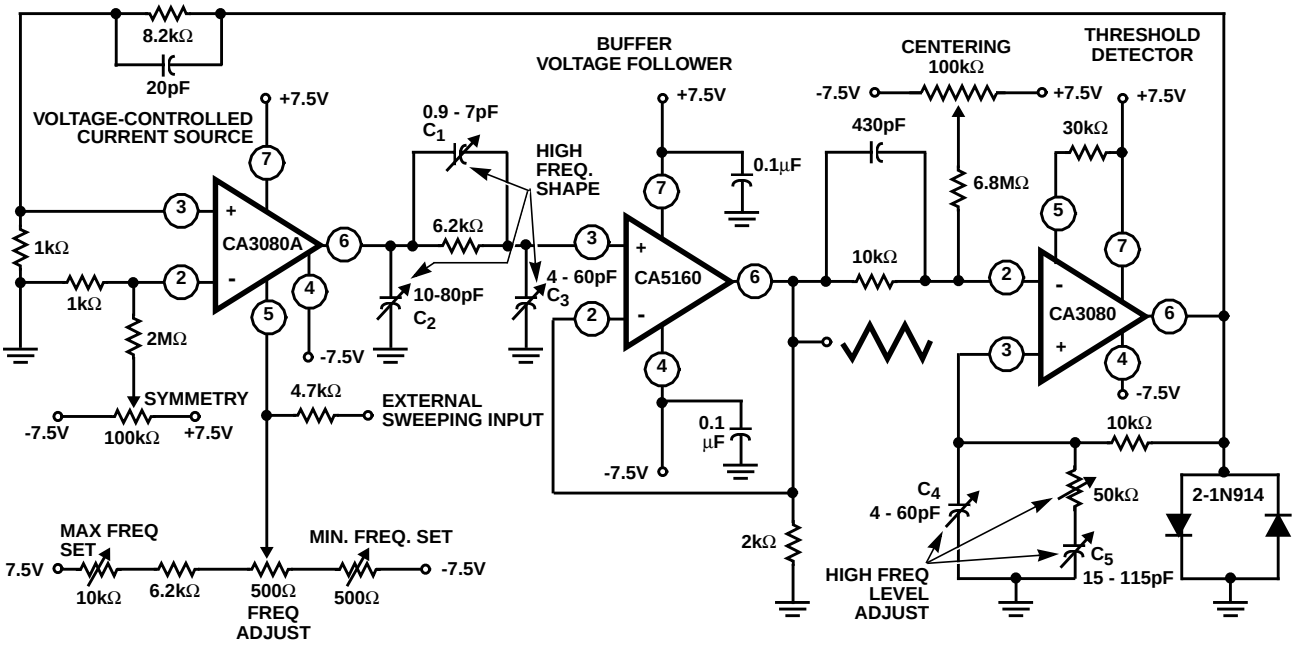
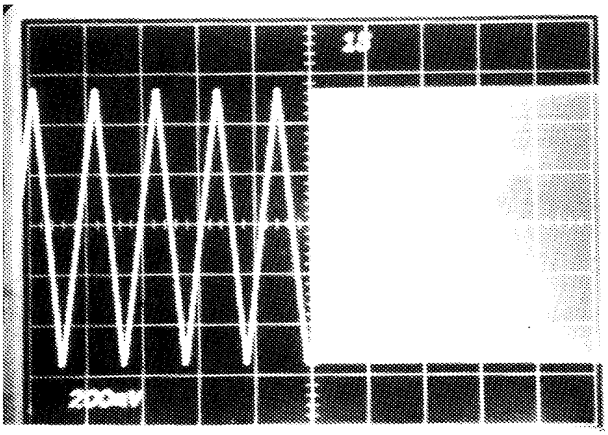
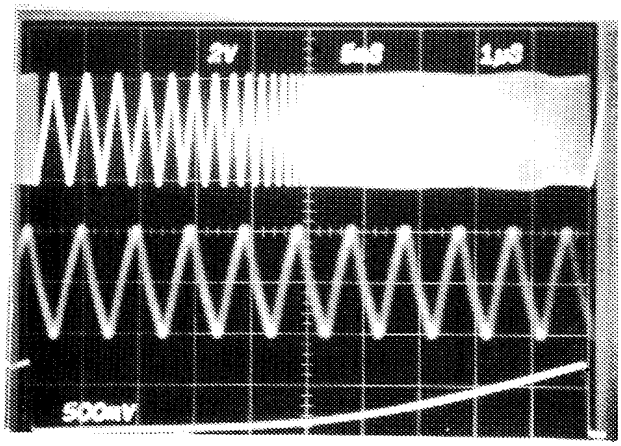


FIGURE 12A. FUNCTION GENERATOR CIRCUIT



NOTE: A square wave signal modulates the external sweeping input to produce 1Hz and 1MHz, showing the 1,000,000/1 frequency range of the function generator.

FIGURE 12B. TWO-TONE OUTPUT SIGNAL FROM THE FUNCTION GENERATOR



NOTE: The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1MHz signal via delayed oscilloscope triggering of the upper swept output signal.

FIGURE 12C. TRIPLE-TRACE OF THE FUNCTION GENERATOR SWEEPING TO 1MHz

FIGURE 12. CA5160 1,000,000/1 SINGLE CONTROL FUNCTION GENERATOR - 1MHz TO 1Hz

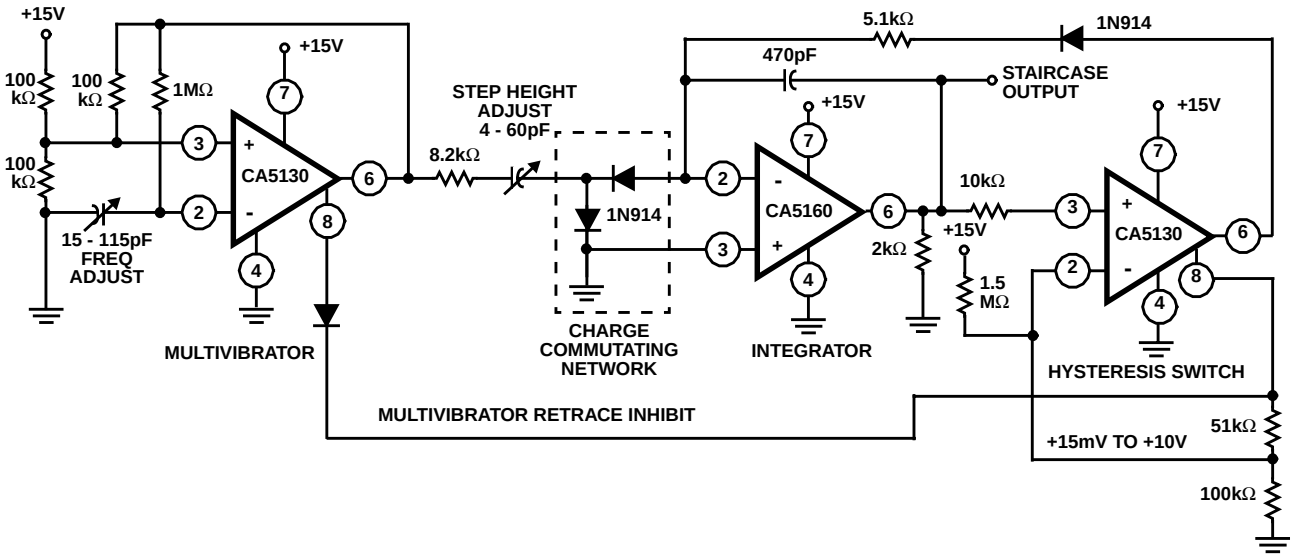
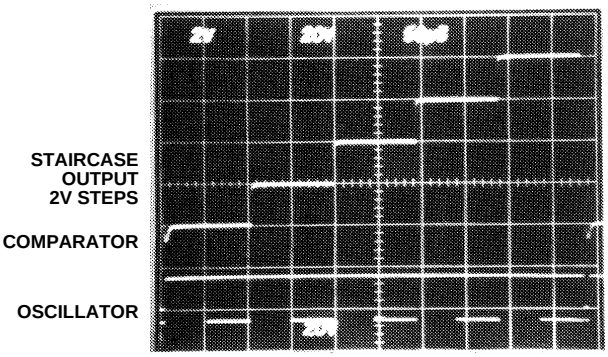


FIGURE 13A. STAIRCASE GENERATOR CIRCUIT



Top Trace: Staircase Output 2V Steps
Center Trace: Comparator
Bottom Trace: Oscillator

FIGURE 13B. STAIRCASE GENERATOR WAVEFORM

FIGURE 13. STAIRCASE GENERATOR CIRCUIT UTILIZING THREE CMOS OPERATIONAL AMPLIFIERS

Function Generator

A function generator having a wide tuning range is shown in Figure 12. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA5160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C_1, C_2, and C_3 shape the triangular signal between 500kHz and 1MHz. Capacitors C_4, C_5, and the trimmer potentiometer in series with C_5 maintain essentially constant (±10%) amplitude up to 1MHz.

Staircase Generator

Figure 13 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA5130s are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA5160, is used as a linear staircase generator.

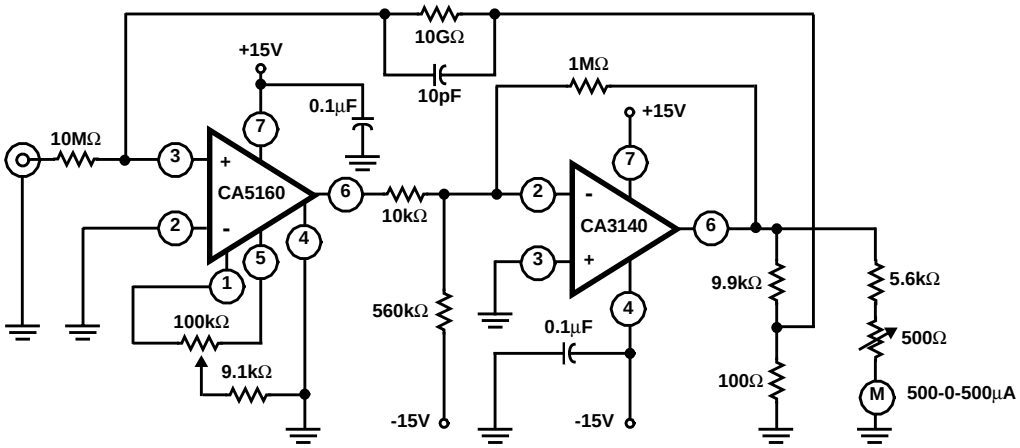


FIGURE 14. CURRENT-TO-VOLTAGE CONVERTER TO PROVIDE A PICOAMMETER WITH ±3pA FULL SCALE DEFLECTION

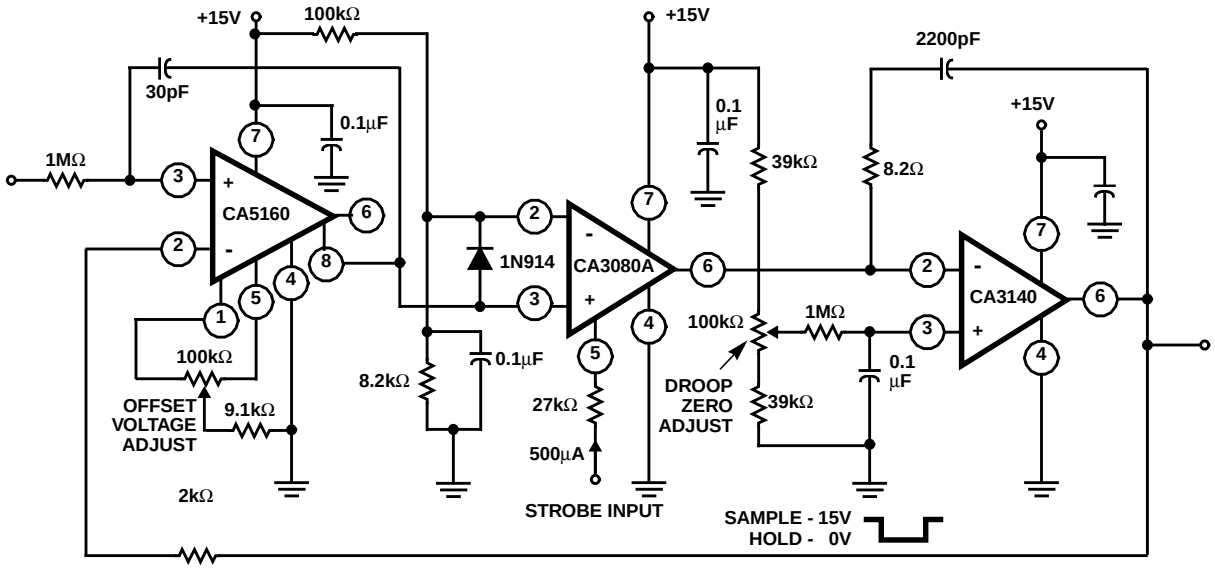
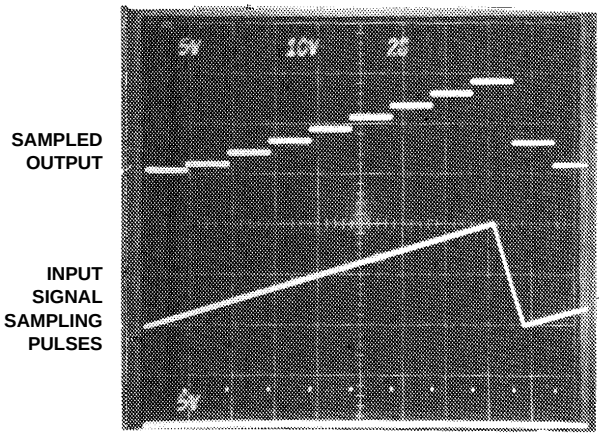
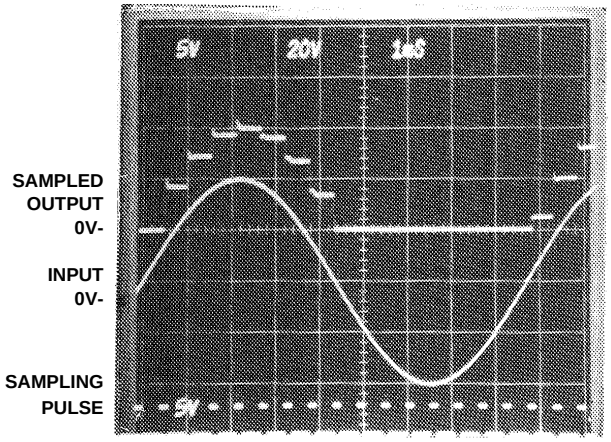


FIGURE 15A. SAMPLE AND HOLD CIRCUIT



Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

FIGURE 15B. SAMPLE AND HOLD WAVEFORM



Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulses

FIGURE 15C. SAMPLE AND HOLD WAVEFORM

FIGURE 15. SINGLE SUPPLY SAMPLE AND HOLD SYSTEM, INPUT 0V TO 10V

Picoammeter Circuit

Figure 14 is a current-to-voltage converter configuration utilizing a CA5160 and CA3140 to provide a picoampere meter for ±3pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA5160 at ground potential, the CA5160 input is operated in the “guarded mode”. Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in 0V across this leakage resistance, thus substantially reducing the leakage current.

If the CA5160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than 1pA level can be achieved as shown in Figure 1.

To further enhance the stability of this circuit, the CA5160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9kΩ resistor in series with a 100Ω resistor sets the voltage at the 10GΩ resistor (in series with Terminal 3) to ±30mV full-scale deflection. This 30mV signal results from ±3V appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9kΩ and 100Ω network similar to that used in the voltmeter circuit shown in Figure 11, a current range of 3pA

to 1nA full scale can be handled with the single 10GΩ resistor.

Single Supply Sample-and-Hold System

Figure 15 shows a single-supply sample-and-hold system using a CA5160 to provide a high input impedance and an input-voltage range of 0V to 10V. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse “droop” during the hold interval can be reduced to zero by adjusting the 100kΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320mV at the amplifier bias circuit (Terminal 5) at least ±100pA of output current will be available.

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA5160 is shown in Figure 16. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1V. The 500Ω potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

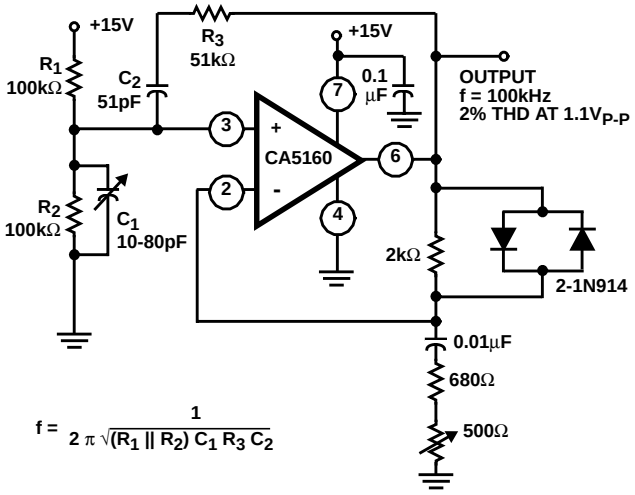
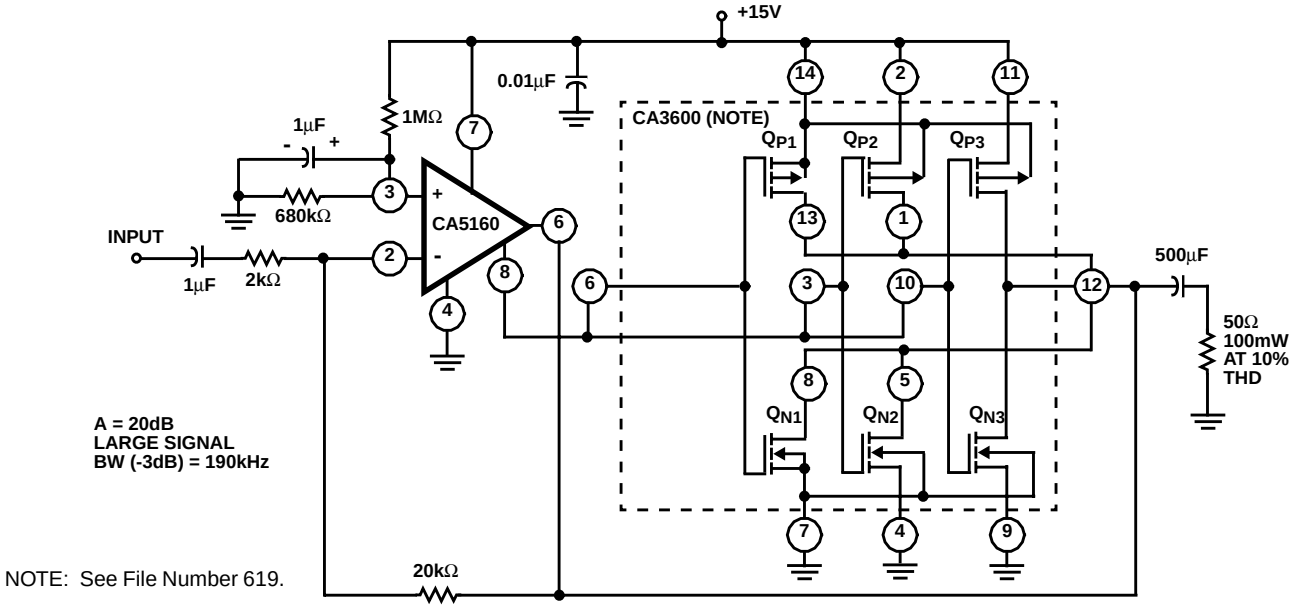


FIGURE 16. SINGLE-SUPPLY WEIN-BRIDGE OSCILLATOR

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA5160 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 17, three CMOS transistor-pairs in a single CA3600 lC array are shown parallel-connected with the output stage in the CA5160. In the Class A mode of CA3600E shown, a typical device consumes 20mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA5160 output stage by about 2.5X.

The amplifier circuit in Figure 17 employs feedback to establish a closed-loop gain of 20dB. The typical large-signal-bandwidth (-3dB) is 190kHz.



NOTE: See File Number 619.

FIGURE 17. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA5160.

Typical Performance Curves

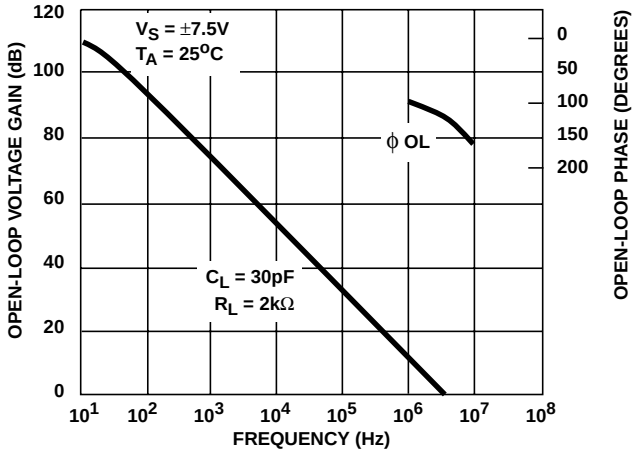


FIGURE 18. OPEN-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

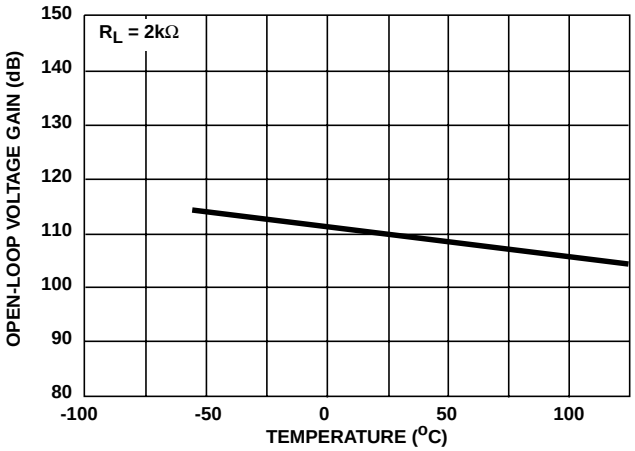


FIGURE 19. OPEN-LOOP GAIN vs TEMPERATURE

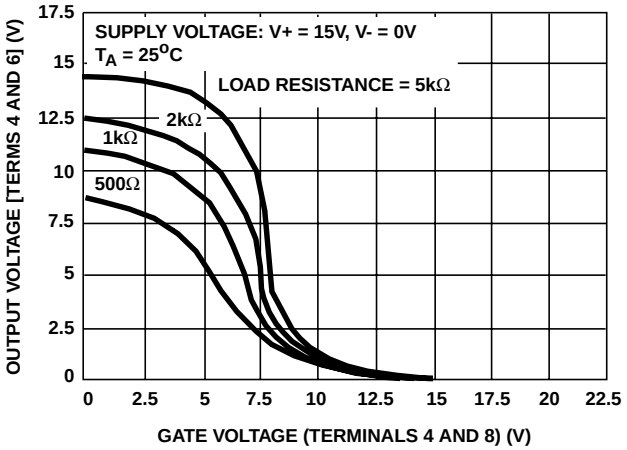


FIGURE 20. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

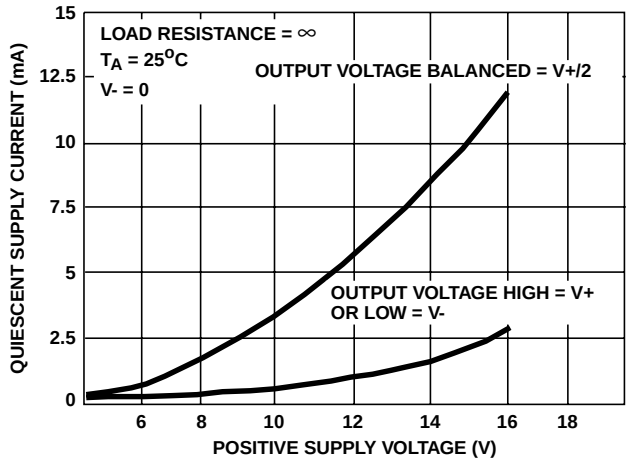


FIGURE 21. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

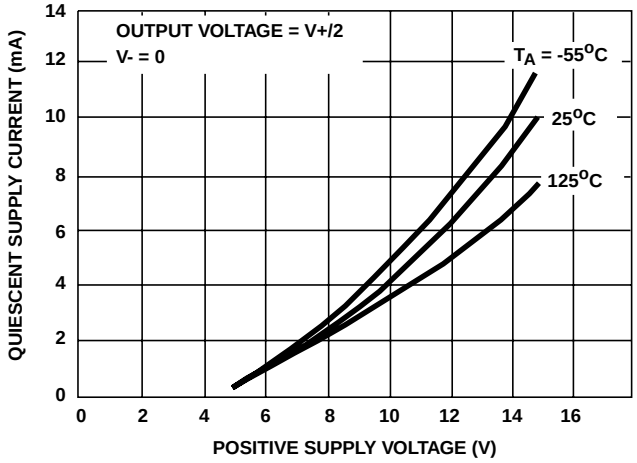


FIGURE 22. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

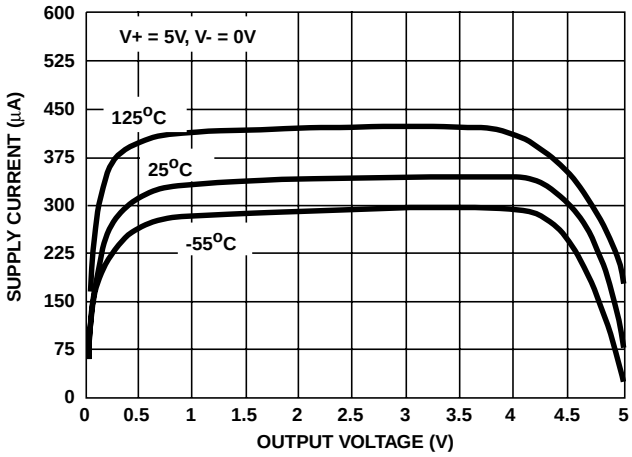


FIGURE 23. SUPPLY CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

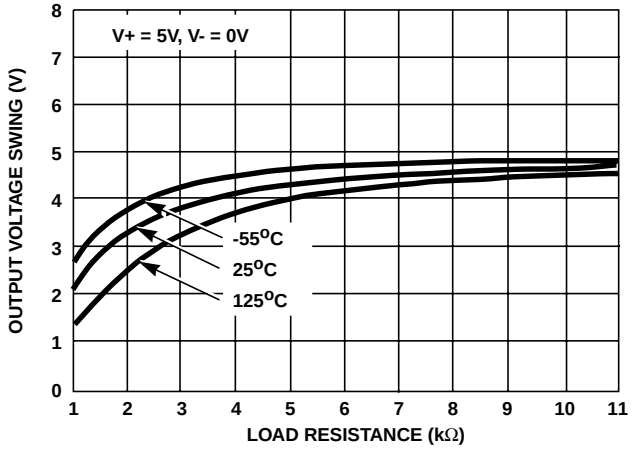


FIGURE 24. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

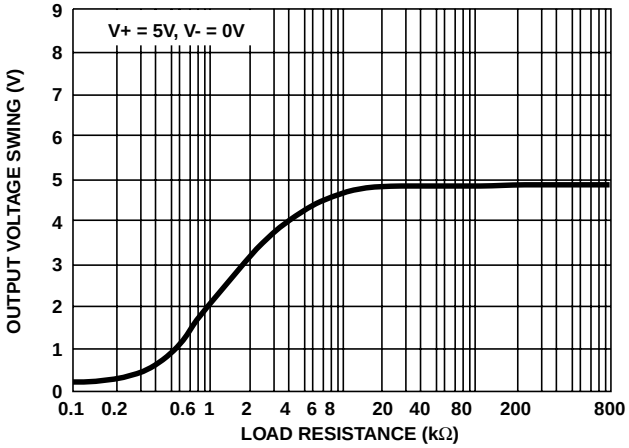


FIGURE 25. OUTPUT SWING vs LOAD RESISTANCE

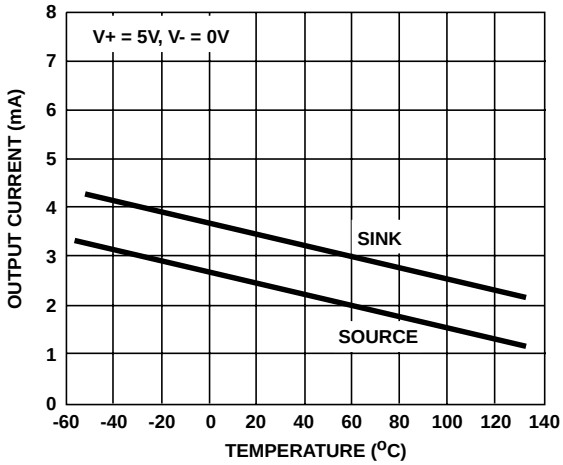


FIGURE 26. OUTPUT CURRENT vs TEMPERATURE

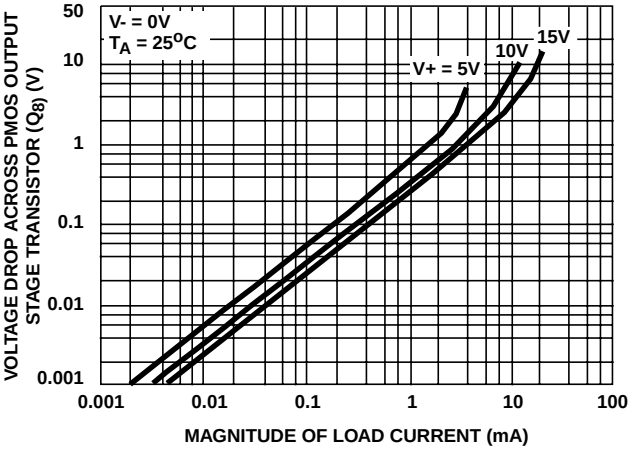


FIGURE 27. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q_8) vs LOAD CURRENT

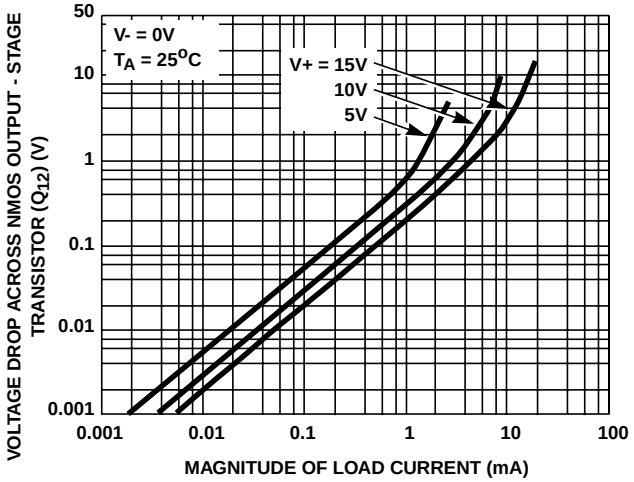


FIGURE 28. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q_{12}) vs LOAD CURRENT

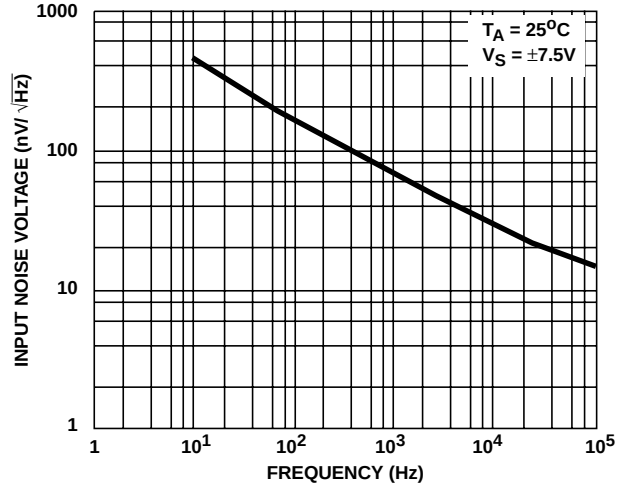
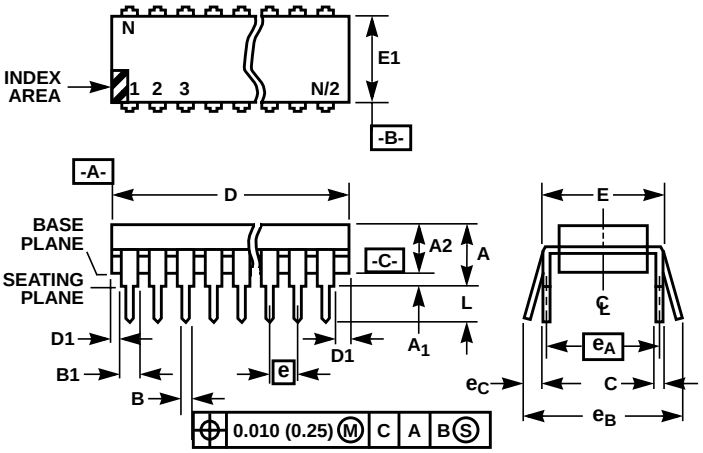


FIGURE 29. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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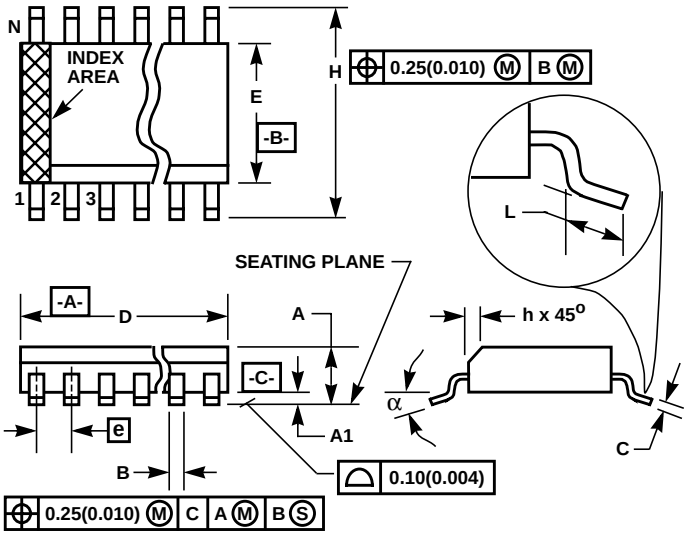
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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