

# BLF988; BLF988S

Power LDMOS transistor

Rev. 1 — 9 October 2012

Objective data sheet

## 1. Product profile

### 1.1 General description

A 600 W LDMOS RF power transistor for transmitter applications and industrial applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. Application information

Test signal	f (MHz)	$P_{L(AV)}$ (W)	$P_{L(M)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	IMD3 (dBc)
<b>RF performance in a common source 860 MHz narrowband test circuit</b>						
2-tone, class-AB	$f_1 = 860; f_2 = 860.1$	250	-	20	46	-32
pulsed, class-AB	860	-	600	20	58	-

### 1.2 Features and benefits

- Excellent ruggedness ( $V_{SWR} \geq 40 : 1$  through all phases)
- Optimum thermal behavior and reliability,  $R_{th(j-c)} = 0.15$  K/W
- High power gain
- High efficiency
- Designed for broadband operation (500 MHz to 1000 MHz)
- Internal input matching for high gain and optimum broadband operation
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

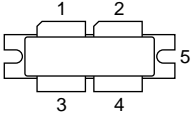
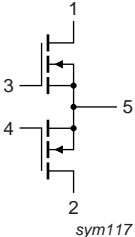
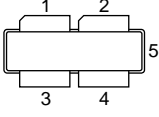
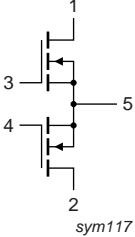
### 1.3 Applications

- Communication transmitter applications
- Industrial applications



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF988 (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF988S (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF988	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF988S	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	110	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_{L(AV)} = 250\text{ W}$	[1] 0.15	K/W

[1]  $R_{th(j-c)}$  is measured under RF conditions.

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.4\text{ mA}$	[1] 110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 240\text{ mA}$	[1] 1.4	1.9	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	36	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 8.5\text{ A}$	[1] -	143	-	$\text{m}\Omega$

[1]  $I_D$  is the drain current.

**Table 7. AC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	[1] -	220	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	74	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	1.2	-	pF

[1] Capacitance values without internal matching.

**Table 8. RF characteristics**

RF characteristics in NXP production narrowband test circuit;  $T_{case} = 25\text{ °C}$  unless otherwise specified.

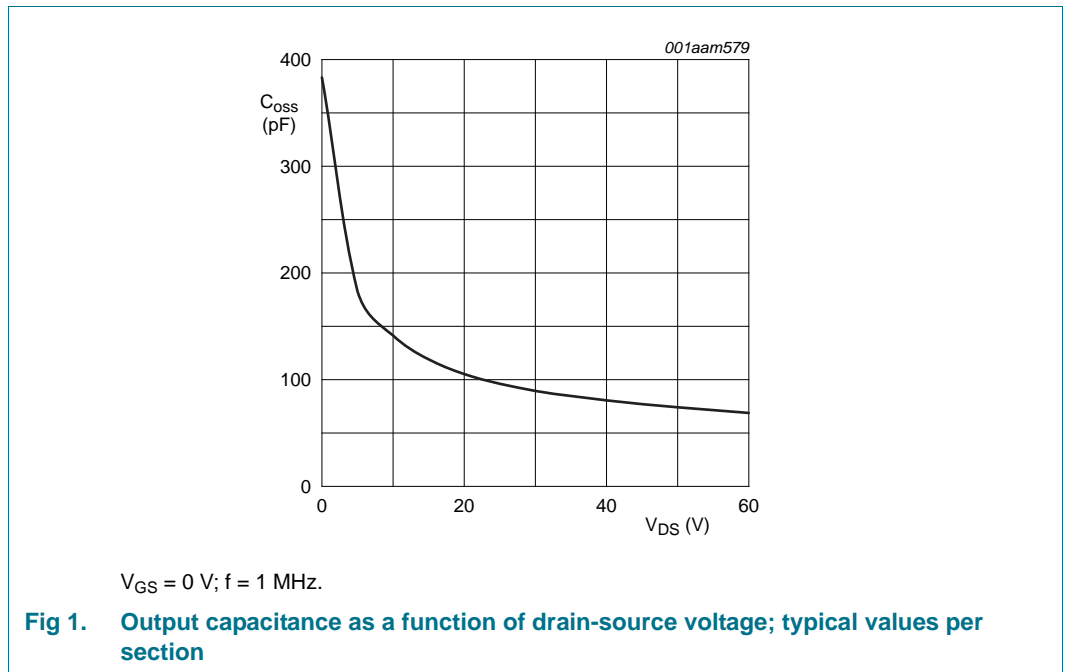
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>2-Tone, class-AB</b>						
$V_{DS}$	drain-source voltage		-	50	-	V
$I_{Dq}$	quiescent drain current		[1] -	1.3	-	A
$P_{L(AV)}$	average output power	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	250	-	-	W
$G_p$	power gain	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	19	20	-	dB
$\eta_D$	drain efficiency	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	42	46	-	%
IMD3	third-order intermodulation distortion	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	-	-32	-28	dBc

**Table 8. RF characteristics ...continued**

RF characteristics in NXP production narrowband test circuit;  $T_{case} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Pulsed, class-AB</b>						
$V_{DS}$	drain-source voltage		-	50	-	V
$I_{Dq}$	quiescent drain current		[1]	1.3	-	A
$P_{L(M)}$	peak output power	$f = 860\text{ MHz}$	-	600	-	W
$G_p$	power gain	$f = 860\text{ MHz}$	<td>	20	<td>	dB
$\eta_D$	drain efficiency	$f = 860\text{ MHz}$	<td>	58	-	%
$t_p$	pulse duration		-	100	-	$\mu\text{s}$
$\delta$	duty cycle		-	20	-	%

[1]  $I_{Dq}$  for total device



## 7. Test information

### 7.1 Impedance information

**Table 9. Typical push-pull impedance**

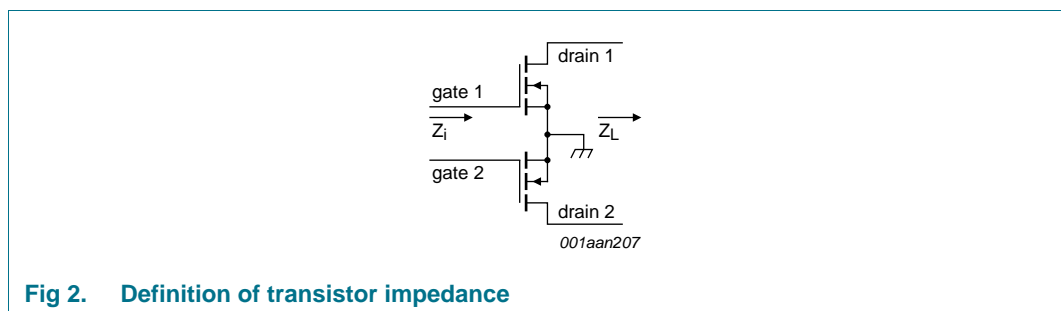
Simulated  $Z_i$  and  $Z_L$  device impedance; impedance info at  $V_{DS} = 50\text{ V}$  and  $P_{L(AV)} = 600\text{ W}$  (pulsed CW). See [Figure 2](#) for definition of transistor impedance.

f	$Z_i$	$Z_L$
MHz	$\Omega$	$\Omega$
300	$0.607 + j0$	$5.495 + j1.936$
325	$0.622 - j1.441$	$5.324 + j2.008$
350	$0.639 - j1.121$	$5.151 + j2.065$

**Table 9. Typical push-pull impedance ...continued**

Simulated  $Z_i$  and  $Z_L$  device impedance; impedance info at  $V_{DS} = 50\text{ V}$  and  $P_{L(AV)} = 600\text{ W}$  (pulsed CW). See [Figure 2](#) for definition of transistor impedance.

f MHz	$Z_i$ $\Omega$	$Z_L$ $\Omega$
375	0.658 – j0.826	4.977 + j2.107
400	0.679 – j0.551	4.805 + j2.136
425	0.703 – j0.291	4.634 + j2.153
450	0.73 – j0.044	4.466 + j2.157
475	0.76 + j0.194	4.301 + j2.151
500	0.793 + j0.424	4.14 + j2.134
525	0.83 + j0.648	3.984 + j2.109
550	0.872 + j0.869	3.833 + j2.075
575	0.919 + j1.088	3.687 + j2.033
600	0.972 + j1.305	3.546 + j1.985
625	1.032 + j1.523	3.411 + j1.931
650	1.101 + j1.741	3.281 + j1.871
675	1.179 + j1.963	3.156 + j1.807
700	1.268 + j2.187	3.036 + j1.738
725	1.371 + j2.416	2.922 + j1.666
750	1.49 + j2.651	2.813 + j1.591
775	1.629 + j2.891	2.708 + j1.512
800	1.792 + j3.138	2.609 + j1.432
825	1.984 + j3.39	2.514 + j1.349
850	2.212 + j3.649	2.423 + j1.264
875	2.484 + j3.91	2.336 + j1.178
900	2.812 + j4.17	2.254 + j1.091
925	3.209 + j4.421	2.175 + j1.003
950	3.689 + j4.648	2.1 + j0.913
975	4.27 + j4.829	2.029 + j0.823
1000	4.967 + j4.927	1.96 + j0.733



**Fig 2. Definition of transistor impedance**

## 7.2 Test circuit information

**Table 10. List of components**

For test circuit, see [Figure 3](#), [Figure 4](#) and [Figure 5](#).

Component	Description	Value	Remarks
B1, B2	semi rigid coax	25 $\Omega$ ; 49.5 mm	UT-090C-25 (EZ 90-25)
C1	multilayer ceramic chip capacitor	12 pF	[1]
C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	8.2 pF	[1]
C7	multilayer ceramic chip capacitor	6.8 pF	[2]
C8	multilayer ceramic chip capacitor	2.7 pF	[2]
C9	multilayer ceramic chip capacitor	2.2 pF	[2]
C10, C13, C14	multilayer ceramic chip capacitor	100 pF	[3]
C11, C12	multilayer ceramic chip capacitor	10 pF	[2]
C15, C16	multilayer ceramic chip capacitor	4.7 $\mu$ F, 50 V	Kemet C1210X475K5RAC-TU or capacitor of same quality.
C17, C18, C23, C24	multilayer ceramic chip capacitor	100 pF	[2]
C19, C20	multilayer ceramic chip capacitor	10 $\mu$ F, 50 V	TDK C570X7R1H106KT000N or capacitor of same quality.
C21, C22	electrolytic capacitor	470 $\mu$ F; 63 V	
C30	multilayer ceramic chip capacitor	10 pF	[4]
C31	multilayer ceramic chip capacitor	9.1 pF	[4]
C32	multilayer ceramic chip capacitor	3.9 pF	[4]
C33, C34, C35	multilayer ceramic chip capacitor	100 pF	[4]
C36, C37	multilayer ceramic chip capacitor	4.7 $\mu$ F, 50 V	TDK C4532X7R1E475MT020U or capacitor of same quality.
L1	microstrip	-	[5] (W $\times$ L) 15 mm $\times$ 13 mm
L2	microstrip	-	[5] (W $\times$ L) 5 mm $\times$ 26 mm
L3, L32	microstrip	-	[5] (W $\times$ L) 2 mm $\times$ 49.5 mm
L4	microstrip	-	[5] (W $\times$ L) 1.7 mm $\times$ 3.5 mm
L5	microstrip	-	[5] (W $\times$ L) 2 mm $\times$ 9.5 mm
L30	microstrip	-	[5] (W $\times$ L) 5 mm $\times$ 13 mm
L31	microstrip	-	[5] (W $\times$ L) 2 mm $\times$ 11 mm
L33	microstrip	-	[5] (W $\times$ L) 2 mm $\times$ 3 mm
R1, R2	wire resistor	10 $\Omega$	
R3, R4	SMD resistor	5.6 $\Omega$	0805
R5, R6	wire resistor	100 $\Omega$	
R7, R8	potentiometer	10 k $\Omega$	

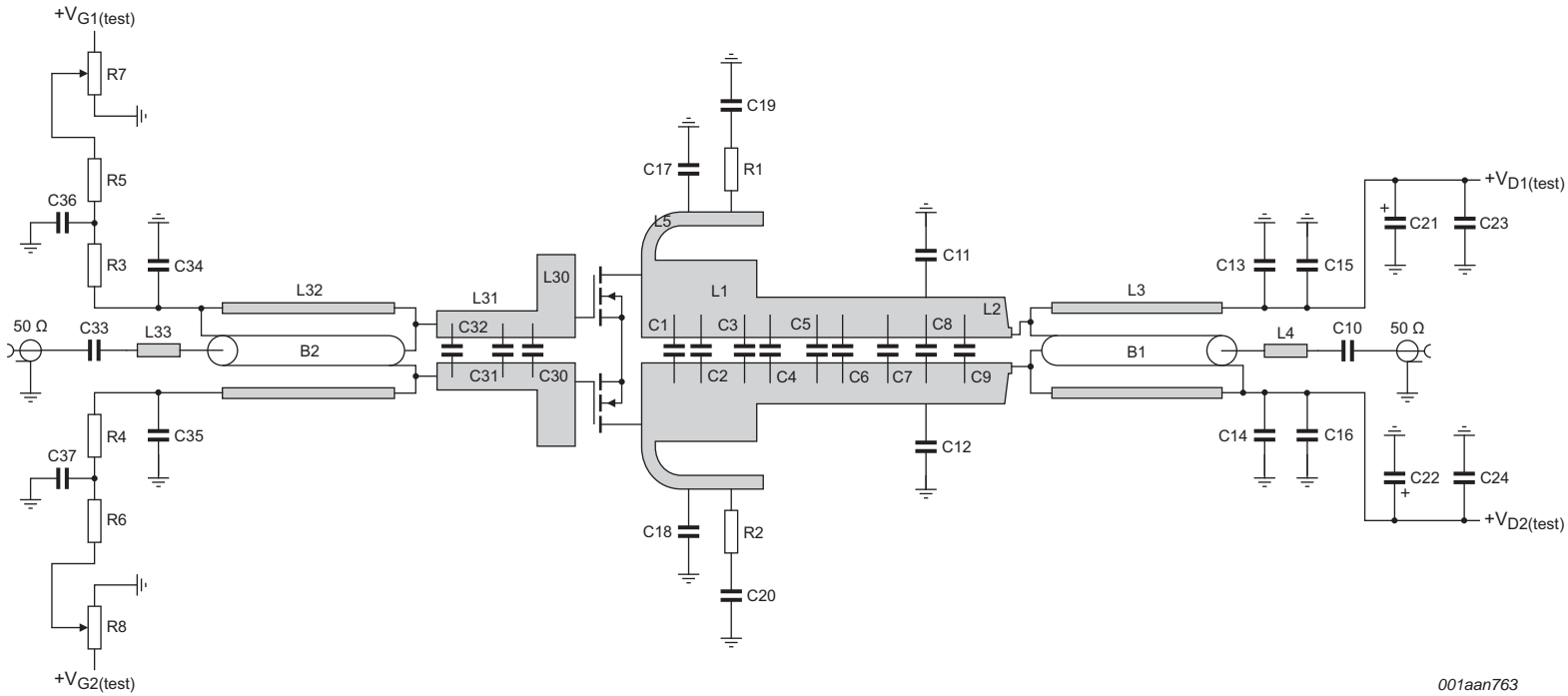
[1] American technical ceramics type 800R or capacitor of same quality.

[2] American technical ceramics type 800B or capacitor of same quality.

[3] American technical ceramics type 180R or capacitor of same quality.

[4] American technical ceramics type 100A or capacitor of same quality.

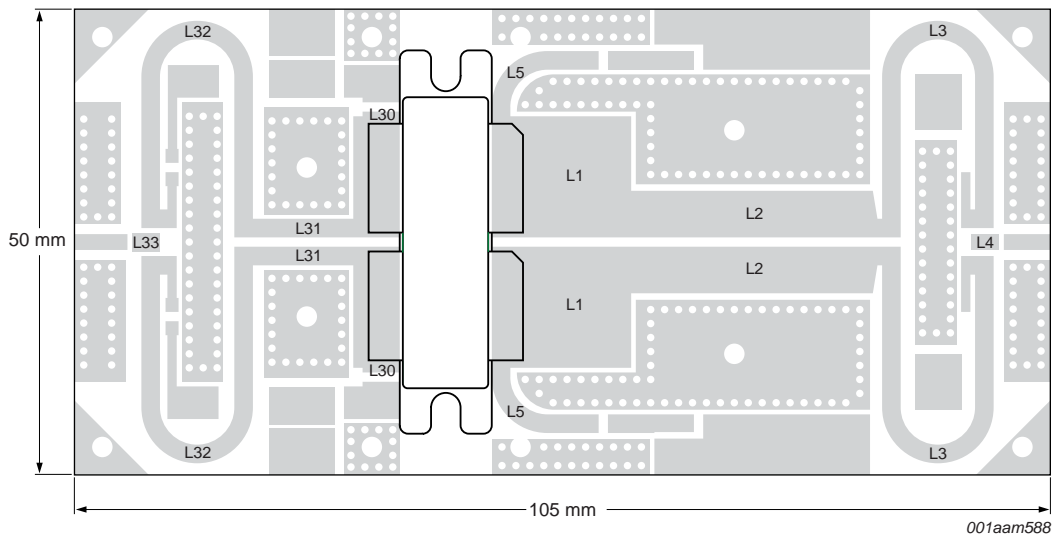
[5] Printed-Circuit Board (PCB): Taconic RF35;  $\epsilon_r = 3.5$  F/m; height = 0.762 mm; Cu (top/bottom metallization); thickness copper plating = 35  $\mu$ m.



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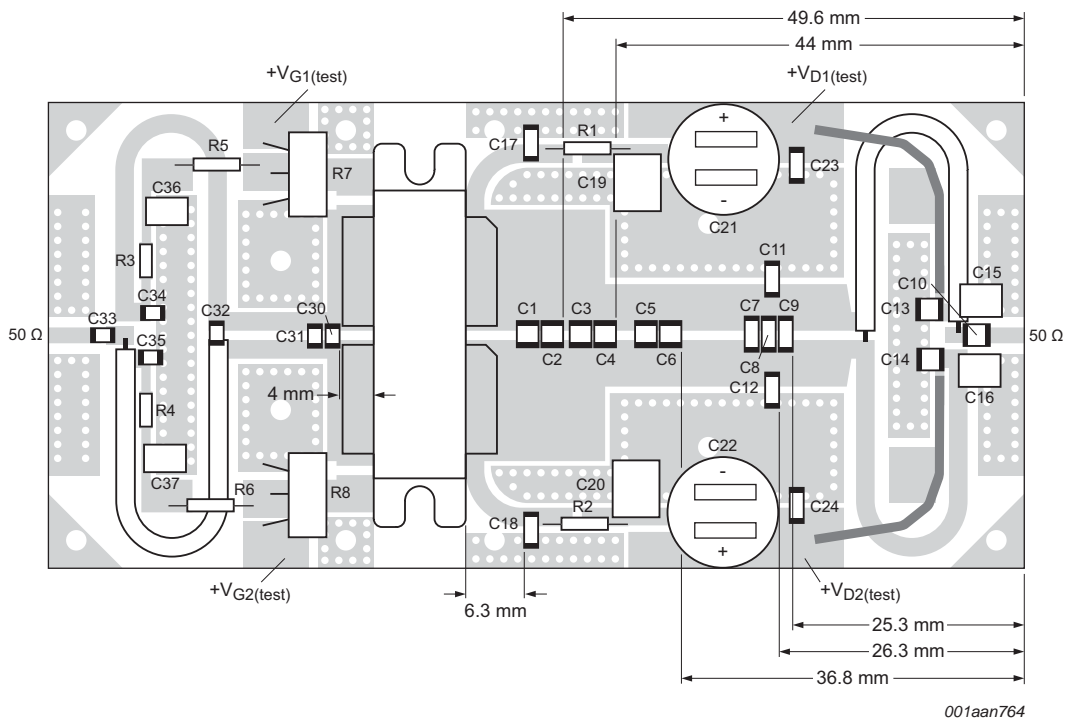
See [Table 10](#) for a list of components.

**Fig 3. Class-AB common source broadband amplifier;  $V_{D1(test)}$ ,  $V_{D2(test)}$ ,  $V_{G1(test)}$  and  $V_{G2(test)}$  are drain and gate test voltages**



See [Table 10](#) for a list of components.

**Fig 4. Printed-Circuit Board (PCB) for class-AB common source amplifier**



See [Table 10](#) for a list of components.

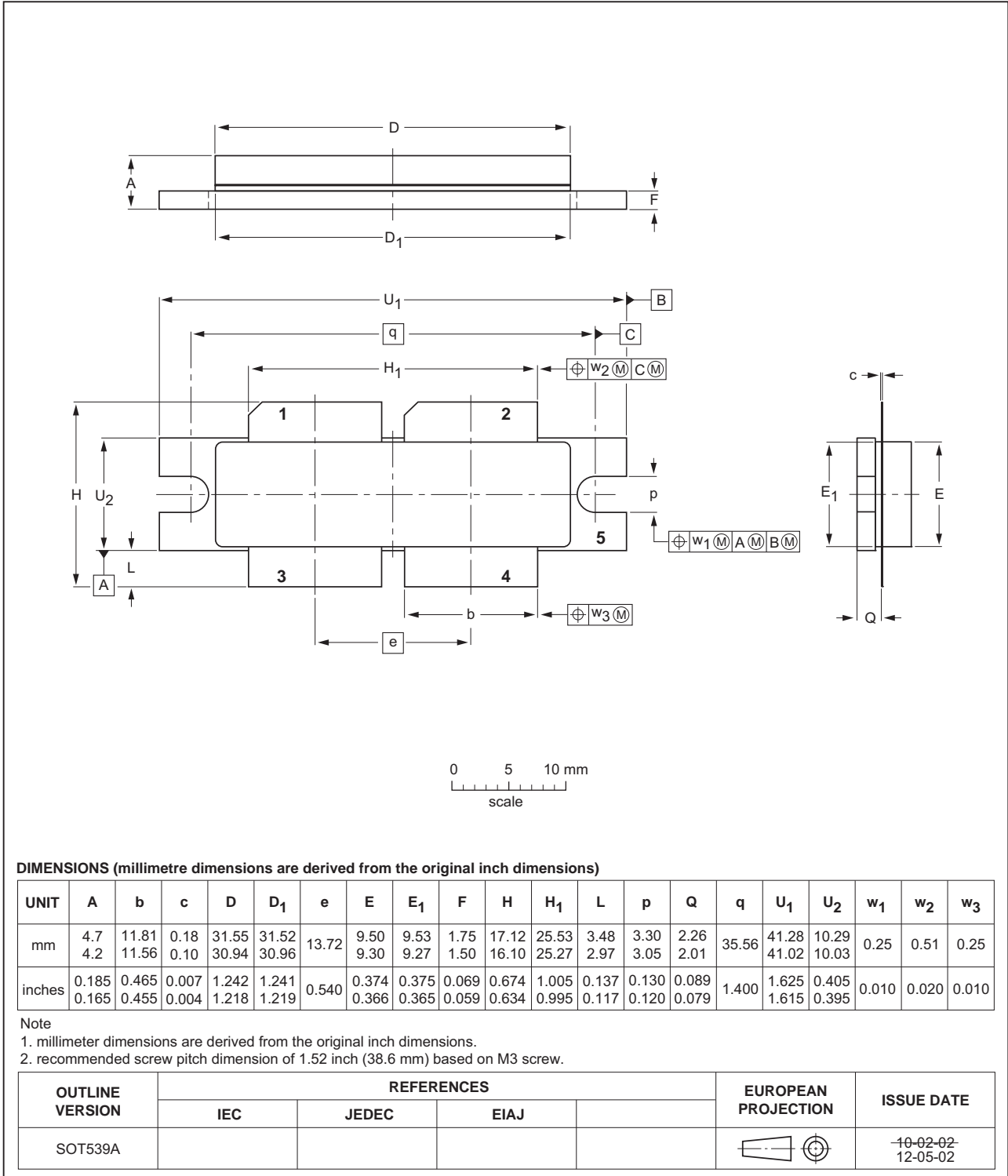
**Fig 5. Component layout for class-AB common source amplifier**



**8. Package outline**

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A



**Fig 6. Package outline SOT539A**

Earless flanged balanced ceramic package; 4 leads

SOT539B

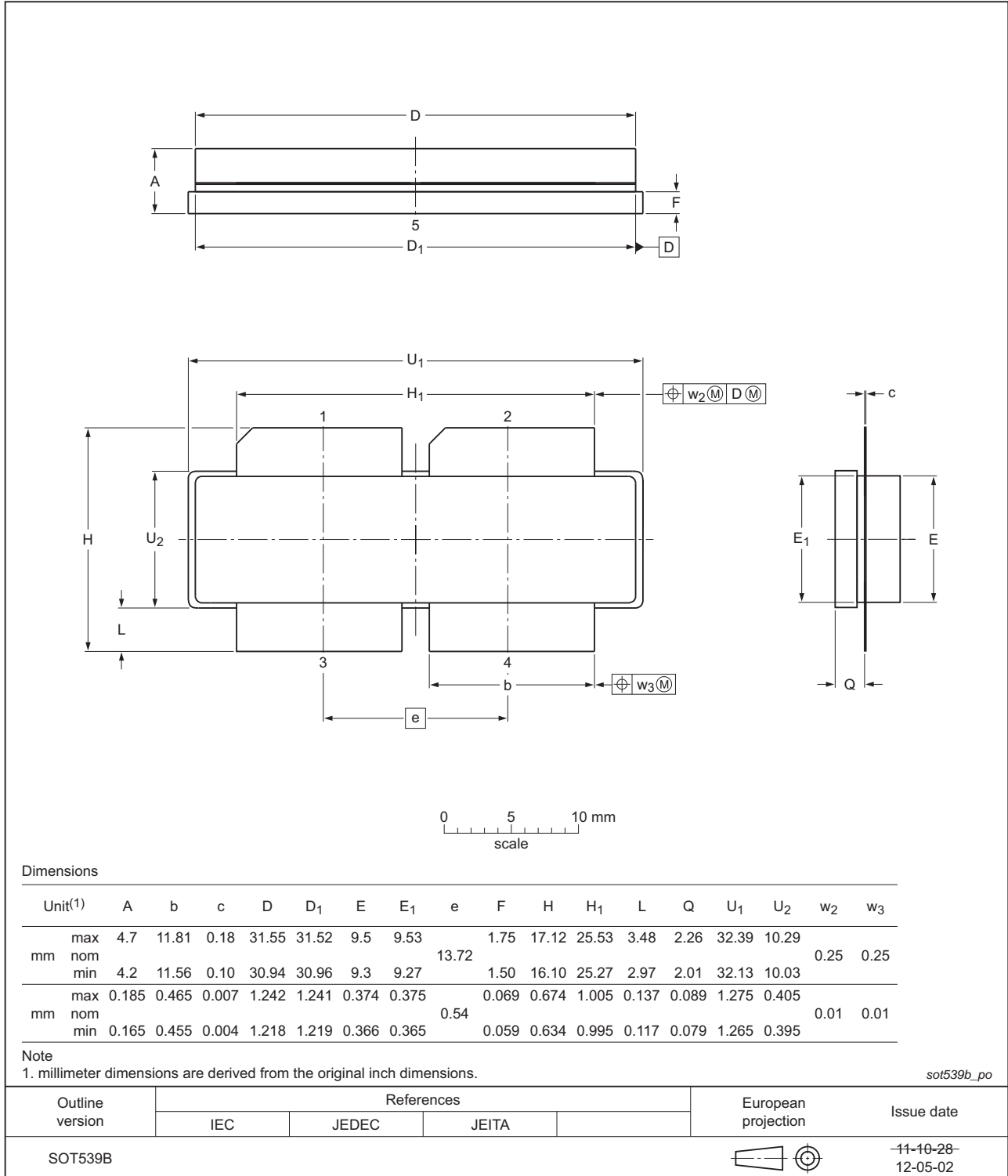


Fig 7. Package outline SOT539B

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF988_BLF988S v.1	20121009	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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