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National Semiconductor

January 11, 2008

LP3996
Dual Linear Regulator with 300mA and 150mA Outputs and Power-On-Reset

General Description

The LP3996 is a dual low dropout regulator with power-on-reset circuit. The first regulator can source 150mA, while the second is capable of sourcing 300mA and has a power-on-reset function included.

The LP3996 provides 1.5% accuracy requiring an ultra low quiescent current of 35µA. Separate enable pins allow each output of the LP3996 to be shut down, drawing virtually zero current.

The LP3996 is designed to be stable with small footprint ceramic capacitors down to 1µF. An external capacitor may be used to set the POR delay time as required.

The LP3996 is available in fixed output voltages and comes in a 10 pin, 3mm x 3mm, LLP package. .

Features

- 2 LDO Outputs with Independent Enable
- 1.5% Accuracy at Room Temperature, 3% over Temperature
- Power-On-Reset Function with Adjustable Delay
- Thermal Shutdown Protection
- Stable with Ceramic Capacitors

Key Specifications

■ Input Voltage Range	2.0V to 6.0V
■ Low Dropout Voltage	210mV at 300mA
■ Ultra-Low I_Q (enabled)	35µA
■ Virtually Zero I_Q (disabled)	<10nA

Package

All available in Lead Free option.

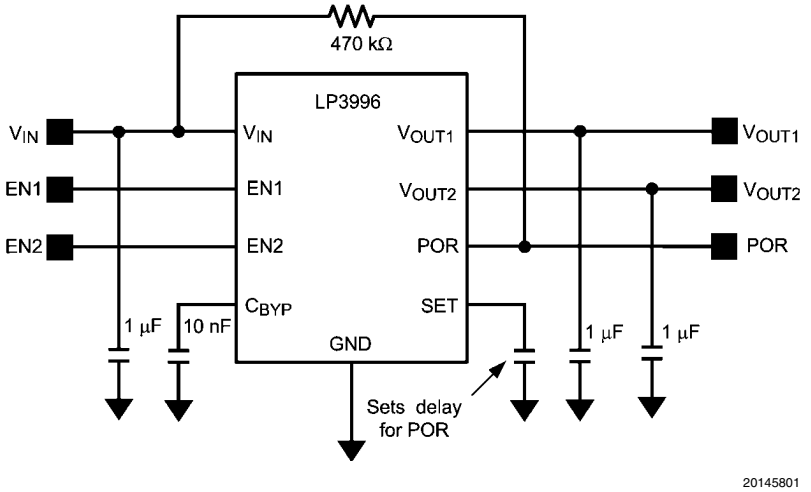
10 pin LLP 3mm x 3mm

For other package options contact your NSC sales office.

Applications

- Cellular Handsets
- PDA's
- Wireless Network Adaptors

Typical Application Circuit



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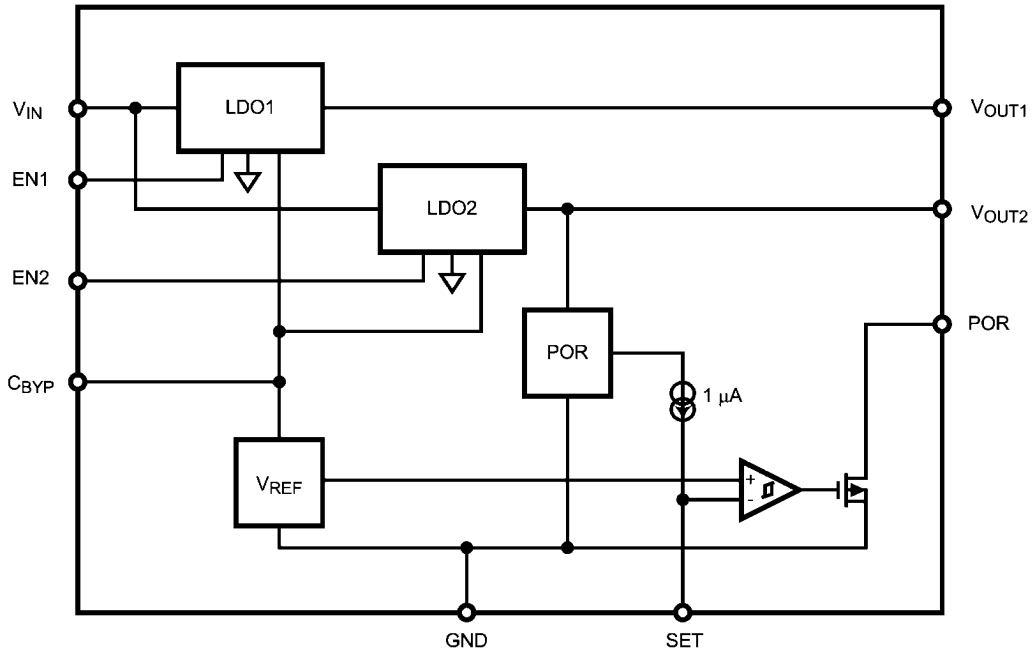
Functional Block Diagram



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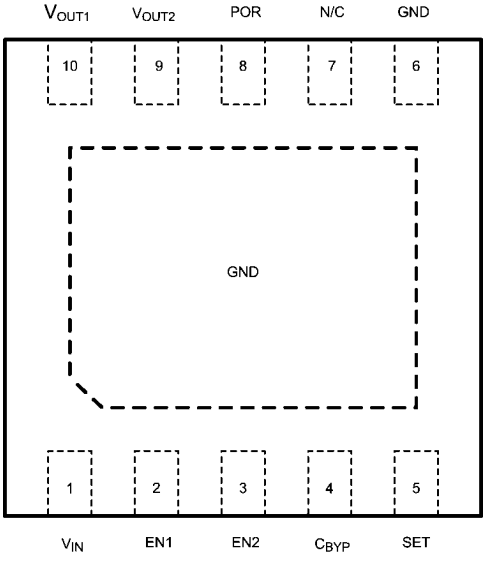
Pin Descriptions

LLP-10 Package

Pin No	Symbol	Name and Function
1	V_{IN}	Voltage Supply Input. Connect a 1µF capacitor between this pin and GND.
2	EN1	Enable Input to Regulator 1. Active high input. High = On. Low = OFF.
3	EN2	Enable Input to Regulator 2. Active high input. High = On. Low = OFF.
4	C_{BYP}	Internal Voltage Reference Bypass. Connect a 10nF capacitor from this pin to GND to reduce output noise and improve line transient and PSRR. This pin may be left open.
5	SET	Set Delay Input. Connect a capacitor between this pin and GND to set the POR delay time. If left open, there will be no delay.
6	GND	Common Ground pin. Connect externally to exposed pad.
7	N/C	No Connection. Do not connect to any other pin.
8	POR	Power-On Reset Output. Open drain output. Active low indicates under-voltage output on Regulator 2. A pull-up resistor is required for correct operation.
9	V_{OUT2}	Output of Regulator 2. 300mA maximum current output. Connect a 1µF capacitor between this pin and GND.
10	V_{OUT1}	Output of Regulator 1. 150mA maximum current output. Connect a 1µF capacitor between this pin and GND.
Pad	GND	Common Ground. Connect to Pin 6.

Connection Diagram

LLP-10 Package



Top View

20145803

See NS package number SDA10A

Ordering Information (LLP-10)

For other voltage options, please contact your local NSC sales office

* These parts avaliable soon.

Output Voltage (V)		Order Number	Spec	Package Marking	Supplied As
Vout1	Vout2				
0.8	3.3	LP3996SD-0833	NOPB	L167B	1000 Units, Tape-and-Reel
		LP3996SDX-0833	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-0833			1000 Units, Tape-and-Reel
		LP3996SDX-0833			4500 Units, Tape-and-Reel
1.0	1.8	LP3996SD-1018	NOPB	L227B	1000 Units, Tape-and-Reel
		LP3996SDX-1018	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-1018			1000 Units, Tape-and-Reel
		LP3996SDX-1018			4500 Units, Tape-and-Reel
1.5	2.5	LP3996SD-1525	NOPB	L168B	1000 Units, Tape-and-Reel
		LP3996SDX-1525	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-1525			1000 Units, Tape-and-Reel
		LP3996SDX-1525			4500 Units, Tape-and-Reel
1.8	3.3	LP3996SD-1833	NOPB	L228B	1000 Units, Tape-and-Reel
		LP3996SDX-1833	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-1833			1000 Units, Tape-and-Reel
		LP3996SDX-1833			4500 Units, Tape-and-Reel
2.5	3.3	LP3996SD-2533	NOPB	L229B	1000 Units, Tape-and-Reel
		LP3996SDX-2533	NOPB		4500 Units, Tape-and-Reel
		LP3996SDX-2533			1000 Units, Tape-and-Reel
		LP3996SD-2533			4500 Units, Tape-and-Reel
2.8	2.8	LP3996SD-2828	NOPB	L171B	1000 Units, Tape-and-Reel
		LP3996SDX-2828	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-2828			1000 Units, Tape-and-Reel
		LP3996SDX-2828			4500 Units, Tape-and-Reel
3.0	3.0	LP3996SD-3030	NOPB	L172B	1000 Units, Tape-and-Reel
		LP3996SDX-3030	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-3030			1000 Units, Tape-and-Reel
		LP3996SDX-3030			4500 Units, Tape-and-Reel
3.0	3.3	LP3996SD-3033	NOPB	L170B	1000 Units, Tape-and-Reel
		LP3996SDX-3033	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-3033			1000 Units, Tape-and-Reel
		LP3996SDX-3033			4500 Units, Tape-and-Reel
3.3	0.8	LP3996SD-3308	NOPB	L188B	1000 Units, Tape-and-Reel
		LP3996SDX-3308	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-3308			1000 Units, Tape-and-Reel
		LP3996SDX-3308			4500 Units, Tape-and-Reel
3.3	3.3	LP3996SD-3333	NOPB	L173B	1000 Units, Tape-and-Reel
		LP3996SDX-3333	NOPB		4500 Units, Tape-and-Reel
		LP3996SD-3333			1000 Units, Tape-and-Reel
		LP3996SDX-3333			4500 Units, Tape-and-Reel

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage to GND	-0.3V to 6.5V
V_{OUT1}, V_{OUT2} EN1 and EN2 Voltage to GND	-0.3V to (V_{IN} + 0.3V) with 6.5V (max)
POR to GND	-0.3V to 6.5V
Junction Temperature (T_{J-MAX})	150°C
Lead/Pad Temp. (Note 3)	235°C
Storage Temperature	-65°C to 150°C
Continuous Power Dissipation Internally Limited(Note 4)	
ESD Rating(Note 5)	
Human Body Model	2.0kV
Machine Model	200V

Operating Ratings (Notes 1, 2)

Input Voltage	2.0V to 6.0V
EN1, EN2, POR Voltage	0 to (V_{IN} + 0.3V) to 6.0V (max)
Junction Temperature	-40°C to 125°C
Ambient Temperature T_ARange (Note 6)	-40°C to 85°C

Thermal Properties (Note 1)

Junction To Ambient Thermal Resistance(Note 7)	
θ_{JA}LLP-10 Package	55°C/W

Electrical Characteristics (Notes 2, 8)

Unless otherwise noted, V_{EN} = 950mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT1} = C_{OUT2} = 1.0µF.

Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, –40 to +125°C.

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
V_{IN}	Input Voltage	(Note 9)			2	6	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA	1.5V < V_{OUT} ≤ 3.3V		-2.5 **-3.75**	+2.5 **+3.75**	%
			V_{OUT} ≤ 1.5V		-2.75 **-4**	+2.75 **+4**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 6.0V		0.03		**0.3**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 150mA (LDO 1)		85		**155**	µV/mA
		I_{OUT} = 1mA to 300mA (LDO 2)		26		**85**	
V_{DO}	Dropout Voltage (Note 10)	I_{OUT} = 1mA to 150mA (LDO 1)		110		**220**	mV
		I_{OUT} = 1mA to 300mA (LDO 2)		210		**550**	
I_Q	Quiescent Current	LDO 1 ON, LDO 2 ON I_{OUT1}= I_{OUT2} = 0mA		35		**100**	µA
		LDO 1 ON, LDO 2 OFF I_{OUT1} = 150mA		45		**110**	
		LDO 1 OFF, LDO 2 ON I_{OUT2} = 300mA		45		**110**	
		LDO 1 ON, LDO 2 ON I_{OUT1} = 150mA, I_{OUT2} = 300mA		70		**170**	
		V_{EN1} = V_{EN2} = 0.4V		0.5		**10**	nA
I_{SC}	Short Circuit Current Limit	LDO 1		420		**750**	mA
		LDO 2		550		**840**	
I_{OUT}	Maximum Output Current	LDO 1			**150**		mA
		LDO 2			**300**		

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
PSRR	Power Supply Rejection Ratio (Note 11)	f = 1kHz, I_{OUT} = 1mA to 150mA C_{BYP} = 10nF	LDO1	58			dB
			LDO2	70			
		f = 20kHz, I_{OUT} = 1mA to 150mA C_{BYP} = 10nF	LDO1	45			
			LDO2	60			
e_n	Output noise Voltage (Note 11)	BW = 10Hz to 100kHz C_{BYP} = 10nF	V_{OUT} = 0.8V	36			μV_{RMS}
			V_{OUT} = 3.3V	75			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		160			°C
		Hysteresis		20			
Enable Control Characteristics							
I_{EN}	Input Current at V_{EN1} or V_{EN2}	V_{EN} = 0.0V		0.005		**0.1**	µA
		V_{EN} = 6V		2		**5**	
V_{IL}	Low Input Threshold at V_{EN1} or V_{EN2}					**0.4**	V
V_{IH}	High Input Threshold at V_{EN1} or V_{EN2}				**0.95**		V
POR Output Characteristics							
V_{TH}	Low Threshold % 0f $V_{OUT2\ (NOM)}$	Flag ON			88		%
	High Threshold % 0f $V_{OUT2\ (NOM)}$	Flag OFF				96	
I_{POR}	Leakage Current	Flag OFF, V_{POR} = 6.5V		30			nA
V_{OL}	Flag Output Low Voltage	I_{SINK} = 250µA		20			mV
Timing Characteristics							
T_{ON}	Turn On Time (Note 11)	To 95% Level C_{BYP} = 10nF		300			µs
Transient Response	Line Transient Response $\lvert\delta V_{OUT}\rvert$ (Note 11)	$T_{rise} = T_{fall}$ = 10µs δV_{IN} = 1VC_{BYP} = 10nF		20			mV (pk - pk)
	Load Transient Response $\lvert\delta V_{OUT}\rvert$ (Note 11)	$T_{rise} = T_{fall}$ = 1µs	LDO 1 I_{OUT} = 1mA to 150mA	175			
			LDO 2 I_{OUT} = 1mA to 300mA	150			
SET Input Characteristics							
I_{SET}	SET Pin Current Source	V_{SET} = 0V		1.3			µA
$V_{TH(SET)}$	SET Pin Threshold Voltage	POR = High		1.25			V

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN-1187, Leadless Leadframe Package.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 5: The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 6: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 7: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 8: Min Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: $V_{IN(MIN)} = V_{OUT(NOM)}$ + 0.5V, or 2.0V, whichever is higher.

Note 10: Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V

Note 11: This electrical specification is guaranteed by design.

Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance (Note 12)	1.0	**0.7**		µF
		ESR		5	500	mΩ

Note 12: The Capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor is X7R. However, depending on the application, X5R, Y5V and Z5U can also be used. (See capacitor section in Applications Hints).

Transient Test Conditions

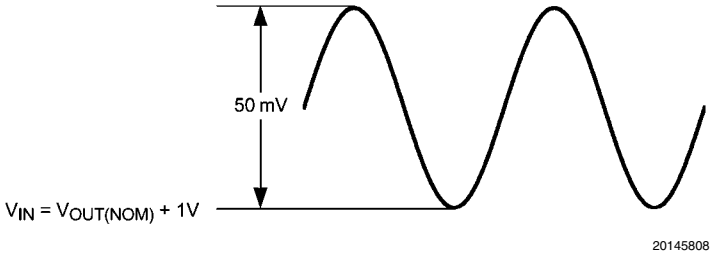


FIGURE 1. PSRR Input Signal

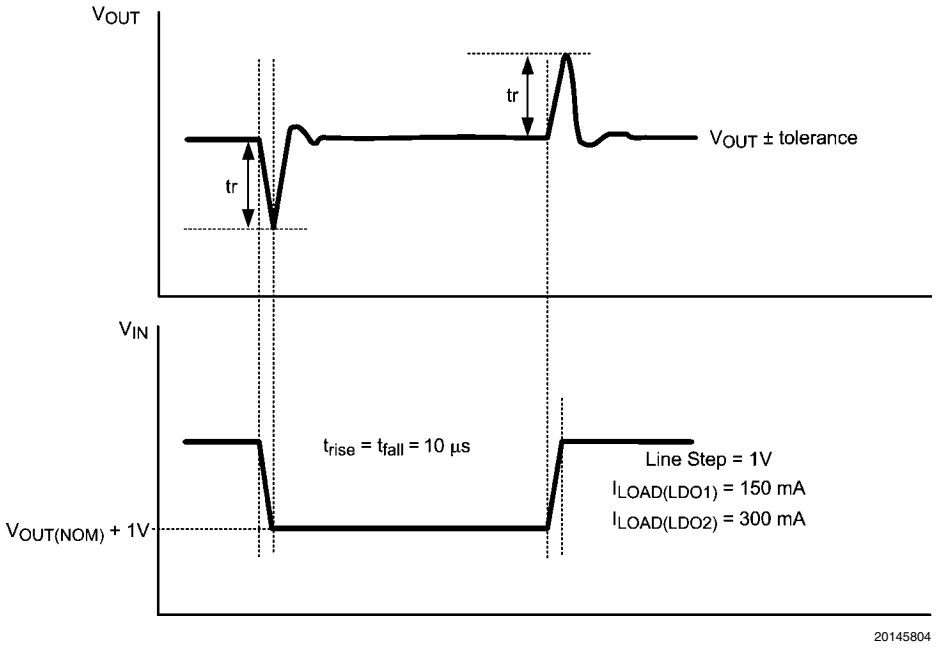


FIGURE 2. Line Transient Input Test Signal

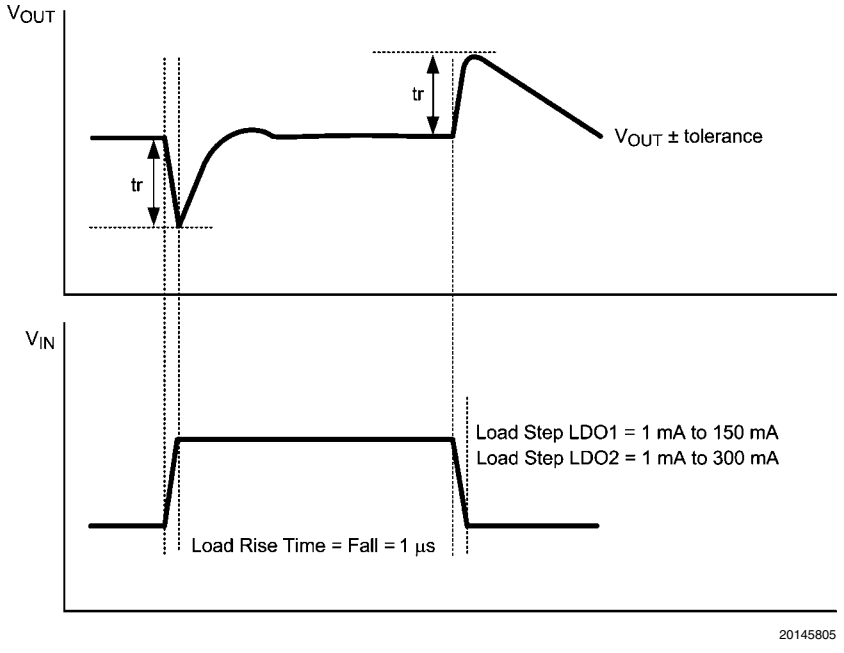
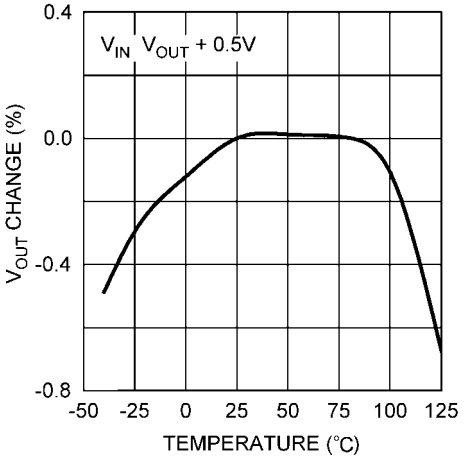


FIGURE 3. Load Transient Input Signal

Typical Performance Characteristics.

Unless otherwise specified, C_{IN} = 1.0µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0µF Ceramic, C_{BYP} = 10nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25°C, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}.

Output Voltage Change vs Temperature



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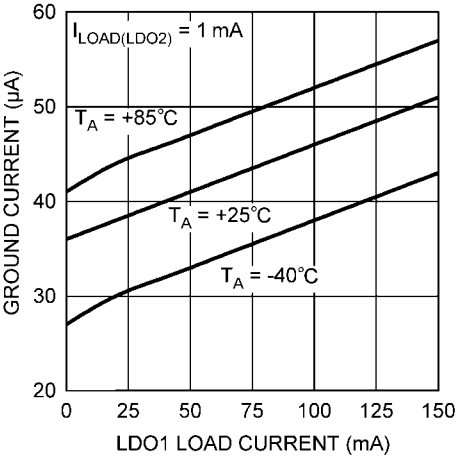
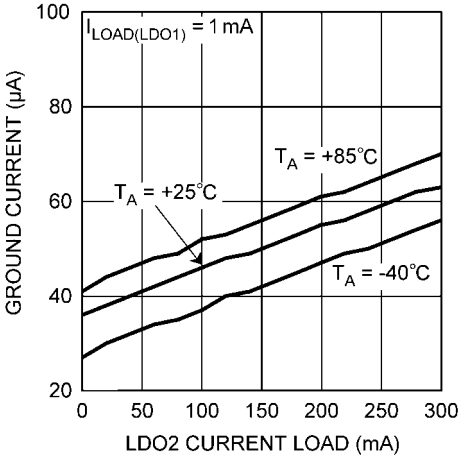
Ground Current vs Load Current, LDO1



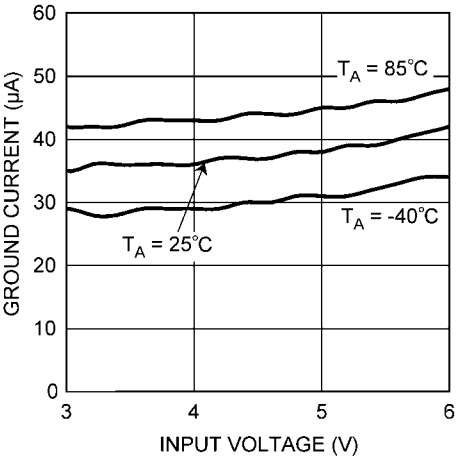
20145813

Ground Current vs Load Current, LDO2



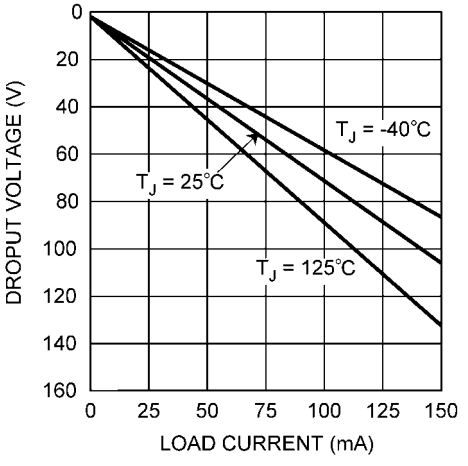
20145814

Ground Current vs V_{IN}. I_{LOAD} = 1mA



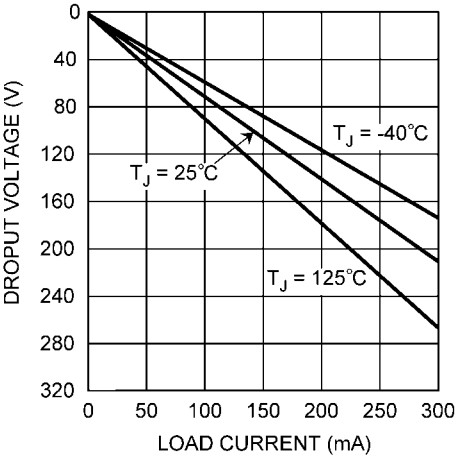
20145815

Dropout Voltage vs I_{LOAD}, LDO1



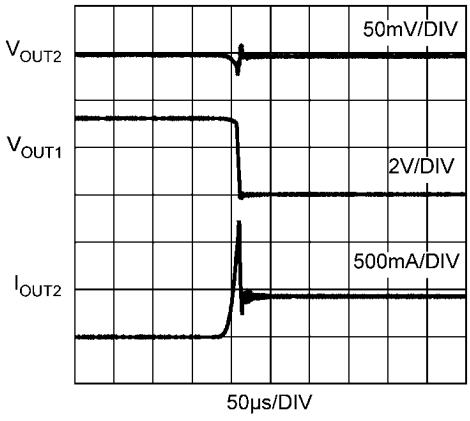
20145811

Dropout Voltage vs I_{LOAD}, LDO2



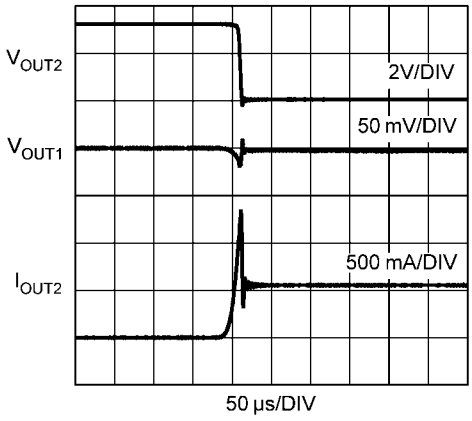
20145812

Short Circuit Current, LDO1



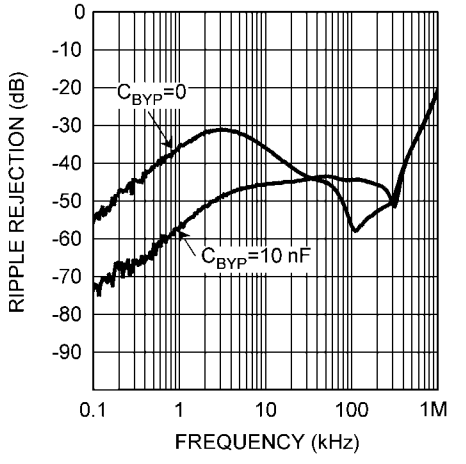
20145852

Short Circuit Current, LDO2



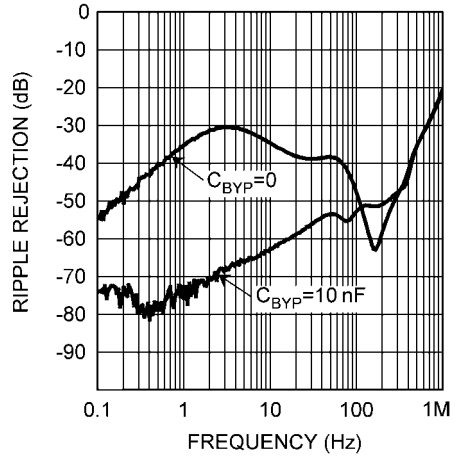
20145853

Power Supply Rejection Ratio, LDO1



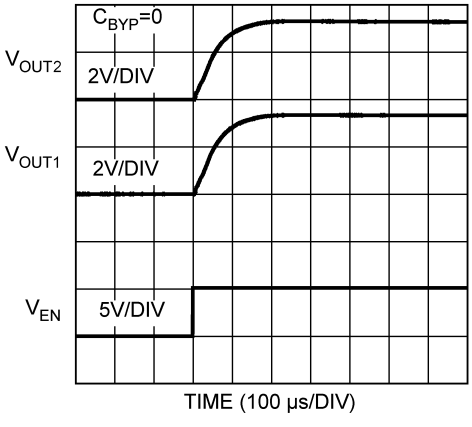
20145855

Power Supply Rejection Ratio, LDO2



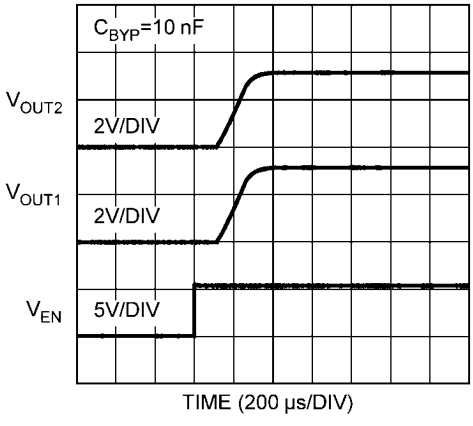
20145854

Enable Start-up Time, C_{BYP}=0



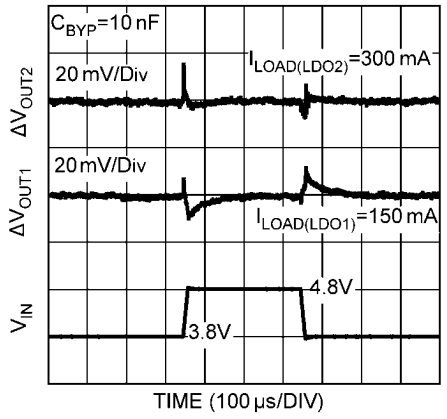
20145860

Enable Start-up Time, C_{BYP}=10nF



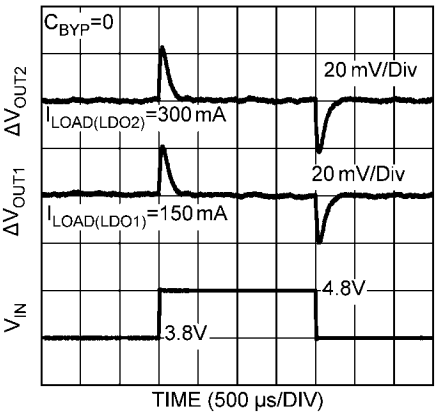
20145861

Line Transient, C_{BYP}=10nF



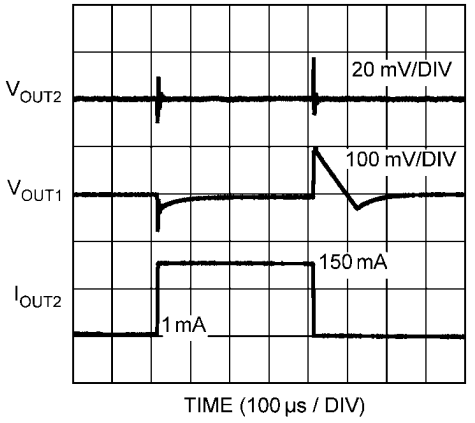
20145819

Line Transient, C_{BYP}=0



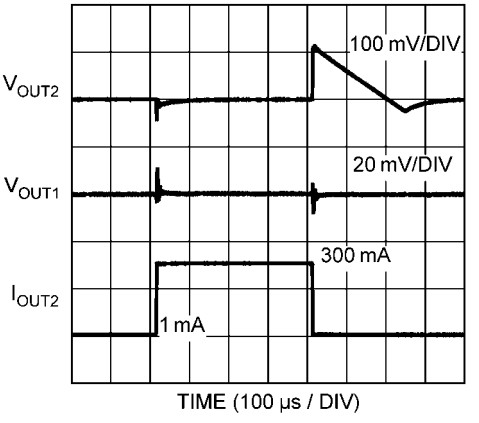
20145820

Load Transient, LDO1



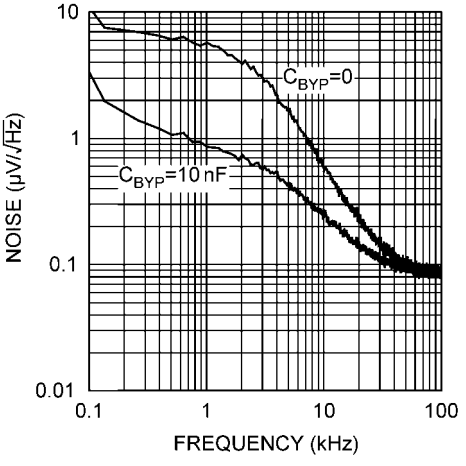
20145850

Load Transient, LDO2



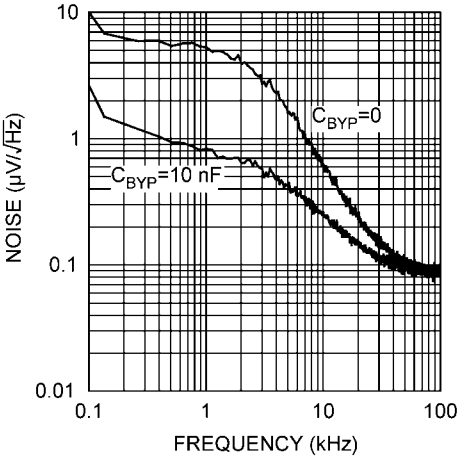
20145851

Noise Density LDO1



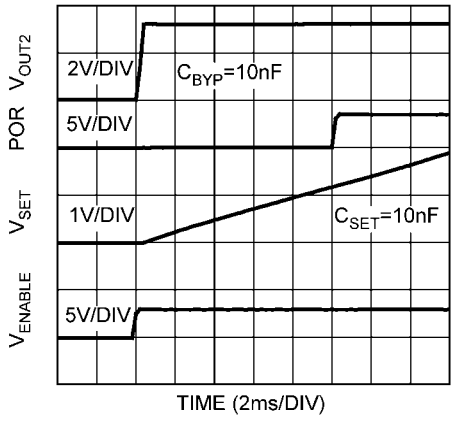
20145856

Noise Density, LDO2



20145857

Power-on-Reset Start-up Operation



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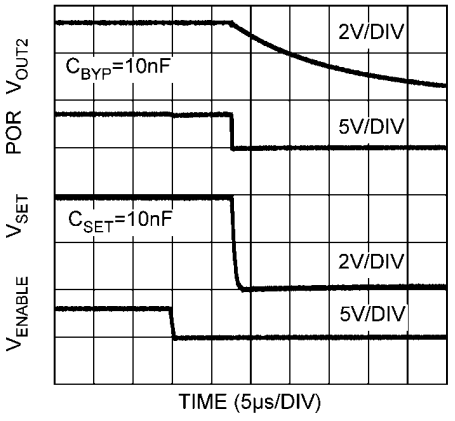
Power-on-Reset Shutdown Operation



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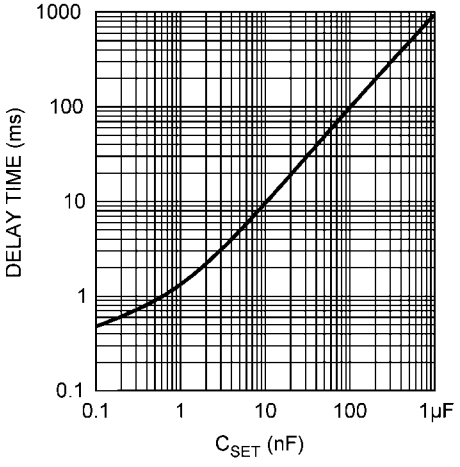
POR Delay Time



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Application Hints

OPERATION DESCRIPTION

The LP3996 is a low quiescent current, power management IC, designed specifically for portable applications requiring minimum board space and smallest components. The LP3996 contains two independently selectable LDOs. The first is capable of sourcing 150mA at outputs between 0.8V and 3.3V. The second can source 300mA at an output voltage of 0.8V to 3.3V. In addition, LDO2 contains power good flag circuit, which monitors the output voltage and indicates when it is within 8% of its nominal value. The flag will also act as a power-on-reset signal and, by adding an external capacitor; a delay may be programmed for the POR output.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP3996 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3996 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5mΩ to 500mΩ, is suitable in the LP3996 application circuit.

For this device the output capacitor should be connected between the V_{OUT} pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5mΩ to 500mΩ for stability.

NO-LOAD STABILITY

The LP3996 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3996 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP3996.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, *Figure 4* shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

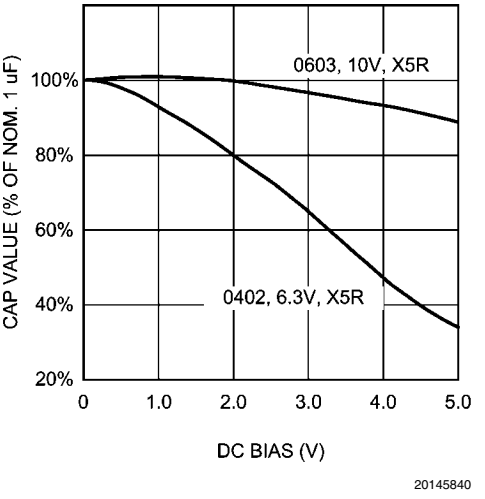

FIGURE 4. Graph Showing a Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more

costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP3996 features active high enable pins for each regulator, EN1 and EN2, which turns the corresponding LDO off when pulled low. The device outputs are enabled when the enable lines are set to high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, one or both enable pins should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on / off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

POWER-ON-RESET

The POR pin is an open-drain output which will be set to Low whenever the output of LDO2 falls out of regulation to approximately 90% of its nominal value. An external pull-up resistor, connected to V_{OUT} or V_{IN}, is required on this pin. During start-up, or whenever a fault condition is removed, the POR flag will return to the High state after the output reaches approximately 96% of its nominal value. By connecting a capacitor from the SET pin to GND, a delay to the rising condition of the POR flag may be introduced. The delayed signal may then be used as a Power-on -Reset for a microprocessor within the user's application.

The duration of the delay is determined by the time to charge the delay capacitor to a threshold voltage of 1.25V at 1.2µA from the SET pin as in the formula below.

$$t_{DELAY} = \frac{V_{TH(SET)} \times C_{SET}}{I_{SET}}$$

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A 0.1µF capacitor will introduce a delay of approximately 100ms.

BYPASS CAPACITOR

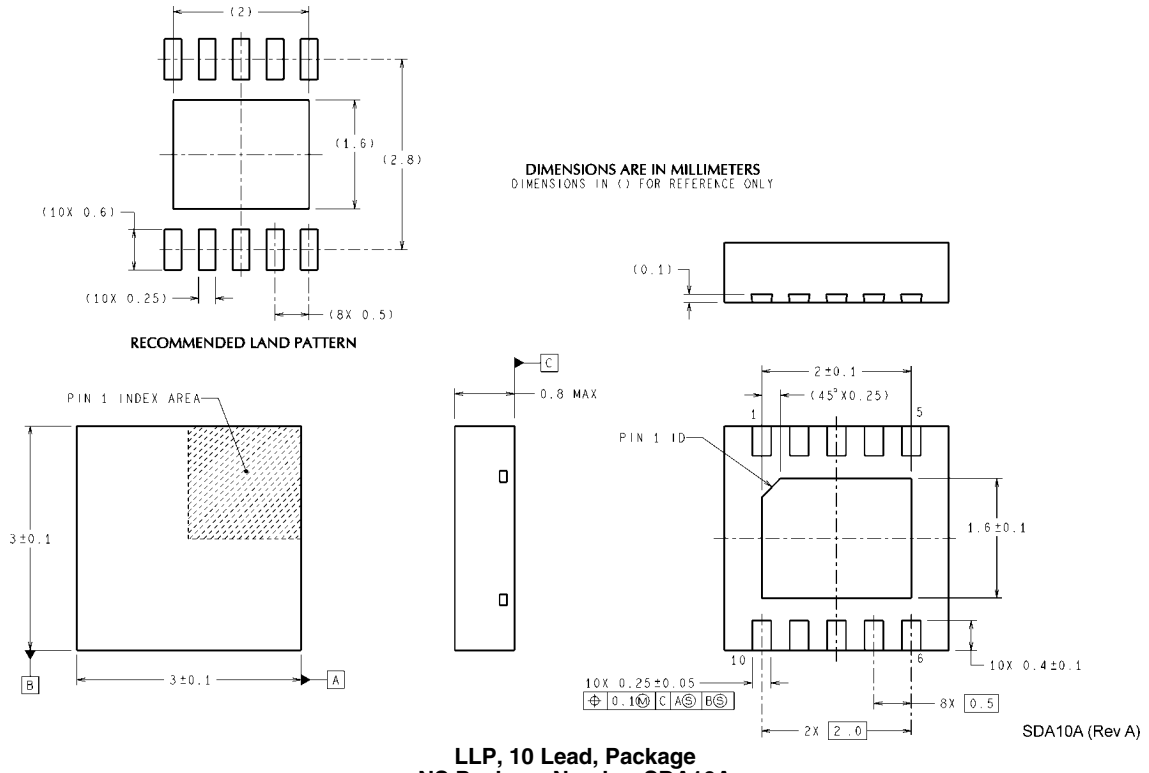
The internal voltage reference circuit of the LP3996 is connected to the C_{BYP} pin via a high value internal resistor. An external capacitor, connected to this pin, forms a low-pass filter which reduces the noise level on both outputs of the device. There is also some improvement in PSSR and line transient performance. Internal circuitry ensures rapid charging of the C_{BYP} capacitor during start-up. A 10nF, high quality ceramic capacitor with either NPO or COG dielectric is recommended due to their low leakage characteristics and low noise performance.

SAFE AREA OF OPERATION

Due consideration should be given to operating conditions to avoid excessive thermal dissipation of the LP3996 or triggering its thermal shutdown circuit. When both outputs are enabled, the total power dissipation will be $P_{D(LDO1)} + P_{D(LDO2)}$ Where $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$ for each LDO.

In general, device options which have a large difference in output voltage will dissipate more power when both outputs are enabled, due to the input voltage required for the higher output voltage LDO. In such cases, especially at elevated ambient temperature, it may not be possible to operate both outputs at maximum current at the same time.

Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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