010108

Am9321

Dual Demultiplexer/One-of-Four Decoder

Distinctive Characteristics

- Dual 1-of-4 Decoder
- Active LOW enable for each decoder
- Can be used as dual four channel Demultiplexer
- 100% reliability assurance testing in compliance with MIL-STD-883

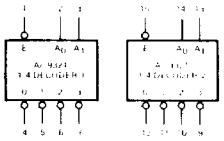
FUNCTIONAL DESCRIPTION

The Am9321 dual demultiplexer/one-of-four decoder consists of two identical independent decoders. Each decoder accepts two address inputs which select one-of-four mutually exclusive outputs. An active LOW enable is also provided on each decoder for expansion and demultiplexing applications. When this enable is at a HIGH logic level all the decoder outputs are forced HIGH.

In the demultiplexing mode data is presented at the enable input and appears noninverted at the selected output.

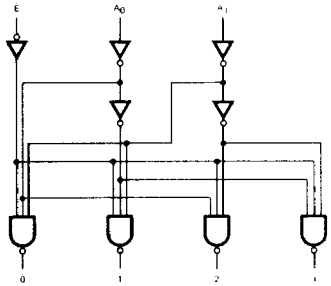
The Am9321 is an ideal MSI element for use in decoding in high-speed memory systems.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

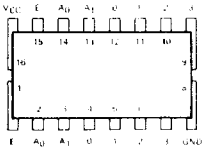


Note: Only one decoder shown.

Am9321 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	9321PC
Hermetic DIP	0°C to +75°C	9321DC
Dice	0°C to +75°C	9321XC
Hermetic DIP	−55°C to +125°C	9321DM
Hermetic Flat Pak	−55°C to +125°C	9321FM
Dice	−55°C to +125°C	9321XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C
Temperature (Ambient) Under Bias	−55°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.
DC Voltage Applied to Outputs for High Output State	−0.5 V to
DC Input Voltage	−0.5
Output Current, Into Outputs	
DC Input Current	−30 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

9321XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
9321XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6	
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4
V_{IH}	Input HIGH Level	Guaranteed input logic HIGH voltage for all inputs	2.0		
V_{IL}	Input LOW Level	Guaranteed input logic LOW voltage for all inputs			0.8
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V		−1.0	−1.6
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		6.0	40
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−20	−40	−70
I_{CC}	Power Supply Current	V_{CC} = MAX.		30	50

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C)

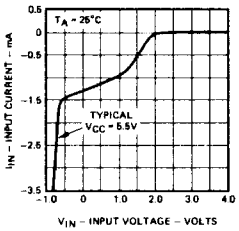
Parameters	Description	Test Conditions	Min.	Typ.	Max.
t_{PLH}	Turn Off Delay A Input to Output	V_{CC} = 5.0V C_L = 15pF		13	20
t_{PHL}	Turn On Delay A Input to Output			10	21
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output			9	14
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output			10	18

Notes: 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.

PERFORMANCE CURVES

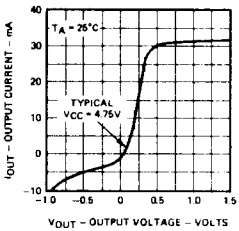
Input/Output Characteristics

Input

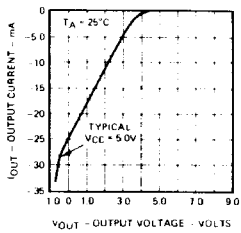


Output

Low State



High State



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Decoder/Demultiplexer On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Unit load One T²L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to −1.6mA at 0.4V.

OPERATIONAL TERMS:

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into output in V_{OL} test.

I_{CC} The current drawn by the device under a +5.0V power supply, bias input terminals grounded and output terminals open.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5V logic level).

t_{PLH} The propagation delay measured from the input transition to a corresponding output signal LOW-HIGH transition.

t_{PHL} The propagation delay measured from the input transition to a corresponding output signal HIGH-LOW transition.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400 Series	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TRUTH TABLE

For Each Decoder

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

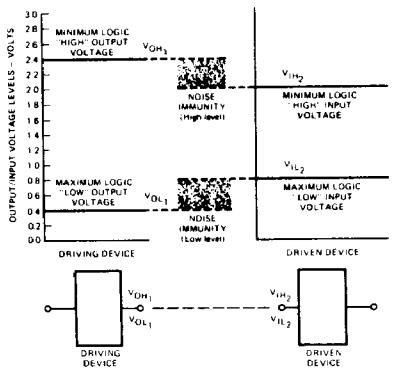
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOADING RULES

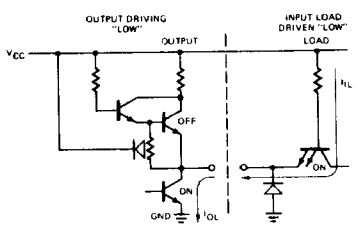
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ Decoder 1	1	1	–	–
A_0	2	1	–	–
A_1	3	1	–	–
$\overline{0}$	4	–	20	10
$\overline{1}$	5	–	20	10
$\overline{2}$	6	–	20	10
$\overline{3}$	7	–	20	10
GND	8	–	–	–
$\overline{3}_{out}$ Decoder 2	9	–	20	10
$\overline{2}$	10	–	20	10
$\overline{1}$	11	–	20	10
$\overline{0}$	12	–	20	10
A_1	13	1	–	–
A_0	14	1	–	–
$\overline{E}$	15	1	–	–
V_{CC}	16	–	–	–

INPUT/OUTPUT INTERFACE CONDITIONS

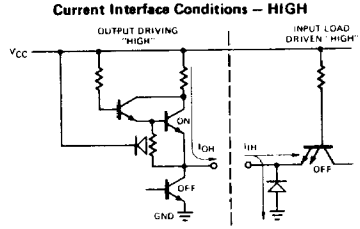
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW

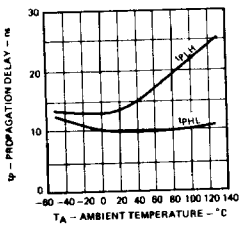


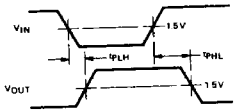
Current Interface Conditions – HIGH



SWITCHING CHARACTERISTICS
(Typical)

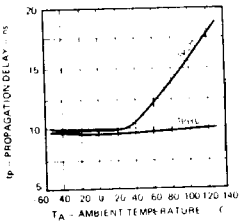
Address Input to Output



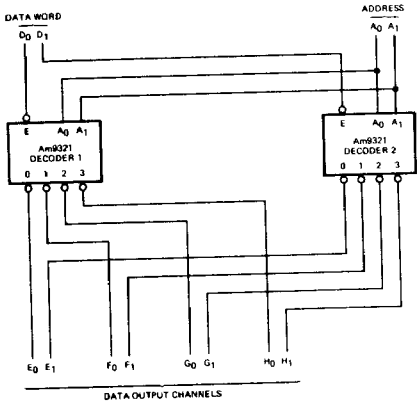


Other Conditions: $\overline{E}$ = LOW

Enable Input to Output



BASIC DEMULTIPLEXER/DECODER APPLICATIONS



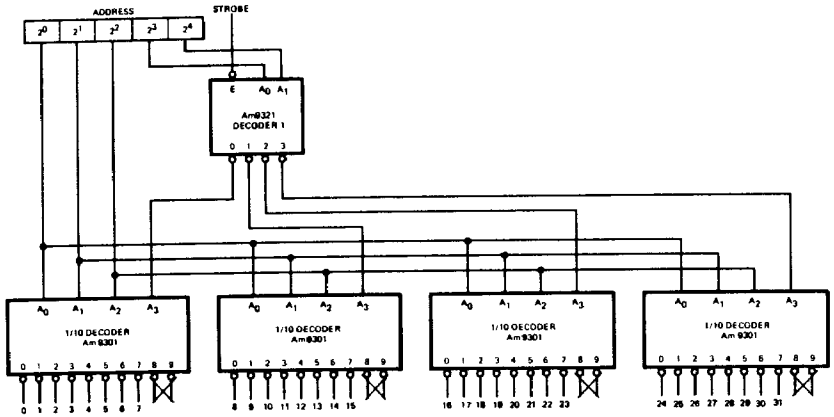
Address		Output Channel
A_0	A_1	
0	0	E
1	0	F
0	1	G
1	1	H

Dual 4 Output Demultiplexer

A 2-Bit Data Field D_0, D_1 is routed to one of four channels E, F, G, H under control of the address Field A.

ADDITIONAL APPLICATIONS

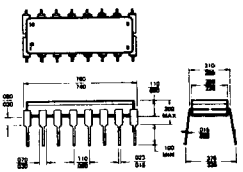
ONE-OUT-OF-THIRTY-TWO DECODER



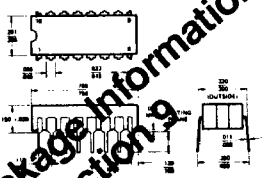
Am9321 Dual 1-of-4 Decoder can be used with other decoders such as the Am9301 1-of-10 Decoder or Am9311 1-of-16 Decoder to build large decoding trees or to form multi channel Demultiplexers.

PHYSICAL DIMENSIONS
Dual-In-Line

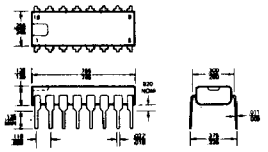
Hermetic



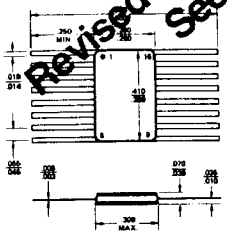
Ceramic



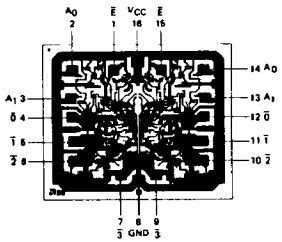
Molded



Flat Package



Metallization and Pad Layout



ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

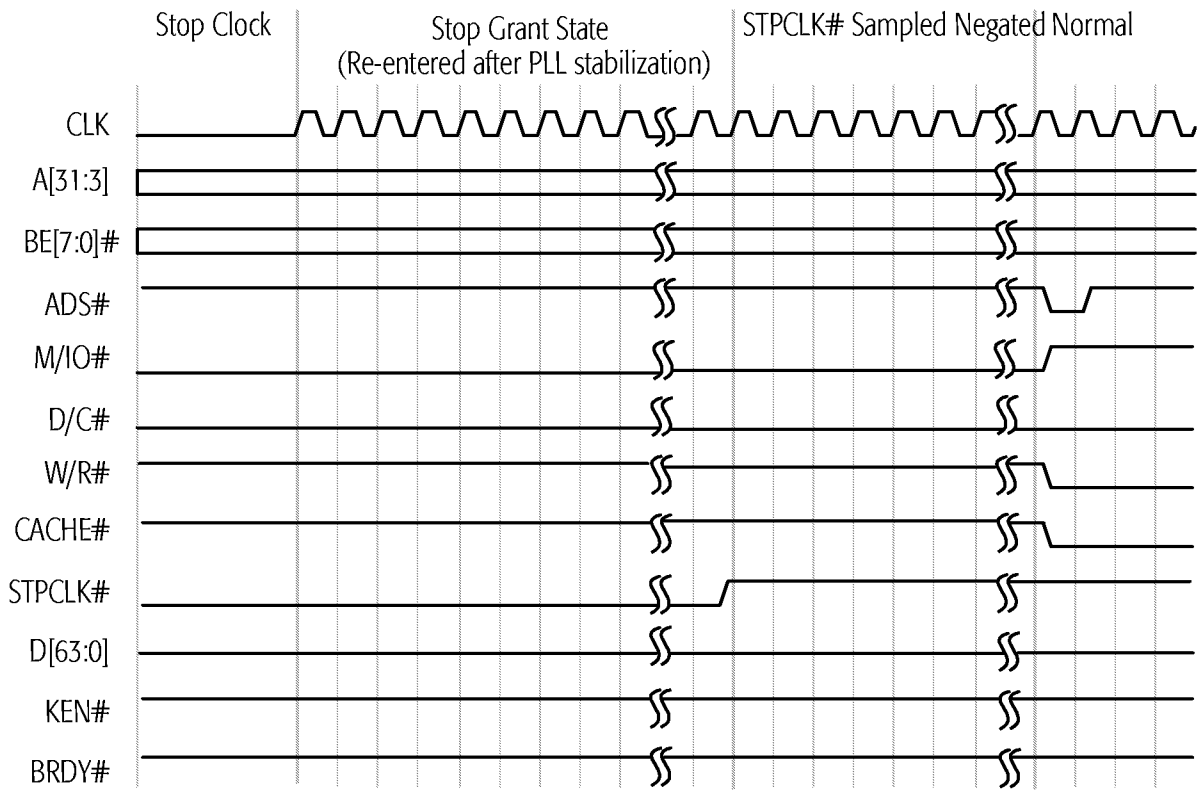


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

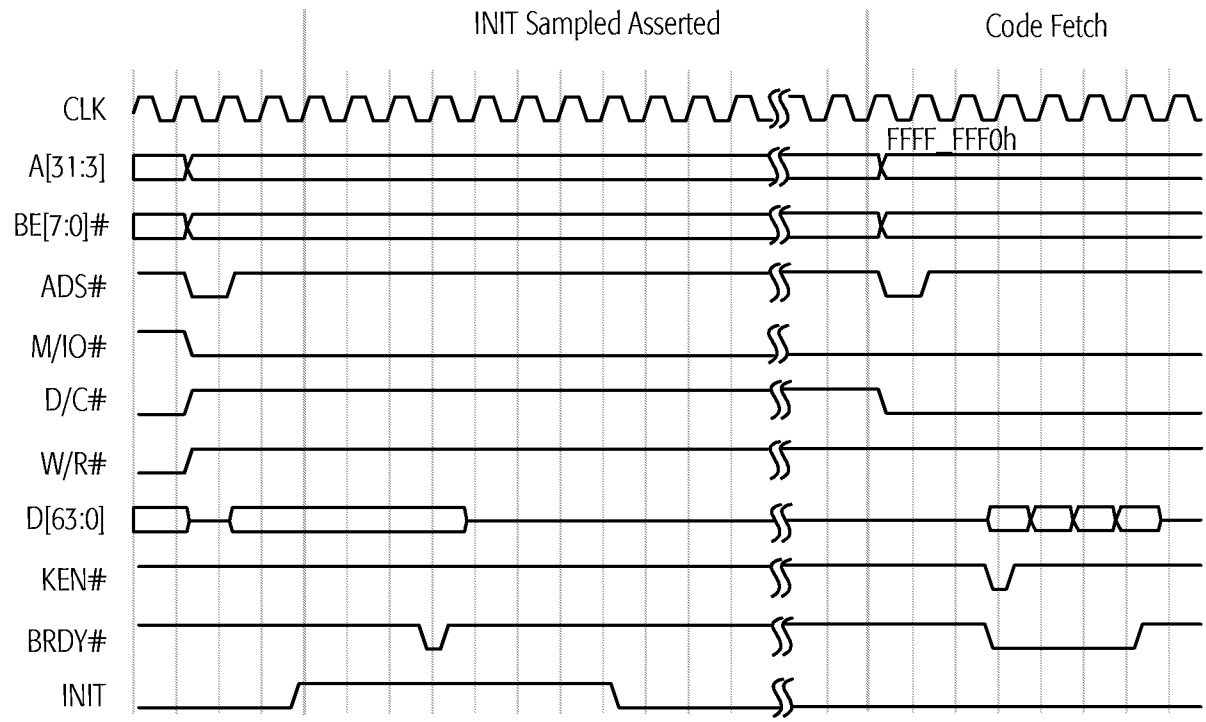


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.