

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# RJK2017DPE

Silicon N Channel MOS FET  
High Speed Power Switching

REJ03G1589-0400

Rev.4.00

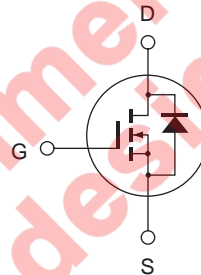
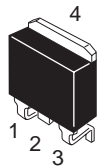
Dec 02, 2009

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.036 \Omega$  typ. (at  $I_D = 22.5 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ )
- Low leakage current
- High speed switching

## Outline

RENESAS Package code: PRSS0004AE-B  
(Package name: LDKPAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	200	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$	45	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	135	A
Body-drain diode reverse drain current	$I_{DR}$	45	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ <sup>Note1</sup>	135	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	12	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	9.6	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	100	W
Channel to case thermal impedance	$\theta_{ch-c}$	1.25	$^\circ\text{C/W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2. Value at  $T_c = 25^\circ\text{C}$

3.  $ST_{ch} = 25^\circ\text{C}$ ,  $T_{ch} \leq 150^\circ\text{C}$

## Electrical Characteristics

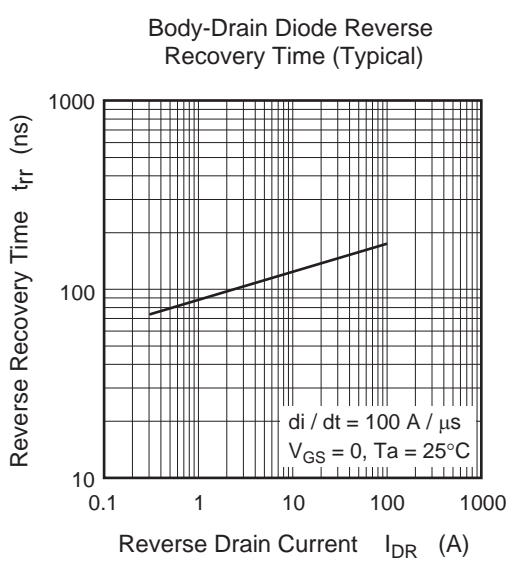
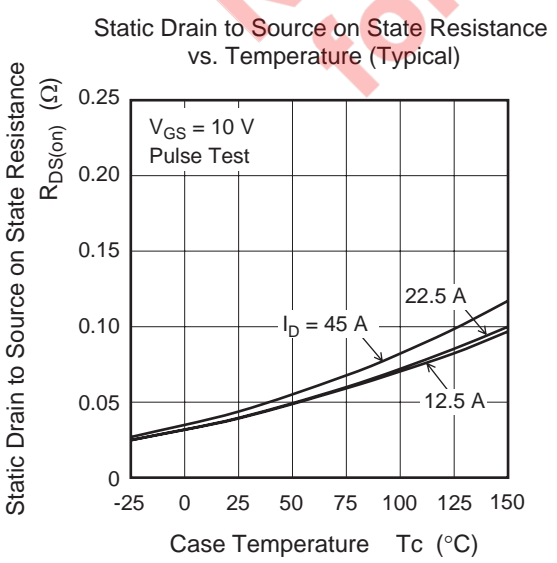
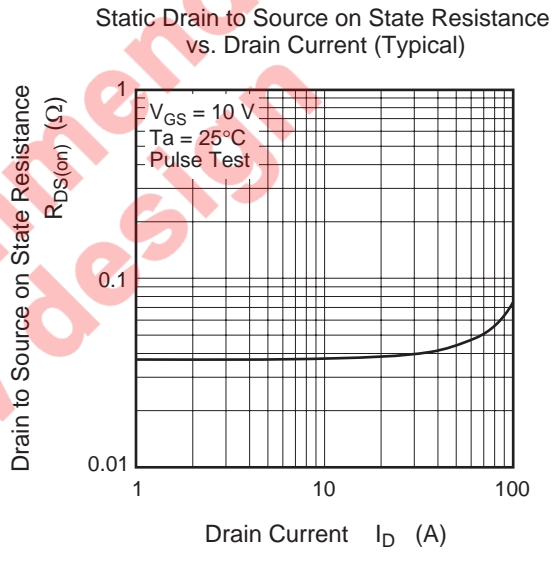
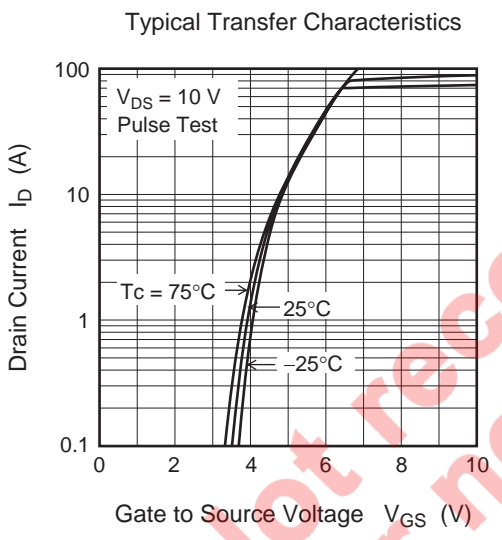
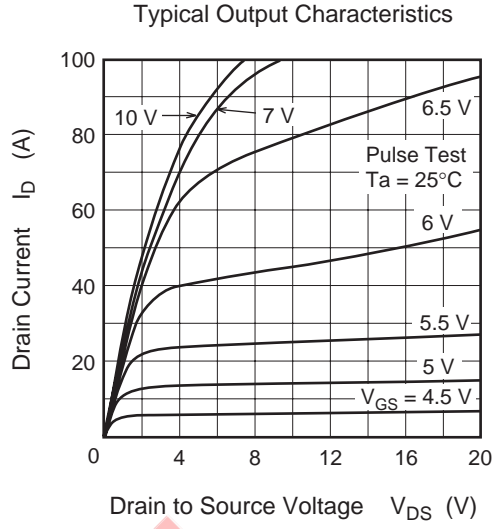
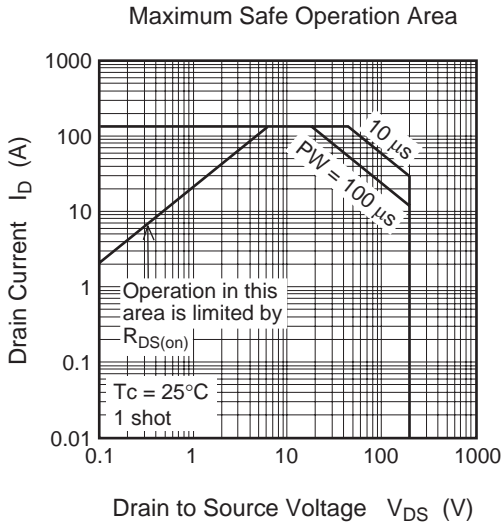
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 200 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2	—	4	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.036	0.047	$\Omega$	$I_D = 22.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	4800	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	290	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	90	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	$I_D = 22.5 \text{ A}$
Rise time	$t_r$	—	40	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	95	—	ns	$R_L = 4.5 \Omega$
Fall time	$t_f$	—	40	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	66	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	$Q_{gs}$	—	26	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	16	—	nC	$I_D = 45 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.88	1.35	V	$I_F = 45 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	150	—	ns	$I_F = 45 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

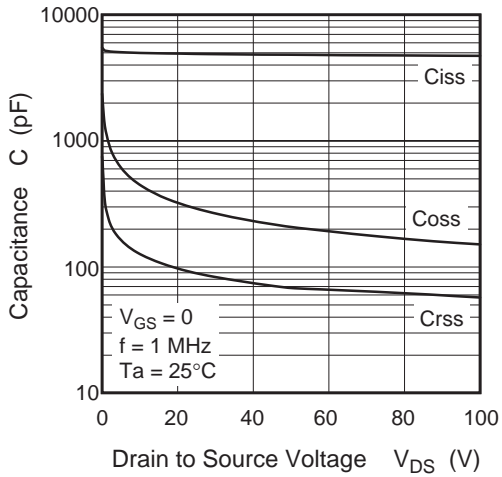
Notes: 4. Pulse test

Not recommended  
for new designs

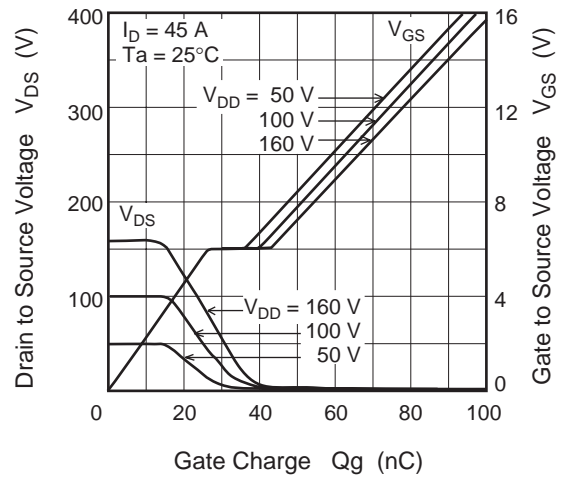
Main Characteristics



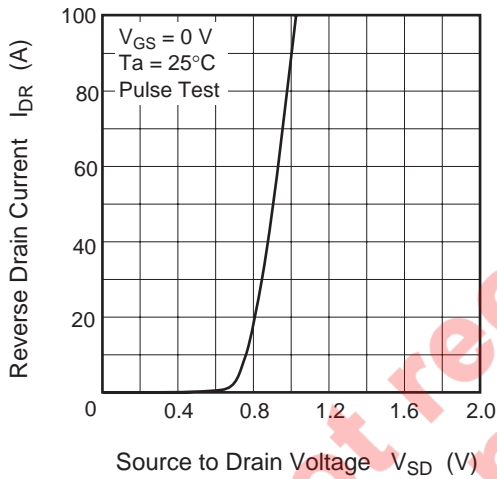
Typical Capacitance vs. Drain to Source Voltage



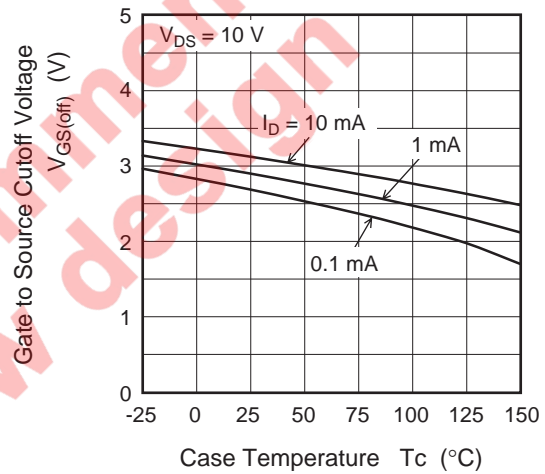
Dynamic Input Characteristics (Typical)

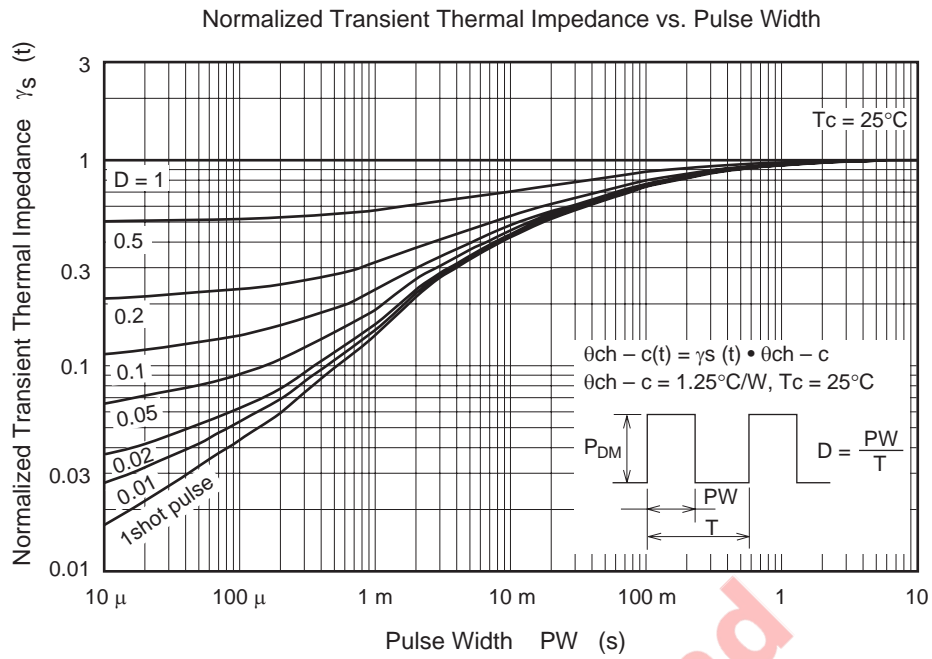


Reverse Drain Current vs. Source to Drain Voltage (Typical)

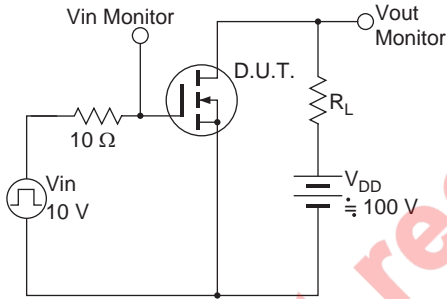


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

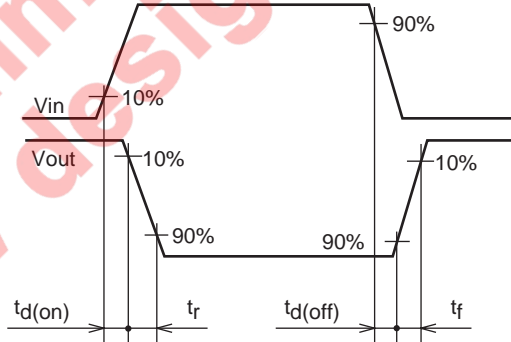




Switching Time Test Circuit

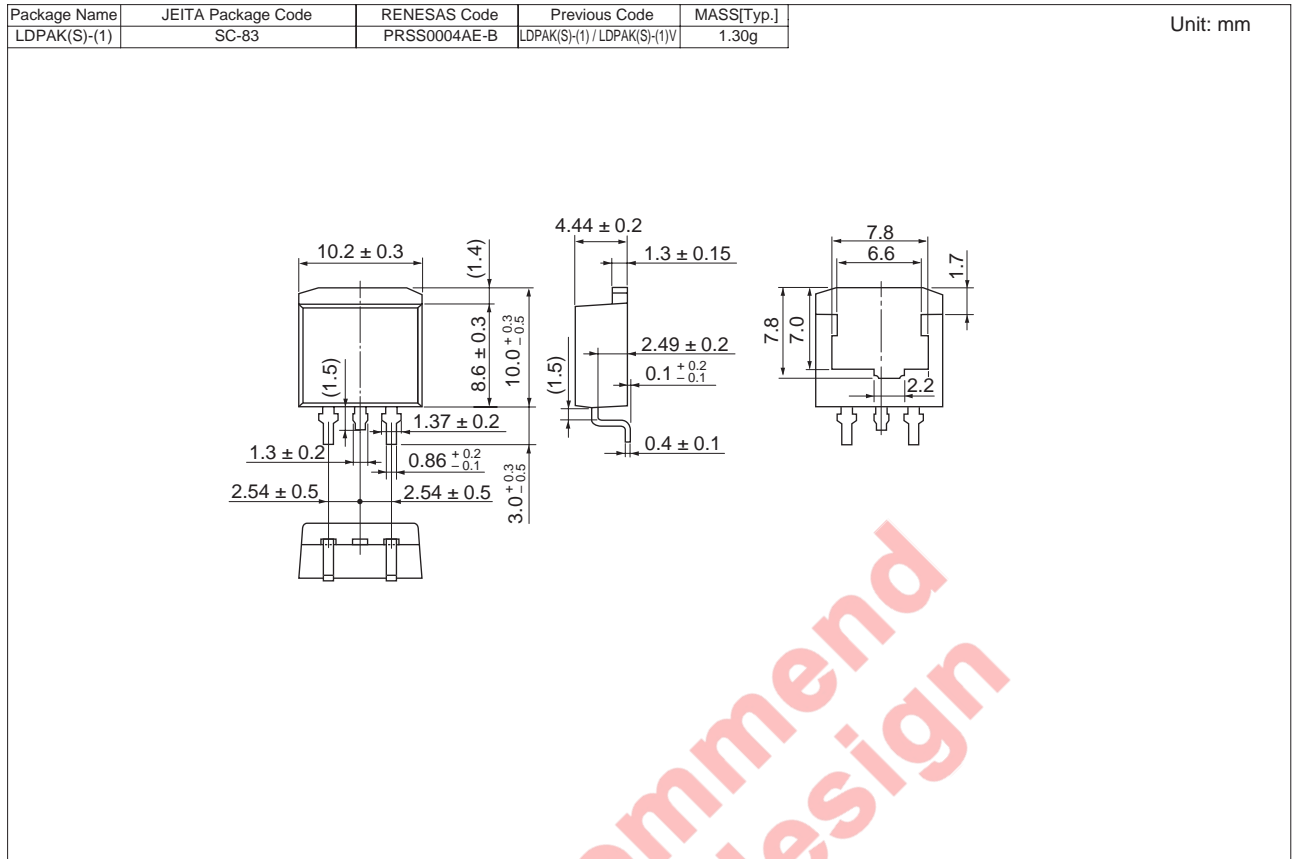


Waveform



Not recommended for new design

### Package Dimensions



### Ordering Information

Part No.	Quantity	Shipping Container
RJK2017DPE-00-J3	1000 pcs	Taping

Not recommend  
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