APPENDIX A
ELECTRICAL CHARACTERISTICS

Table A–1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to + 7.0	V
Input Voltage	V_{in}	–0.3 to + 7.0	V
Operating Temperature Range MC68HC(7)11Ex MC68HC(7)11ExC MC68HC(7)11ExV MC68HC(7)11ExM MC68HC811E2 MC68HC811E2C MC68HC811E2V MC68HC811E2M MC68L11Ex	T_A	T_L to T_H 0 to + 70 –40 to + 85 –40 to + 105 –40 to + 125 0 to + 70 –40 to + 85 –40 to + 105 –40 to + 125 –20 to + 70	°C
Storage Temperature Range	T_{stg}	–55 to + 150	°C
Current Drain per Pin[1] Excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA

NOTES:
1. One pin at a time, observing maximum power dissipation limits

Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table A–2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average Junction Temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient Temperature	T_A	User-determined	°C
Package Thermal Resistance (Junction-to-Ambient) 48-Pin Plastic DIP (MC68HC811E2 only) 56-Pin Plastic SDIP 52-Pin Plastic Leaded Chip Carrier 52-Pin Plastic Thin Quad Flat Pack (TQFP) 64-Pin Quad Flat Pack	Θ_{JA}	 50 50 50 85 85	°C/W
Total Power Dissipation (Note 1)	P_D	$P_{INT} + P_{I/O}$ $K / (T_J + 273°C)$ (Note 1)	W
Device Internal Power Dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O Pin Power Dissipation (Note 2)	$P_{I/O}$	User-determined	W
A Constant (Note 3)	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W·°C

NOTES:
1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

Table A–3 DC Electrical Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristics	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = ±10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	0.1 —	V
Output High Voltage (Note 1) All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = –0.8 mA, V_{DD} = 4.5 V	V_{OH}	V_{DD} –0.8	—	V
Output Low Voltage All Outputs Except XTAL I_{Load} = 1.6 mA	V_{OL}	—	0.4	V
Input High Voltage All Inputs Except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	0.7 × V_{DD} 0.8 × VDD	V_{DD} + 0.3 V_{DD} + 0.3	V
Input Low Voltage All Inputs	V_{IL}	V_{SS} –0.3	0.2 × V_{DD}	V
I/O Ports, Three-State Leakage PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$ V_{in} = V_{IH} or V_{IL}	I_{OZ}	—	±10	µA
Input Leakage Current (Note 2) V_{in} = V_{DD} or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ V_{in} = V_{DD} or V_{SS} MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)	I_{in}	— —	±1 ±10	µA µA
RAM Standby Voltagee Power down	V_{SB}	4.0	V_{DD}	V
RAM Standby Current Power down	I_{SB}	—	10	µA
Input Capacitance PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{in}	— —	8 12	pF pF
Output Load Capacitance All Outputs Except PD[4:1] PD[4:1]	C_L	— —	90 100	pF pF
Maximum Total Supply Current (Note 3)				
RUN:	I_{DD}			
Single-Chip Mode 2 MHz		—	15	mA
3 MHz		—	27	mA
Expanded Multiplexed Mode 2 MHz		—	27	mA
3 MHz		—	35	mA
WAIT: (All Peripheral Functions Shut Down)	W_{IDD}			
Single-Chip Mode 2 MHz		—	6	mA
3 MHz		—	15	mA
Expanded Multiplexed Mode 2 MHz		—	10	mA
3 MHz		—	20	mA
STOP:	S_{IDD}			
Single-Chip Mode, No Clocks –40 to + 85		—	25	µA
> + 85 to + 105		—	50	
> +105 to + 125		—	100	
Maximum Power Dissipation	P_D			
Single-Chip Mode 2 MHz		—	85	mW
3 MHz		—	150	mW
Expanded Multiplexed Mode 2 MHz		—	150	mW
3 MHz		—	195	mW

NOTES:
1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. Refer to A/D specification for leakage current for port E.
3. EXTAL is driven with a square wave, and
   t_{cyc} = 500 ns for 2 MHz rating;
   t_{cyc} = 333 ns for 3 MHz rating; $V_{IL} \leq 0.2$ V;
   $V_{IH} \geq V_{DD} - 0.2$ V; No dc loads

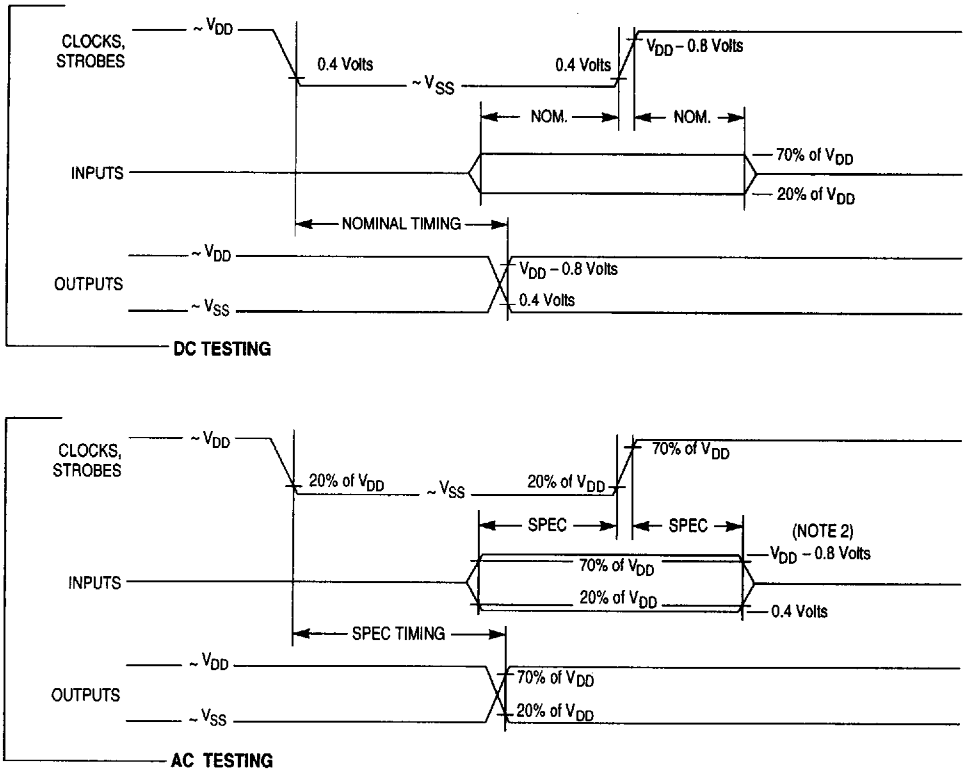
Table A–3a DC Electrical Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = ±10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	0.1 —	V V
Output High Voltage (Note 1) All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = –0.5 mA, V_{DD} = 3.0 V I_{Load} = –0.8 mA, V_{DD} = 4.5 V	V_{OH}	V_{DD} –0.8	—	V
Output Low Voltage All Outputs Except XTAL I_{Load} = 1.6 mA, V_{DD} = 5.0 V I_{Load} = 1.0 mA, V_{DD} = 3.0 V	V_{OL}	—	0.4	V
Input High Voltage All Inputs Except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	0.7 × V_{DD} 0.8 × VDD	V_{DD} + 0.3 V_{DD} + 0.3	V V
Input Low Voltage All Inputs	V_{IL}	V_{SS} –0.3	0.2 × V_{DD}	V
I/O Ports, Three-State Leakage PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$ $V_{in} = V_{IH}$ or V_{IL}	I_{OZ}	—	±10	µA
Input Leakage Current (Note 2) $V_{in} = V_{DD}$ or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ $V_{in} = V_{DD}$ or V_{SS} MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)	I_{in}	 — —	 ±1 ±10	 µA µA
RAM Standby Voltage Power down	V_{SB}	2.0	V_{DD}	V
RAM Standby Current Power down	I_{SB}	—	10	µA
Input Capacitance PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{in}	— —	8 12	pF pF
Output Load Capacitance All Outputs Except PD[4:1] PD[4:1]	C_L	— —	90 100	pF pF

Characteristic		Symbol	1 MHz	2 MHz	Unit
Maximum Total Supply Current (Note 3)					
RUN:		I_{DD}			
Single-Chip Mode	V_{DD} = 5.5 V		8	15	mA
	V_{DD} = 3.0 V		4	8	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		14	27	mA
	V_{DD} = 3.0 V		7	14	mA
WAIT:(All Peripheral Functions Shut Down)		W_{IDD}			
Single-Chip Mode	V_{DD} = 5.5 V		3	6	mA
	V_{DD} = 3.0 V		1.5	3	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		5	10	mA
	V_{DD} = 3.0 V		2.5	5	mA
STOP:		S_{IDD}			
Single-Chip Mode, No Clocks	V_{DD} = 5.5 V		50	50	µA
	V_{DD} = 3.0 V		25	25	µA
Maximum Power Dissipation		P_D			
Single-Chip Mode	V_{DD} = 5.5 V		44	85	mW
	V_{DD} = 3.0 V		12	24	mW
Expanded Multiplexed Mode	V_{DD} = 5.5 V		77	150	mW
	V_{DD} = 3.0 V		21	42	mW

NOTES:
1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. Refer to A/D specification for leakage current for port E.
3. EXTAL is driven with a square wave, and
   t_{cyc} = 1000 ns for 1 MHz rating;
   t_{cyc} = 500 ns for 2 MHz rating; $V_{IL} \leq 0.2$ V;
   $V_{IH} \geq V_{DD}$ - 0.2 V; No dc loads.



NOTES:

1. Full test loads are applied during all DC electrical tests and AC timing measurements.
2. During AC timing measurements, inputs are driven to 0.4 volts and VDD – 0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

TEST METHODS

Figure A–1 Test Methods

Table A–4 Control Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	333	—	ns
Crystal Frequency	f_{XTAL}	—	4.0	—	8.0	—	12.0	MHz
External Oscillator Frequency	4 f_o	dc	4.0	dc	8.0	dc	12.0	MHz
Processor Control Setup Time t_{PCSU} = 1/4 t_{cyc} + 50 ns	t_{PCSU}	300	—	175	—	133	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	PW_{RSTL}	 8 1	 — —	 8 1	 — —	 8 1	 — —	t_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	2	—	2	—	t_{cyc}
Mode Programming Hold Time	t_{MPH}	10	—	10	—	10	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge-Sensitive Mode PW_{IRQ} = t_{cyc} + 20 ns	PW_{IRQ}	1020	—	520	—	353	—	ns
Wait Recovery Start-up Time	t_{WRS}	—	4	—	4	—	4	t_{cyc}
Timer Pulse Width Input Capture Pulse Accumulator Input PW_{TIM} = t_{cyc} + 20 ns	PW_{TIM}	1020	—	520	—	353	—	ns

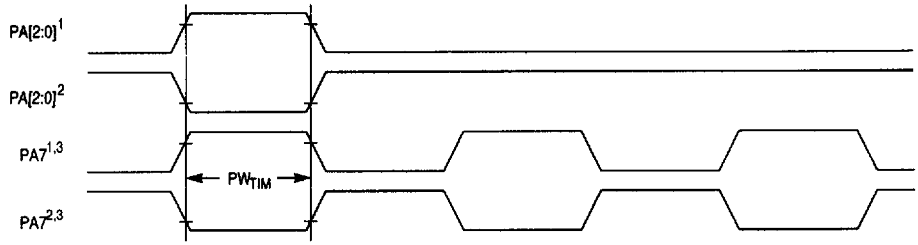
NOTES:
1. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

Table A–4a Control Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Crystal Frequency	f_{XTAL}	—	4.0	—	8.0	MHz
External Oscillator Frequency	4 f_o	dc	4.0	dc	8.0	MHz
Processor Control Setup Time t_{PCSU} = 1/4 t_{cyc} + 75 ns	t_{PCSU}	325	—	200	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	PW_{RSTL}	 8 1	 — —	 8 1	 — —	 t_{cyc} t_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	2	—	t_{cyc}
Mode Programming Hold Time	t_{MPH}	10	—	10	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge-Sensitive Mode PW_{IRQ} = t_{cyc} + 20 ns	PW_{IRQ}	1020	—	520	—	ns
Wait Recovery Start-up Time	t_{WRS}	—	4	—	4	t_{cyc}
Timer Pulse Width, Input Capture Pulse Accumulator Input PW_{TIM} = t_{cyc} + 20 ns	PW_{TIM}	1020	—	520	—	ns

NOTES:
1. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



NOTES:
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

TIMER INPUTS TIM

Figure A–2 Timer Inputs

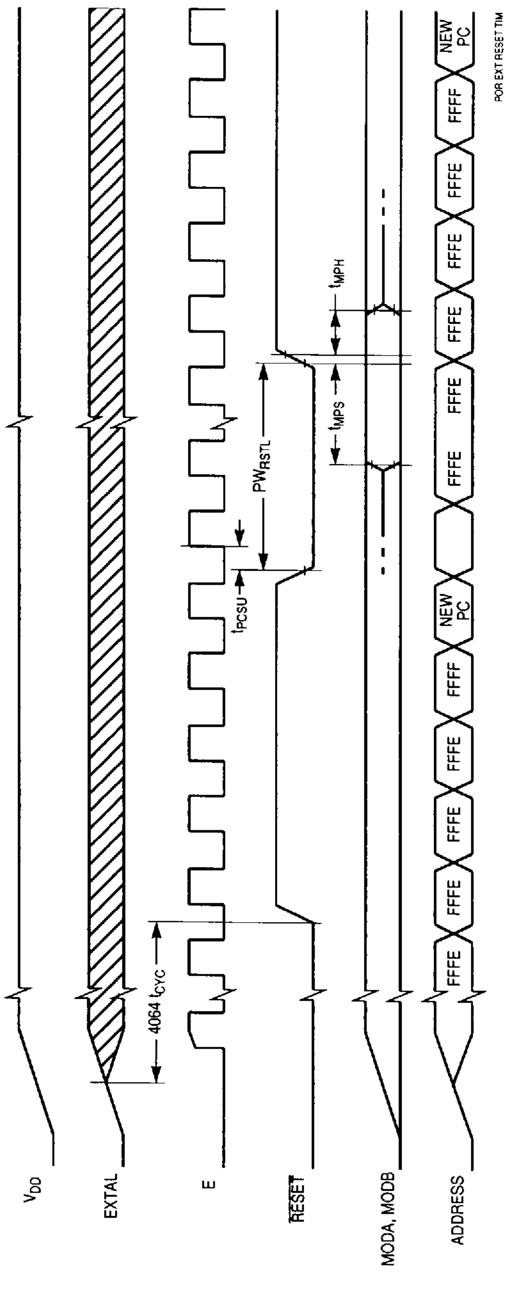


Figure A–3 POR External Reset Timing Diagram

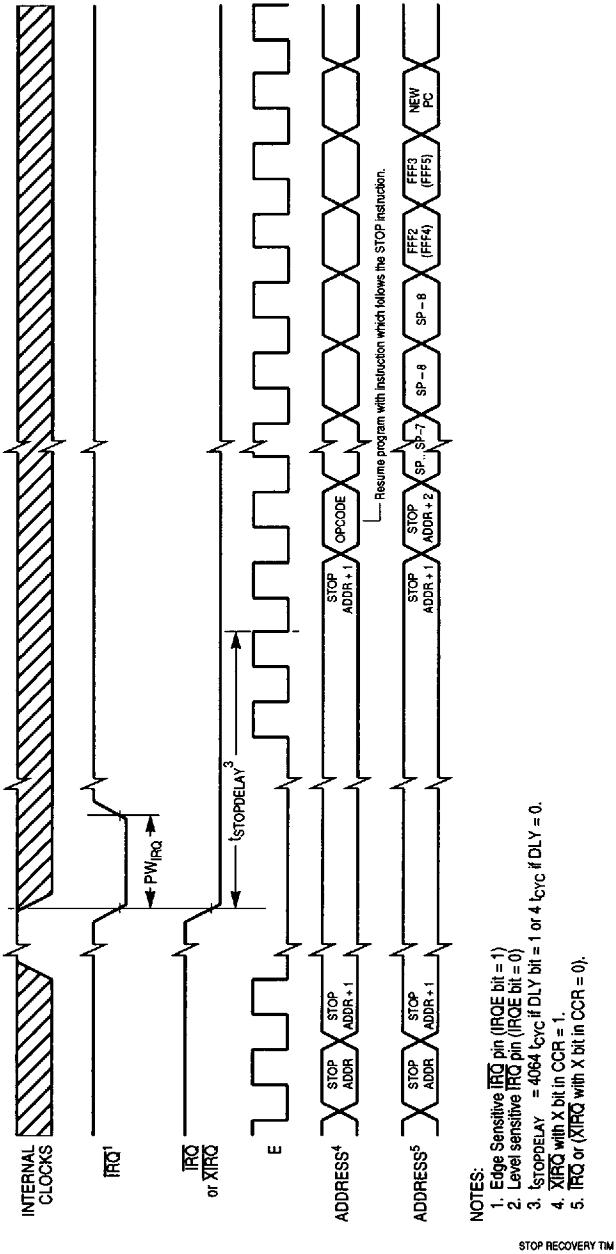


Figure A–4 STOP Recovery Timing Diagram

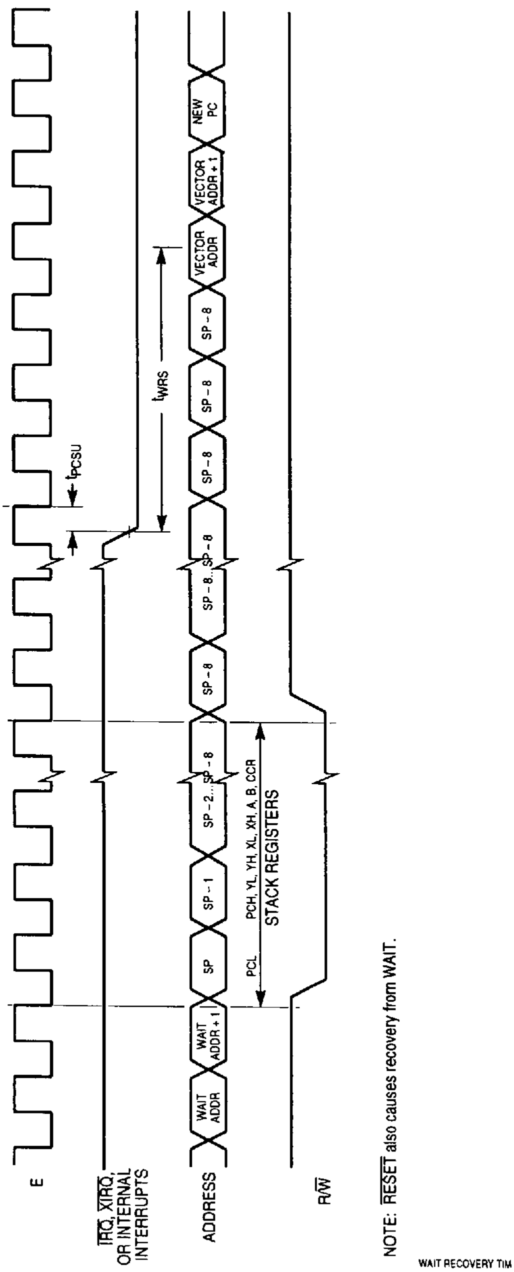


Figure A–5 WAIT Recovery from Interrupt Timing Diagram

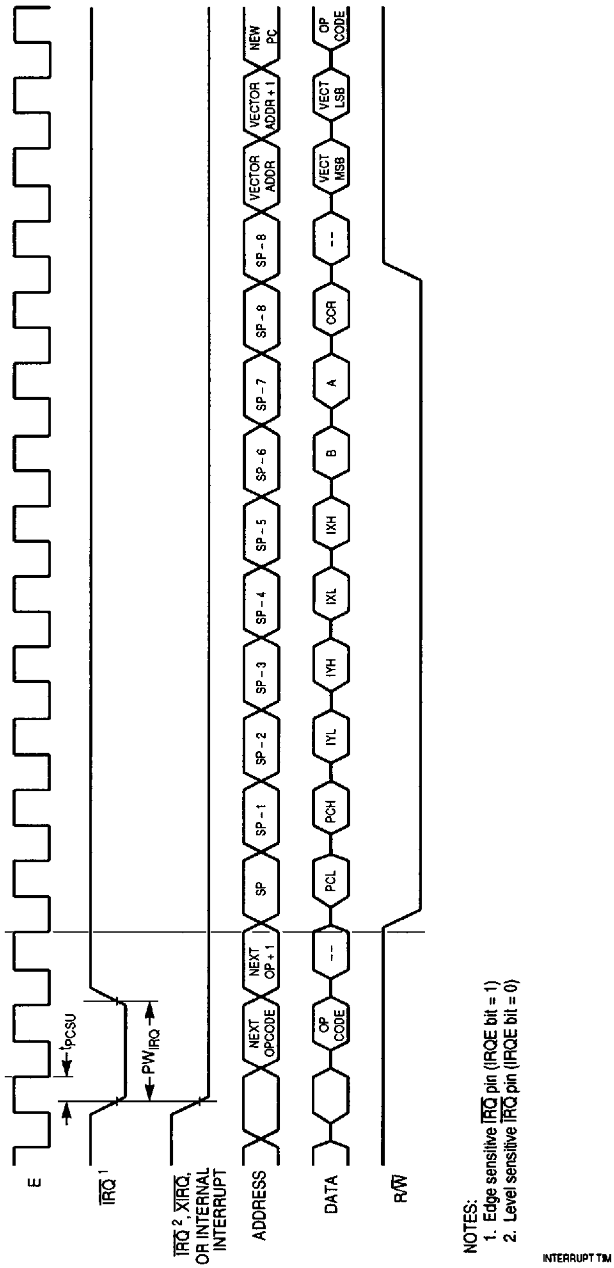


Figure A–6 Interrupt Timing Diagram

Table A–5 Peripheral Port Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	333	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	t_{PDSU}	100	—	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	t_{PDH}	50	—	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 100 ns	t_{PWD}	— —	200 350	— —	200 225	— —	200 183	ns ns
Input Data Setup Time (Port C)	t_{IS}	60	—	60	—	60	—	ns
Input Data Hold Time (Port C)	t_{IH}	100	—	100	—	100	—	ns
Delay Time, E Fall to STRB t_{DEB} = 1/4 t_{cyc} + 100 ns	t_{DEB}	—	350	—	225	—	183	ns
Setup Time, STRA Asserted to E Fall (Note 1)	t_{AES}	0	—	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	t_{PCD}	—	100	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	—	10	—	10	—	ns
Three-State Hold Time	t_{PCZ}	—	150	—	150	—	150	ns

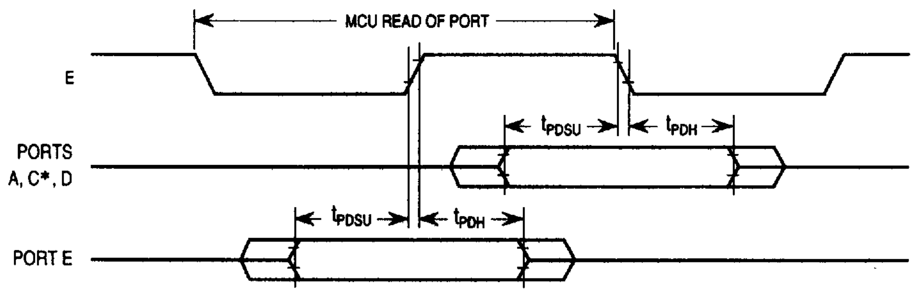
NOTES:
1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

Table A–5a Peripheral Port Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	t_{PDSU}	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	t_{PDH}	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D $t_{PWD} = 1/4\ t_{cyc} + 150$ ns	t_{PWD}	 — —	 250 400	 — —	 250 275	 ns ns
Input Data Setup Time (Port C)	t_{IS}	60	—	60	—	ns
Input Data Hold Time (Port C)	t_{IH}	100	—	100	—	ns
Delay Time, E Fall to STRB $t_{DEB} = 1/4\ t_{cyc} + 150$ ns	t_{DEB}	—	400	—	275	ns
Setup Time, STRA Asserted to E Fall (Note 1)	t_{AES}	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	t_{PCD}	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	—	10	—	ns
Three-State Hold Time	t_{PCZ}	—	150	—	150	ns

NOTES:
1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



* FOR NON-LATCHED OPERATION OF PORT C

EI PORT RD TIM

Figure A–7 Port Read Timing Diagram

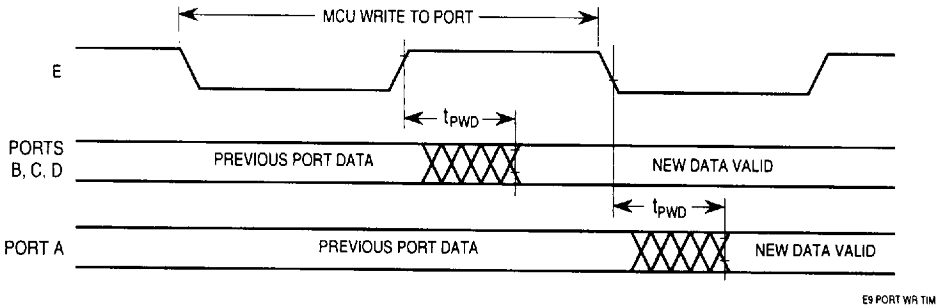


Figure A–8 Port Write Timing Diagram

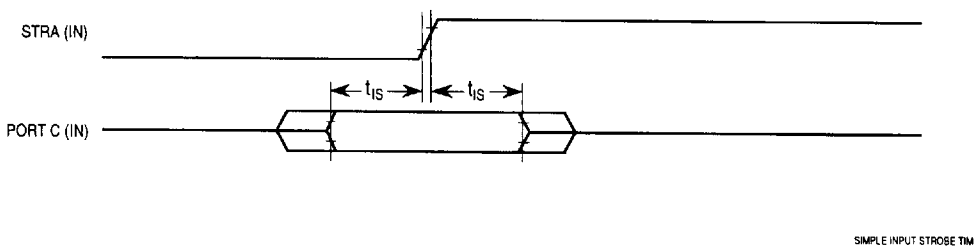


Figure A–9 Simple Input Strobe Timing Diagram

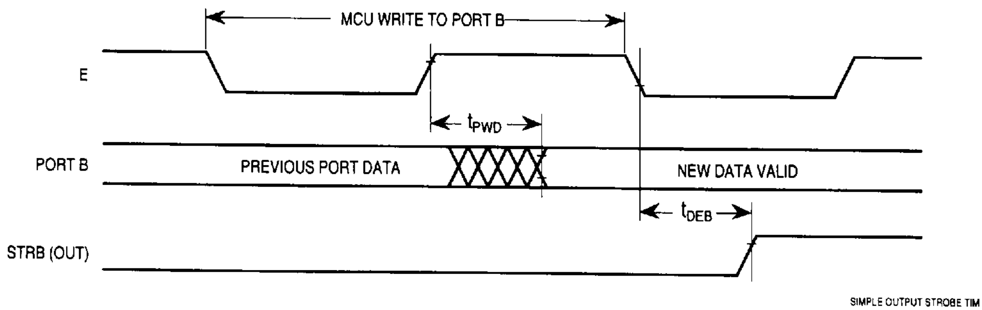
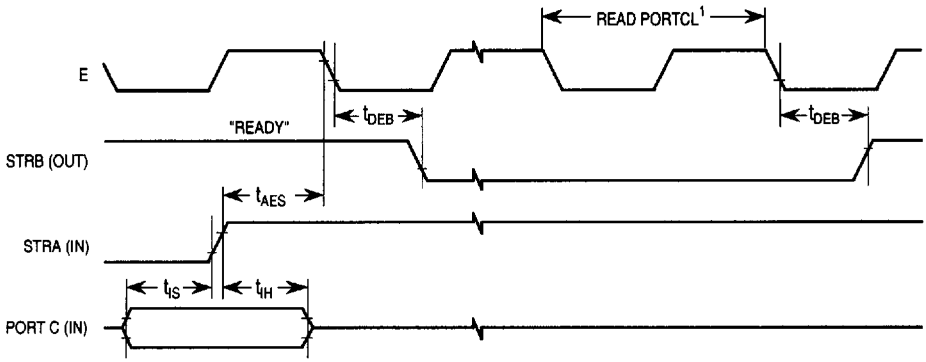


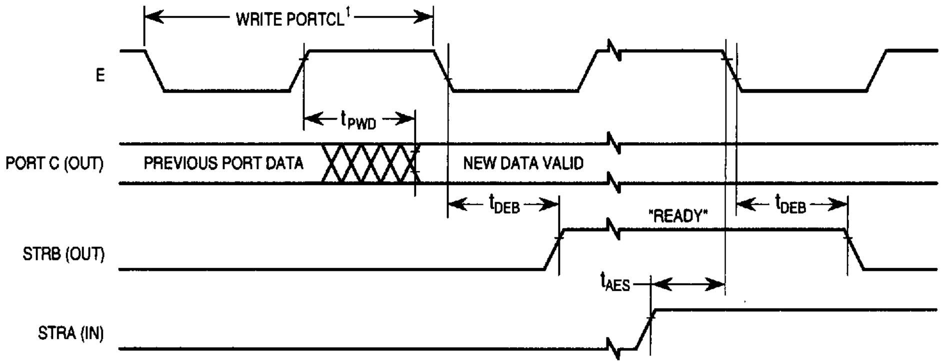
Figure A–10 Simple Output Strobe Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C INPUT HNDSHK TIM

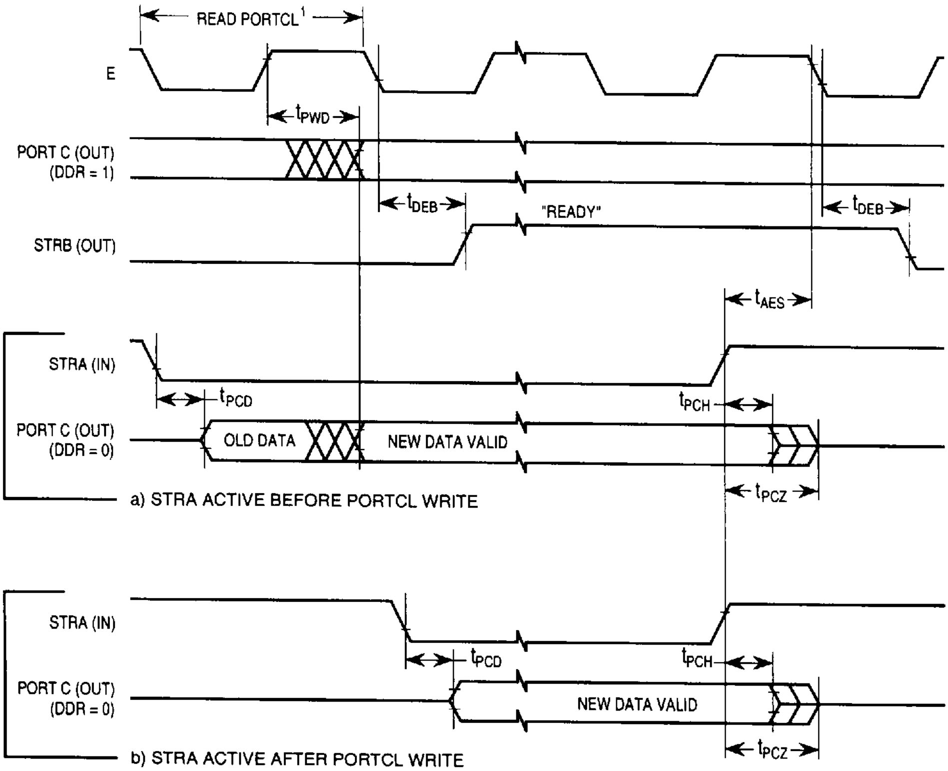
Figure A–11 Port C Input Handshake Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C OUTPUT HNDSHK TIM

Figure A–12 Port C Output Handshake Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

3-STATE VAR OUTPUT HNDSHK TIM

Figure A–13 Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)

Table A–6 Analog-To-Digital Converter Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, 750 kHz ≤E ≤3.0 MHz, unless otherwise noted

Characteristic	Parameter	Min	Absolute	2.0 MHz Max	3.0 MHz Max	Unit
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	±1/2	±1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	±1/2	±1	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	±1/2	±1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	±1/2	±1 1/2	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	±1/2	±1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	±1	±2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	—	V_{RH}	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (Note 2)	V_{RL}	—	V_{DD} + 0.1	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage (Note 2)	V_{SS} -0.1	—	V_{RH}	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL} (Note 2)	3	—	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:					
	E Clock	—	32	—	—	t_{cyc}
	Internal RC Oscillator	—	—	t_{cyc} + 32	t_{cyc} + 32	µs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—	—
Zero Input Reading	Conversion Result when V_{in} = V_{RL}	00	—	—	—	Hex
Full Scale Reading	Conversion Result when V_{in} = V_{RH}	—	—	FF	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:					
	E Clock	—	12	—	—	t_{cyc}
	Internal RC Oscillator	—	—	12	12	µs
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]	—	—	400	400	nA
	V_{RL}, V_{RH}	—	—	1.0	1.0	µA

NOTES:
1. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.
2. Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ±10%.

Table A–6a Analog-To-Digital Converter Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤E ≤2.0 MHz, unless otherwise noted

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	±1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	±1	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	±1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	±1 1/2	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	±1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	±2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	—	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage	V_{RL}	—	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage	V_{SS} –0.1	—	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL}	3.0	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:				
	E Clock	—	32	—	t_{cyc}
	Internal RC Oscillator	—	—	t_{cyc} + 32	μs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:				
	E Clock	—	12	—	t_{cyc}
	Internal RC Oscillator	—	—	12	μs
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]	—	—	400	nA
	V_{RL}, V_{RH}	—	—	1.0	μA

NOTES:
1. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.

Table A–7 Expansion Bus Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	333	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2\ t_{cyc} - 23$ ns (Note 1)	PW_{EL}	477	—	227	—	146	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2\ t_{cyc} - 28$ ns (Note 1)	PW_{EH}	472	—	222	—	141	—	ns
4a 4b	E and AS Rise Time E and AS Fall Time	t_r t_f	— —	20 20	— —	20 20	— —	20 15	ns
9	Address Hold Time $t_{AH} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2a)	t_{AH}	95.5	—	33	—	26	—	ns
12	Nonmultiplexed Address Valid Time to E Rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1, 2a)	t_{AV}	281.5	—	94	—	54	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	145.5	0	83	0	51	ns
19	Write Data Delay Time $t_{DDW} = 1/8\ t_{cyc} + 65.5$ ns (Note 1, 2a)	t_{DDW}	—	190.5	—	128		71	ns
21	Write Data Hold Time $t_{DHW} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2a)	t_{DHW}	95.5	—	33	—	26	—	ns
22	Multiplexed Address Valid Time to E Rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1, 2a)	t_{AVM}	271.5	—	84	—	54	—	ns
24	Multiplexed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} - 70$ ns (Note 1)	t_{ASL}	151	—	26	—	13	—	ns
25	Multiplexed Address Hold Time $t_{AHL} = 1/8\ t_{cyc} - 29.5$ ns (Note 1, 2b)	t_{AHL}	95.5	—	33	—	31	—	ns
26	Delay Time, E to AS Rise $t_{ASD} = 1/8\ t_{cyc} - 9.5$ ns (Note 1, 2a)	t_{ASD}	115.5	—	53	—	31	—	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4\ t_{cyc} - 29$ ns (Note 1)	PW_{ASH}	221	—	96	—	63	—	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8\ t_{cyc} - 9.5$ ns (Note 1, 2b)	t_{ASED}	115.5	—	53	—	31	—	ns
29	MPU Address Access Time (Note 2a) $t_{ACCA} = t_{cyc} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	t_{ACCA}	744.5	—	307	—	196	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} - t_{DSR}$	t_{ACCE}	—	442	—	192		111	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1, 2a)	t_{MAD}	145.5	—	83	—	51	—	ns

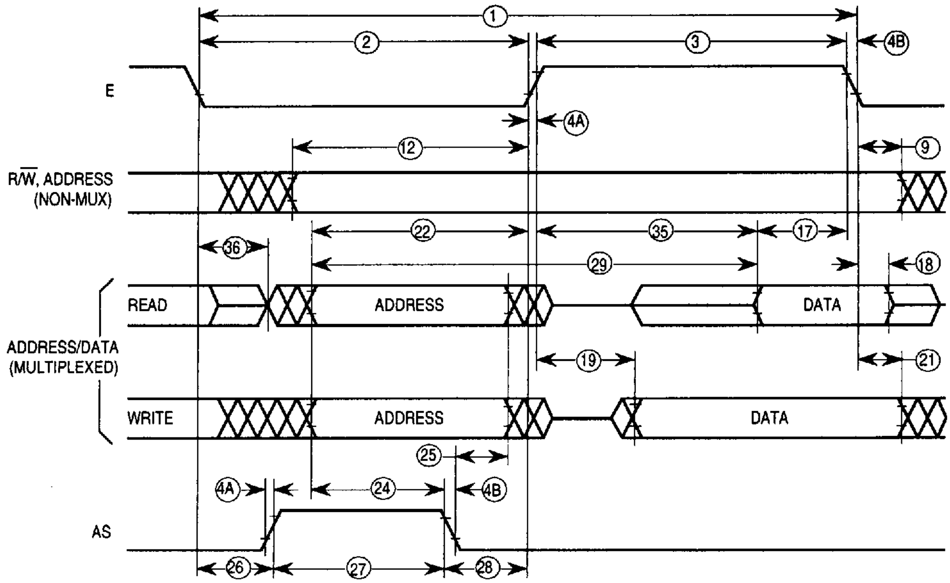
1. Formula only for dc to 2 MHz.
2. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas, where applicable:
   (a) (1–DC) × 1/4 t_{cyc}
   (b) DC × 1/4 t_{cyc}
   Where:
   DC is the decimal value of duty cycle percentage (high time).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

Table A–7a Expansion Bus Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	ns
2	Pulse Width, E Low PW_{EL} = 1/2 t_{cyc} –25 ns	PW_{EL}	475	—	225	—	ns
3	Pulse Width, E High PW_{EH} = 1/2 t_{cyc} –30 ns	PW_{EH}	470	—	220	—	ns
4A 4B	E and AS Rise Time E and AS Fall Time	t_r t_f	— —	25 25	— —	25 25	ns ns
9	Address Hold Time t_{AH} = 1/8 t_{cyc} –30 ns (Note 1a)	t_{AH}	95	—	33	—	ns
12	Nonmultiplexed Address Valid Time to E Rise t_{AV} = PW_{EL} –(t_{ASD} + 80 ns) (Note 1a)	t_{AV}	275	—	88	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	150	0	88	ns
19	Write Data Delay Time t_{DDW} = 1/8 t_{cyc} + 70 ns (Note 1a)	t_{DDW}	—	195	—	133	ns
21	Write Data Hold Time t_{DHW} = 1/8 t_{cyc} –30 ns (Note 1a)	t_{DHW}	95	—	33	—	ns
22	Multiplexed Address Valid Time to E Rise t_{AVM} = PW_{EL} –(t_{ASD} + 90 ns) (Note 1a)	t_{AVM}	265	—	78	—	ns
24	Multiplexed Address Valid Time to AS Fall t_{ASL} = PW_{ASH} –70 ns	t_{ASL}	150	—	25	—	ns
25	Multiplexed Address Hold Time t_{AHL} = 1/8 t_{cyc} –30 ns (Note 1b)	t_{AHL}	95	—	33	—	ns
26	Delay Time, E to AS Rise t_{ASD} = 1/8 t_{cyc} –5 ns (Note 1a)	t_{ASD}	120	—	58	—	ns
27	Pulse Width, AS High PW_{ASH} = 1/4 t_{cyc} –30 ns	PW_{ASH}	220	—	95	—	ns
28	Delay Time, AS to E Rise t_{ASED} = 1/8 t_{cyc} –5 ns (Note 1b)	t_{ASED}	120	—	58	—	ns
29	MPU Address Access Time (Note 1a) t_{ACCA} = t_{cyc} –(PW_{EL}–t_{AVM}) –t_{DSR}–t_f	t_{ACCA}	735	—	298	—	ns
35	MPU Access Time t_{ACCE} = PW_{EH} –t_{DSR}	t_{ACCE}	—	440	—	190	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) t_{MAD} = t_{ASD} + 30 ns (Note 1a)	t_{MAD}	150	—	88	—	ns

NOTES:
1. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas, where applicable:
   (a) (1–DC) × 1/4 t_{cyc}
   (b) DC × 1/4 t_{cyc}
   Where:
   DC is the decimal value of duty cycle percentage (high time).
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



NOTE: Measurement points shown are 20% and 70% of V_{DD}.

MUX BUS TIM

Figure A–14 Multiplexed Expansion Bus Timing Diagram

Table A–8 Serial Peripheral Interface Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

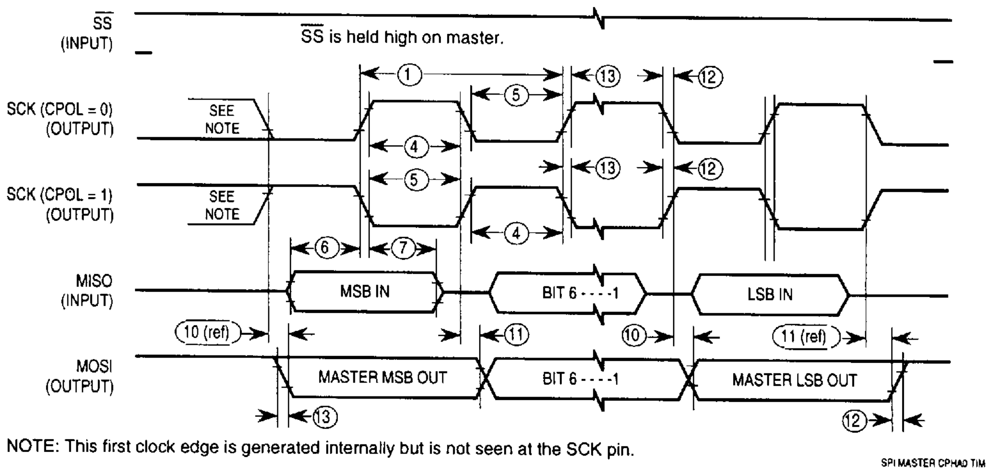
Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 2.0	dc dc	0.5 3.0	f_{op} MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 500	— —	2.0 333	— —	t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 250	— —	— 240	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 250	— —	— 240	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	340 190	— —	227 127	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	340 190	— —	227 127	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	t_a	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	t_{dis}	—	240	—	167	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{rm} t_{rs}	— —	100 2.0	— —	100 2.0	ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{fm} t_{fs}	— —	100 2.0	— —	100 2.0	ns µs

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on SCK, MOSI, and MISO pins.

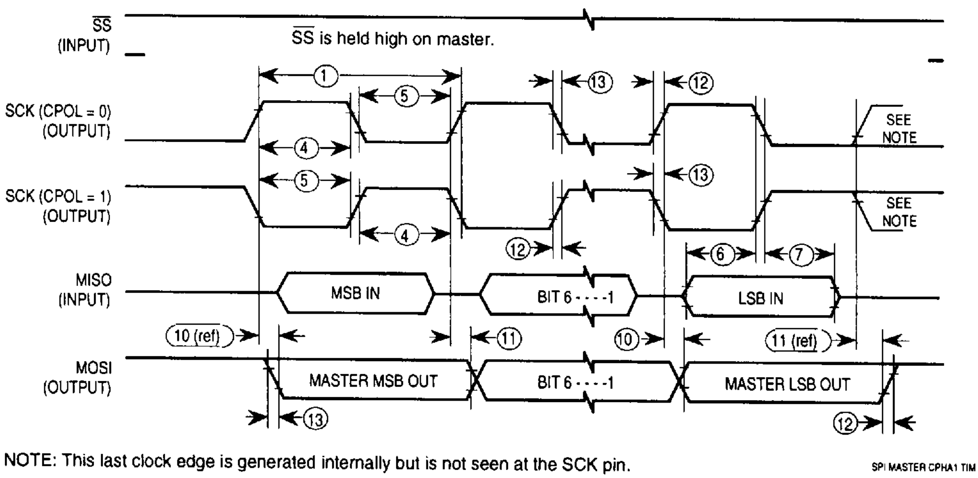
Table A–8a Serial Peripheral Interface Timing (MC68L11E9)

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 1.0	dc dc	0.5 2.0	f_{op} MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 1000	— —	2.0 500	— —	t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 500	— —	— 250	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 500	— —	— 250	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	680 380	— —	340 190	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	680 380	— —	340 190	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	t_a	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	t_{dis}	—	240	—	240	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{rm} t_{rs}	— —	100 2.0	— —	100 2.0	ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{fm} t_{fs}	— —	100 2.0	— —	100 2.0	ns µs

NOTES:
1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 100 pF load on all SPI pins.

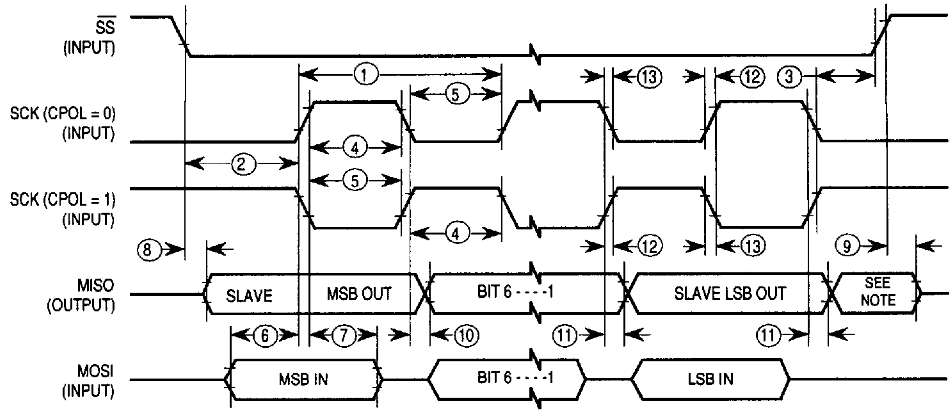


a) SPI Master Timing (CPHA = 0)



b) SPI Master Timing (CPHA = 1)

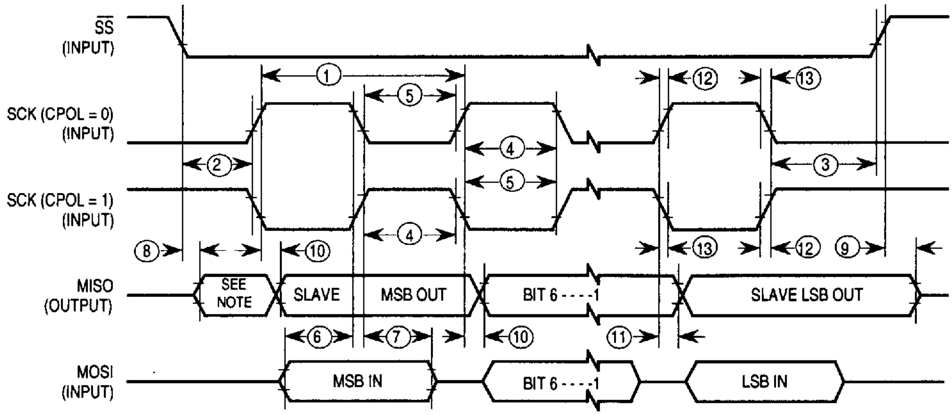
Figure A–15 SPI Timing Diagram (1 of 2)



NOTE: Not defined but normally MSB of character just received.

SPI SLAVE CPHA0 TIM

a) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character previously transmitted.

SPI SLAVE CPHA1 TIM

b) SPI Slave Timing (CPHA = 1)

Figure A–15 SPI Timing Diagram (2 of 2)

Table A–9 EEPROM Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic		Temperature Range			Unit
		–40 to 85°C	–40 to 105°C	–40 to 125°C	
Programming Time (Note 1)	<1.0 MHz, RCO Enabled 1.0 to 2.0 MHz, RCO Disabled ≥2.0 MHz (or Anytime RCO Enabled)	10 20 10	15 Must use RCO 15	20 Must use RCO 20	ms
Erase Time (Note 1)	Byte, Row and Bulk	10	10	10	ms
Write/Erase Endurance (Note 2)		10,000	10,000	10,000	Cycles
Data Retention (Note 2)		10	10	10	Years

NOTES:
1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

Table A–9a EEPROM Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic		Temperature Range –20 to 70°C	Unit
Programming Time (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled 5 V, E ≤ 2.0 MHz, RCO Enabled	25 10	ms ms
Erase Time (Byte, Row and Bulk) (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled 5 V, E ≤ 2.0 MHz, RCO Enabled	25 10	ms ms
Write/Erase Endurance (Note 2)		10,000	Cycles
Data Retention (Note 2)		10	Years

NOTES:
1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

APPENDIX B
MECHANICAL DATA AND ORDERING INFORMATION

M68HC11 E-series microcontrollers are available in 52-pin plastic leaded chip carrier (PLCC), 52-pin windowed ceramic leaded chip carrier (CLCC), 64-pin quad flat pack (QFP), 52-pin thin quad flat pack (TQFP), and 56-pin dual in-line package with .070" lead spacing (SDIP). In addition to these packages, the MC68HC811E2 is available in a 48-pin plastic DIP (.100" lead spacing). Refer to **Table B–1**, **Table B–2**, and **Table B–3** for ordering information.

B.1 Ordering Information

Use the information in **Table B–1, Table B–2**, and **Table B–3** to specify the appropriate device when placing an order.

Table B–1 Standard Device Ordering Information

Package	Description	CONFIG	Temperature	Frequency	MC Order Number
52-Pin PLCC	BUFFALO ROM	$0F	–40° to +85° C	2 MHz	MC68HC11E9BCFN2
				3 MHz	MC68HC11E9BCFN3
	No ROM	$0D	–40° to +85° C	2 MHz	MC68HC11E1CFN2
				3 MHz	MC68HC11E1CFN3
			–40° to +105° C	2 MHz	MC68HC11E1VFN2
			–40° to +125° C	2 MHz	MC68HC11E1MFN2
	No ROM, No EEPROM	$0C	–40° to +85° C	2 MHz	MC68HC11E0CFN2
				3 MHz	MC68HC11E0CFN3
			–40° to +105° C	2 MHz	MC68HC11E0VFN2
			–40° to +125° C	2 MHz	MC68HC11E0MFN2
	OTPROM	$0F	–40° to +85° C	2 MHz	MC68HC711E9CFN2
				3 MHz	MC68HC711E9CFN3
			–40° to +105° C	2 MHz	MC68HC711E9VFN2
			–40° to +125° C	2 MHz	MC68HC711E9MFN2
	OTPROM, Enhanced Security Feature	$0F	–40° to +85° C	2 MHz	MC68S711E9CFN2
	20 Kbytes OTPROM	$0F	0° to +70° C	3 MHz	MC68HC711E20FN3
			–40° to +85° C	2 MHz	MC68HC711E20CFN2
				3 MHz	MC68HC711E20CFN3
			–40° to +105° C	2 MHz	MC68HC711E20VFN2
			–40° to +125° C	2 MHz	MC68HC711E20MFN2
	No ROM, 2 Kbytes EEPROM	$FF	0° to +70° C	2 MHz	MC68HC811E2FN2
			–40° to +85° C	2 MHz	MC68HC811E2CFN2
			–40° to +105° C	2 MHz	MC68HC811E2VFN2
			–40° to +125° C	2 MHz	MC68HC811E2MFN2
64-Pin QFP	BUFFALO ROM	$0F	–40° to +85° C	2 MHz	MC68HC11E9BCFU2
				3 MHz	MC68HC11E9BCFU3
	No ROM	$0D	–40° to +85° C	2 MHz	MC68HC11E1CFU2
				3 MHz	MC68HC11E1CFU3
			–40° to +105° C	2 MHz	MC68HC11E1VFU2
	No ROM, No EEPROM	$0C	–40° to +85° C	2 MHz	MC68HC11E0CFU2
			–40° to +105° C	2 MHz	MC68HC11E0VFU2
	20 Kbytes OTPROM	$0F	0° to +70° C	3 MHz	MC68HC711E20FU3
			–40° to +85° C	2 MHz	MC68HC711E20CFU2
				3 MHz	MC68HC711E20CFU3
			–40° to +105° C	2 MHz	MC68HC711E20VFU2
			–40° to +125° C	2 MHz	MC68HC711E20MFU2
52-Pin TQFP (10 mm X 10 mm)	BUFFALO ROM	$0F	–40° to +85° C	2 MHz	MC68HC11E9BCPB2
				3 MHz	MC68HC11E9BCPB3

Table B–1 Standard Device Ordering Information (Continued)

Package	Description	CONFIG	Temperature	Frequency	MC Order Number
52-Pin CLCC (Windowed)	EPROM	$0F	–40° to +85° C	2 MHz	MC68HC711E9CFS2
				3 MHz	MC68HC711E9CFS3
			–40° to +105° C	2 MHz	MC68HC711E9VFS2
			–40° to +125° C	2 MHz	MC68HC711E9VFS2
	20 Kbytes EPROM	$0F	0° to +70° C	3 MHz	MC68HC711E20FS3
			–40° to +85° C	2 MHz	MC68HC711E20CFS2
				3 MHz	MC68HC711E20CFS3
			–40° to +105° C	2 MHz	MC68HC711E20VFS2
			–40° to +125° C	2 MHz	MC68HC711E20MFS2
48-Pin DIP (MC68HC811 E2 only)	No ROM, 2 Kbytes EEPROM	$FF	0° to +70° C	2 MHz	MC68HC811E2P2
			–40° to +85° C	2 MHz	MC68HC811E2CP2
			–40° to +105° C	2 MHz	MC68HC811E2VP2
			–40° to +125° C	2 MHz	MC68HC811E2MP2
56-Pin SDIP (.070" Spac- ing)	BUFFALO ROM	$0F	–40° to +85° C	2 MHz	MC68HC11E9BCB2
				3 MHz	MC68HC11E9BCB3
	No ROM	$0D	–40° to +85° C	2 MHz	MC68HC11E1CB2
				3 MHz	MC68HC11E1CB3
			–40° to +105° C	2 MHz	MC68HC11E1VB2
			–40° to +125° C	2 MHz	MC68HC11E1MB2
	No ROM, No EEPROM	$0C	–40° to +85° C	2 MHz	MC68HC11E0CB2
				3 MHz	MC68HC11E0CB3
			–40° to +105° C	2 MHz	MC68HC11E0VB2
			–40° to +125° C	2 MHz	MC68HC11E0MB2

Table B–2 Custom ROM Device Ordering Information

Package	Description	Temperature	Frequency	MC Order Number
52-Pin PLCC	Custom ROM	0° to +70° C	3 MHz	MC68HC11E9FN3
		–40° to +85° C	2 MHz	MC68HC11E9CFN2
			3 MHz	MC68HC11E9CFN3
		–40° to +105° C	2 MHz	MC68HC11E9VFN2
		–40° to +125° C	2 MHz	MC68HC11E9MFN2
	Custom ROM, No EEPROM	0° to +70° C	3 MHz	MC68HC11E8FN3
		–40° to +85° C	2 MHz	MC68HC11E8CFN2
			3 MHz	MC68HC11E8CFN3
		–40° to +105° C	2 MHz	MC68HC11E8VFN2
		–40° to +125° C	2 MHz	MC68HC11E8MFN2
	20 Kbytes Custom ROM	0° to +70° C	3 MHz	MC68HC11E20FN3
		–40° to +85° C	2 MHz	MC68HC11E20CFN2
			3 MHz	MC68HC11E20CFN3
		–40° to +105° C	2 MHz	MC68HC11E20VFN2
		–40° to +125° C	2 MHz	MC68HC11E20MFN2
64-Pin QFP	Custom ROM	0° to +70° C	3 MHz	MC68HC11E9FU3
		–40° to +85° C	2 MHz	MC68HC11E9CFU2
			3 MHz	MC68HC11E9CFU3
		–40° to +105° C	2 MHz	MC68HC11E9VFU2
		–40° to +125° C	2 MHz	MC68HC11E9MFU2
	Custom ROM, No EEPROM	0° to +70° C	3 MHz	MC68HC11E8FU3
		–40° to +85° C	2 MHz	MC68HC11E8CFU2
			3 MHz	MC68HC11E8CFU3
		–40° to +105° C	2 MHz	MC68HC11E8VFU2
		–40° to +125° C	2 MHz	MC68HC11E8MFU2
	20 Kbytes Custom ROM	0° to +70° C	3 MHz	MC68HC11E20FU3
		–40° to +85° C	2 MHz	MC68HC11E20CFU2
			3 MHz	MC68HC11E20CFU3
		–40° to +105° C	2 MHz	MC68HC11E20VFU2
		–40° to +125° C	2 MHz	MC68HC11E20MFU2
52-Pin TQFP (10 mm X 10 mm)	Custom ROM	0° to +70° C	3 MHz	MC68HC11E9PB3
		–40° to +85° C	2 MHz	MC68HC11E9CPB2
			3 MHz	MC68HC11E9CPB3
		–40° to +105° C	2 MHz	MC68HC11E9VPB2
		–40° to +125° C	2 MHz	MC68HC11E9MPB2
	Custom ROM, No EEPROM	0° to +70° C	3 MHz	MC68HC11E8PB3
		–40° to +85° C	2 MHz	MC68HC11E8CPB2
			3 MHz	MC68HC11E8CPB3
		–40° to +105° C	2 MHz	MC68HC11E8VPB2
		–40° to +125° C	2 MHz	MC68HC11E8MPB2

Table B–2 Custom ROM Device Ordering Information (Continued)

Package	Description	Temperature	Frequency	MC Order Number
56-Pin SDIP (.070" Spacing)	Custom ROM	0° to +70° C	3 MHz	MC68HC11E9B3
		–40° to +85° C	2 MHz	MC68HC11E9CB2
			3 MHz	MC68HC11E9CB3
		–40° to +105° C	2 MHz	MC68HC11E9VB2
		–40° to +125° C	2 MHz	MC68HC11E9MB2
	Custom ROM, No EEPROM	0° to +70° C	3 MHz	MC68HC11E8B3
		–40° to +85° C	2 MHz	MC68HC11E8CB2
			3 MHz	MC68HC11E8CB3
		–40° to +105° C	2 MHz	MC68HC11E8VB2
		–40° to +125° C	2 MHz	MC68HC11E8MB2

Table B–3 Extended Voltage Device Ordering Information (3.0 Vdc to 5.5 Vdc)

Package	Description	Temperature	Frequency	MC Order Number
52-Pin PLCC	Custom ROM	–20° to +70° C	2 MHz	MC68L11E9FN2
	Custom ROM, No EEPROM		2 MHz	MC68L11E8FN2
	No ROM		2 MHz	MC68L11E1FN2
	No ROM, No EEPROM		2 MHz	MC68L11E0FN2
64-Pin QFP	Custom ROM	–20° to +70° C	2 MHz	MC68L11E9FU2
	Custom ROM, No EEPROM		2 MHz	MC68L11E8FU2
	No ROM		2 MHz	MC68L11E1FU2
	No ROM, No EEPROM		2 MHz	MC68L11E0FU2
52-Pin TQFP (10 mm X 10 mm)	Custom ROM	–20° to +70° C	2 MHz	MC68L11E9PB2
	Custom ROM, No EEPROM		2 MHz	MC68L11E8PB2
	No ROM		2 MHz	MC68L11E1PB2
	No ROM, No EEPROM		2 MHz	MC68L11E0PB2
56-Pin SDIP (.070" Spacing)	Custom ROM	–20° to +70° C	2 MHz	MC68L11E9B2
	Custom ROM, No EEPROM		2 MHz	MC68L11E8B2
	No ROM		2 MHz	MC68L11E1B2
	No ROM, No EEPROM		2 MHz	MC68L11E0B2

B.2 Obtaining M68HC11 E-Series Mechanical Information

Although all devices manufactured by Motorola conform to current JDEC standards, complete mechanical information regarding M68HC11 E-series microcontrollers is available by facsimile through Motorola's MFAX system.

Users can obtain instructions on the use of this system by calling (602) 244-6609. The automated system will request that a fax number be entered. Once entered, a facsimile message will be sent containing the instructions.