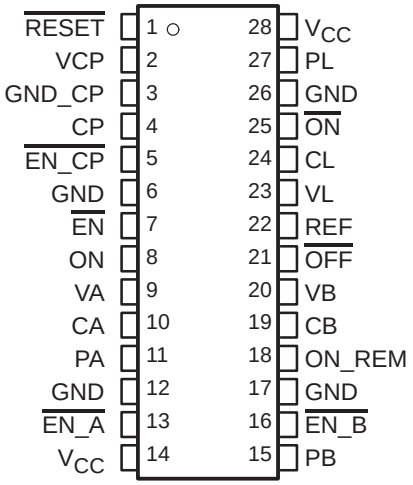
- **Complete Power Supply for Cellular Handsets**
- **Three Low-Dropout Regulators (LDOs) with 100-mV Dropout**
- **Less Than 1 μA Supply Current in Shutdown Typ**
- **250-ms Microprocessor Reset Output**
- **10-mA Charge-Pump Driver Configurable For Inverted or Doubled Output**
- **Separate Enables for LDOs and Charge Pump**
- **1.185-V Reference**
- **28-Pin TSSOP Package**

PW PACKAGE
(TOP VIEW)



description

The TPS9110 incorporates a complete power supply system for a cellular subscriber terminal that uses battery packs with three or four NiMH/NiCd cells or a single lithium-ion cell. The device includes three low-dropout linear regulators rated for 3.3 V or 3 V at 100 mA each, a charge-pump driver, and logic that includes a 250-ms reset, on/off control, and processor interface. Regulators A and B and the charge-pump driver have separate enables allowing circuitry to be powered up or down as necessary to conserve battery power. Regulators VL, VA, and VB, and the charge pump driver are active as soon as UVLO and OTP are valid and $\overline{ON}$ is toggled low.

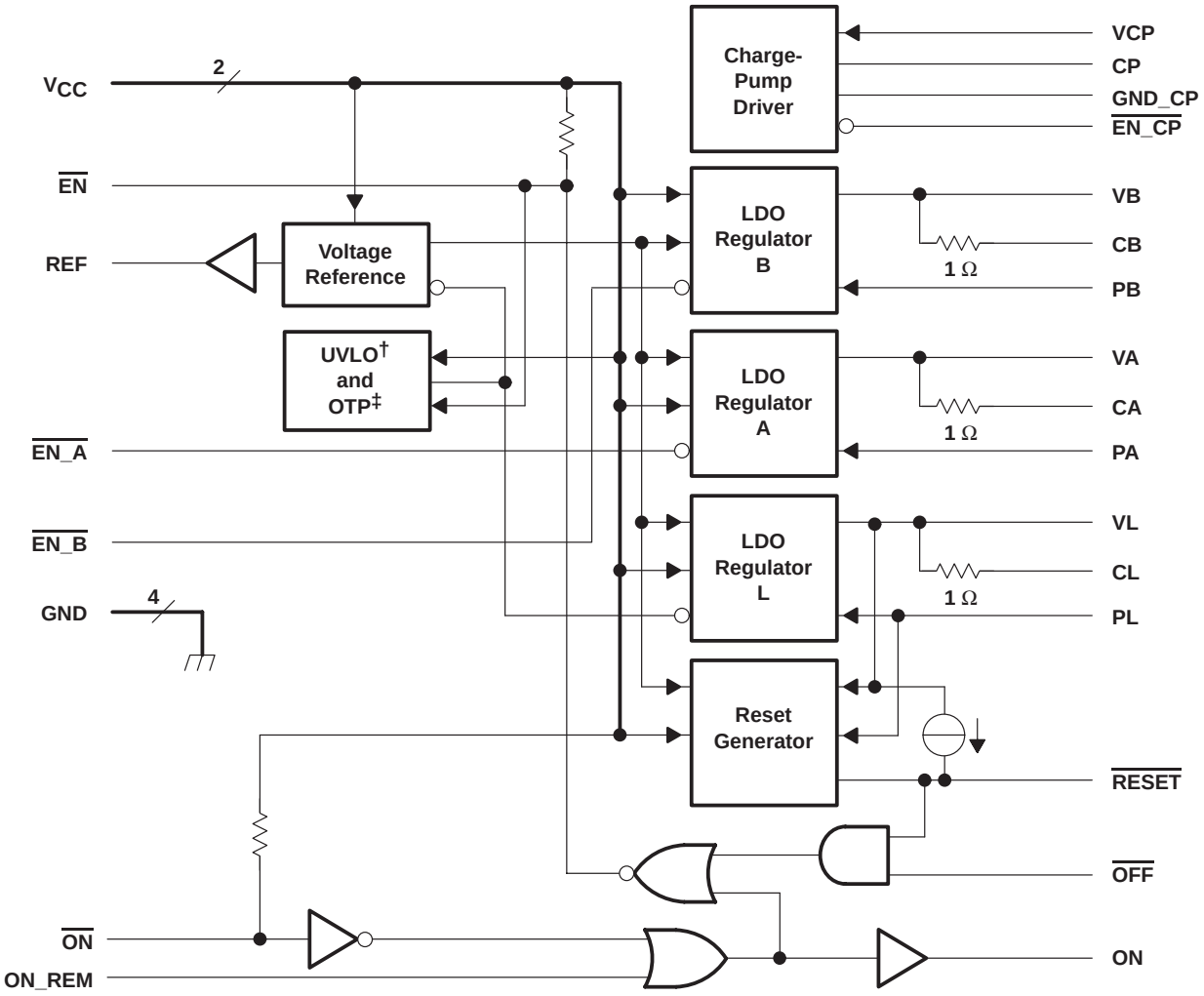
The TPS9110 operates over a free-air temperature range of –40°C to 85°C and is supplied in a 28-pin TSSOP package.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM
	TSSOP (PW)	(Y)
–40°C to 85°C	TPS9110IPWLE	TPS9110Y

The PW package is only available left-end taped and reeled.

functional block diagram

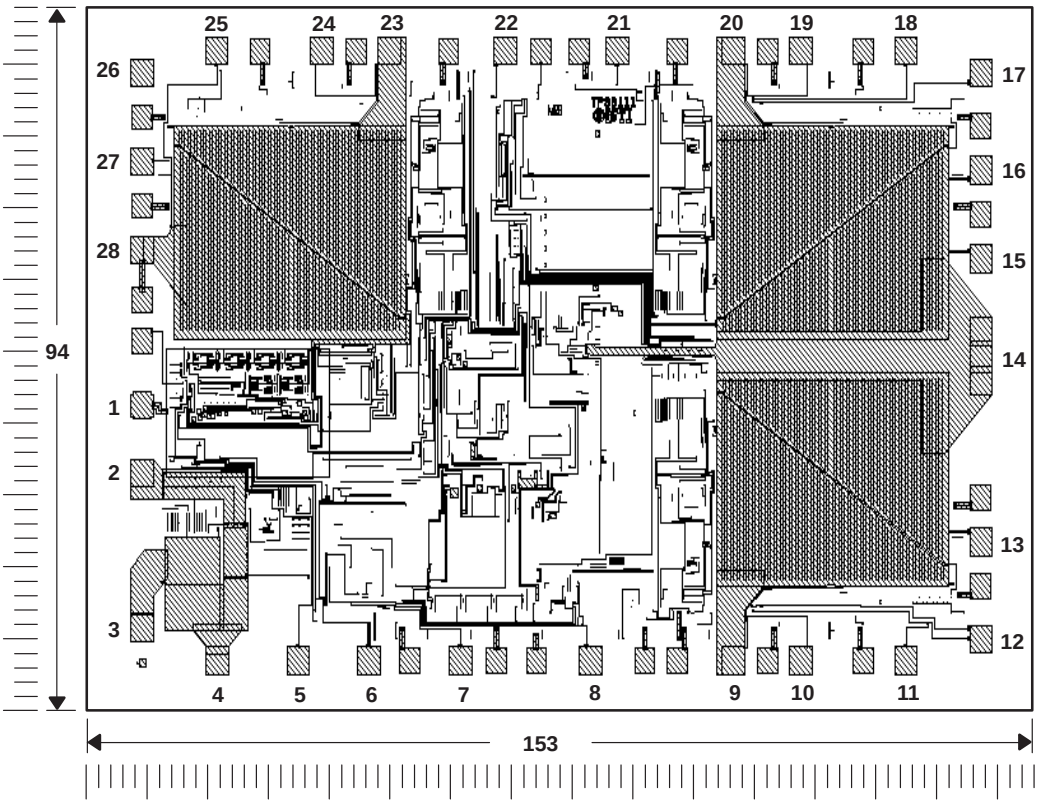


† UVLO - Undervoltage lockout
‡ OTP - Overtemperature protection

TPS9110Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS9110. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
3.3 × 3.3 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CA	10		Regulator A filter capacitor connection
$\overline{\text{EN\_A}}$	13	I	Regulator A enable input. A logic low on $\overline{\text{EN\_A}}$ turns on regulator A.
PA	11	I	Program A. PA provides programming input for regulator A.
VA	9	O	Regulator A output voltage
CB	19		Regulator B filter capacitor connection
$\overline{\text{EN\_B}}$	16	I	Regulator B enable input. A logic low on $\overline{\text{EN\_B}}$ turns on regulator B.
PB	15	I	Program B. PB provides programming input for regulator B.
VB	20	O	Regulator B output voltage
CL	24		Regulator L filter capacitor connection
PL	27	I	Program L. PL provides voltage programming input for regulator L.
VL	23	O	Regulator L output voltage
GND	6, 12, 17, 26		Ground. GND terminals should be externally connected to ground to ensure proper functionality.
REF	22	O	1.185-V reference output. Decouple REF with an external 0.01-μF to 0.1-μF capacitor to ground.
V_{CC}	14, 28		Supply voltage input. V_{CC} terminals are not connected internally and must be externally connected to ensure proper functionality.
CP	4	O	Charge pump driver output
$\overline{\text{EN\_CP}}$	5	I	Charge pump driver enable input. Logic low on $\overline{\text{EN\_CP}}$ turns on the charge pump.
GND_CP	3		Charge pump driver ground
VCP	2		Charge pump driver supply voltage
$\overline{\text{EN}}$	7	I/O	Enable signal input/output. A logic low on $\overline{\text{EN}}$ enables the TPS9110.
$\overline{\text{OFF}}$	21	I	Off-signal input. A logic low on $\overline{\text{OFF}}$ turns off the TPS9110.
ON	8	O	On-signal output. ON is the logical inversion of $\overline{\text{ON}}$.
$\overline{\text{ON}}$	25	I	On signal. A logic low on $\overline{\text{ON}}$ enables the TPS9110.
ON_REM	18	I	Remote on. A logic high on ON_REM enables the TPS9110.
$\overline{\text{RESET}}$	1	O	Microprocessor reset output. $\overline{\text{RESET}}$ is a logic low for 250 ms at power-up.

detailed description

voltage reference

The regulators and reset generator utilize an internal 1.185-V band-gap voltage reference. The reference is also buffered and brought out on REF for external use; REF can source a maximum of 2 mA. A 0.01-μF to 0.1-μF capacitor must be connected between REF and ground.

LDO regulators

The TPS9110 includes three low-dropout regulators, implemented with 1-Ω PMOS series-pass transistors, with quiescent supply currents of 100 μA. Each of the regulators can supply up to 100 mA of continuous output current. The 1-Ω PMOS series-pass transistor achieves the dropout voltage of 100 mV at the maximum-rated output current. Each regulator output voltage can be independently programmed to either 3.3 V or 3 V using its programming control input PL, PA or PB (Px). A logic low on Px sets the output voltage of the regulator to 3.3 V; a logic high sets it to 3 V.

Each LDO contains a current limit circuit. When the current demand on the regulator exceeds the current limit, the output voltage drops in proportion to the excess current. When the excess load current is removed, the output voltage returns to regulation. Exceeding the current limit on VL can disable the TPS9110. If enough current demand is placed on VL, the output voltage drops below the reset threshold voltage causing $\overline{\text{RESET}}$ to go low, effectively unlatching the enable.

VL is intended to be the primary supply voltage for the microprocessor and other system logic functions. VA and VB can power low-noise analog circuits and/or implement system power management. The enable terminals $\overline{\text{EN\_A}}$ and $\overline{\text{EN\_B}}$ are utilized to power down circuitry when it is not required. $\overline{\text{EN\_A}}$ and $\overline{\text{EN\_B}}$ are TTL-compatible inputs with 10-μA active current-source pullups. A logic low enables the respective regulator while a logic high pulls the regulator output voltage to ground and reduces the regulator quiescent current to leakage levels.

Stability of the LDOs is ensured by the addition of compensation terminals CL, CA, and CB, which connect to the output of the regulator through an internal 1-Ω resistor. This compensation scheme allows for capacitors with equivalent series resistance (ESR) of up to 15 Ω, eliminating the need for expensive, low-ESR capacitors.

reset generator

$\overline{\text{RESET}}$ is a microprocessor reset signal that goes to logic low at power-up, or whenever VL drops below 2.93 V (2.6 V for 3-V applications), and remains in that state for 250 ms after VL exceeds the $\overline{\text{RESET}}$ threshold (see Figure 5). The open-drain output has a 30-μA pullup that eliminates the need for an external pullup resistor and still allows it to be connected with other open-drain or open-collector signals. $\overline{\text{RESET}}$ is valid for supply voltages as low as 1.5 V.

$\overline{\text{ON}}$, $\overline{\text{OFF}}$, ON, ON_REM and $\overline{\text{EN}}$ functions

The $\overline{\text{ON}}$ input is intended to be the main enable for the TPS9110 and should be connected to ground through a pushbutton switch. Once the switch is pressed, internal logic pulls $\overline{\text{EN}}$ low. $\overline{\text{EN}}$ is designed to sink 3.2 mA and can be used as a pulldown to enable other functions on the TPS9110 or other system circuitry. When $\overline{\text{EN}}$ is pulled low, the TPS9110 checks to make sure the supply voltage is above the undervoltage lockout (UVLO) threshold voltage and the die temperature is below 160°C. If both of these conditions are met, the reference circuitry, regulator L, reset generator, and other support circuitry are enabled. When $\overline{\text{RESET}}$ goes high, the system can respond with a logic high on $\overline{\text{OFF}}$, which latches the TPS9110 on, and the $\overline{\text{ON}}$ pushbutton can then be released.

The TPS9110 is disabled in a similar manner. If the $\overline{\text{ON}}$ pushbutton is pressed while the TPS9110 is enabled, ON responds with a logic high. Once this logic high is detected, the system can respond with a logic low on $\overline{\text{OFF}}$, disabling the TPS9110 and reducing supply currents to 1 μA (see Figure 1).

$\overline{ON}$, $\overline{OFF}$, ON, ON_REM and $\overline{EN}$ functions (continued)

ON_REM can be used in the same manner as $\overline{ON}$ in enabling or disabling the TPS9110. The signal is provided as a system interface to increase the flexibility of the system. $\overline{EN}$ can also be used as an input wired-OR open collector/drain to enable the TPS9110; however, it does not produce a logic signal on ON and, therefore, cannot be used in the disable sequence described above. It is not recommended that $\overline{EN}$ be used as the primary enable signal for the TPS9110.

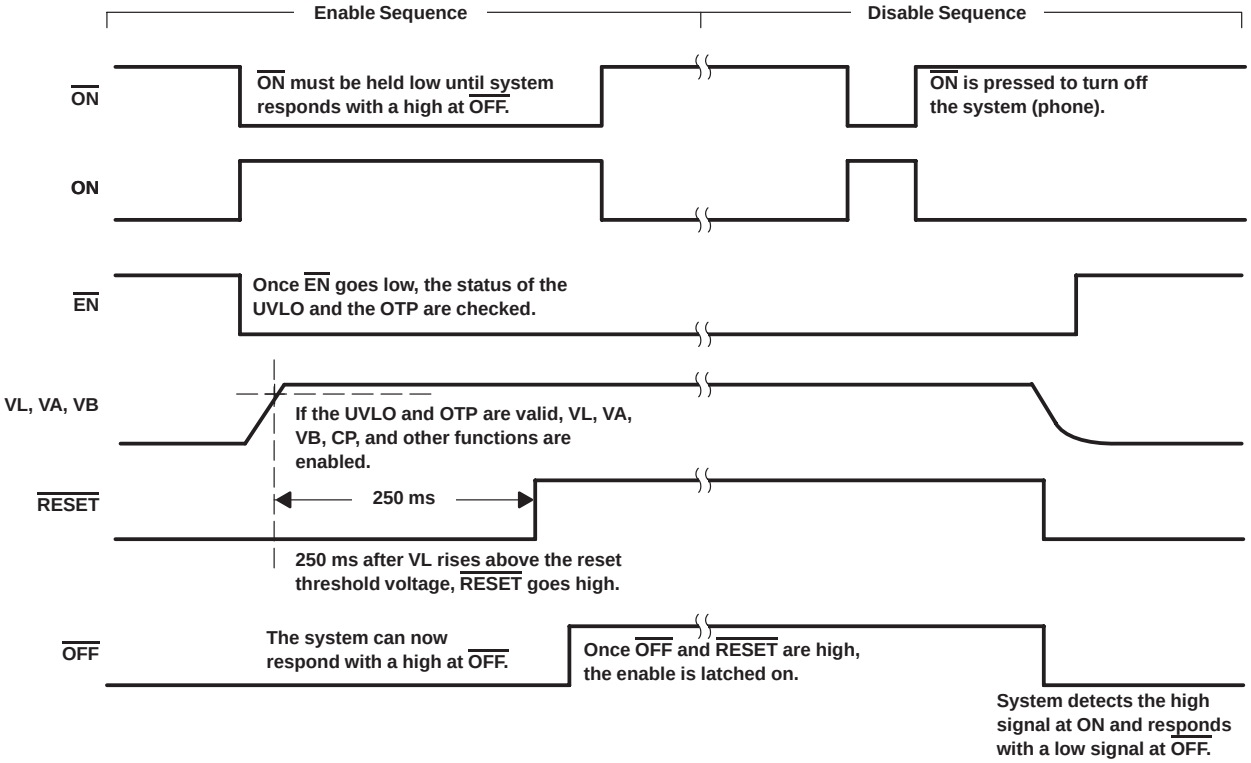


Figure 1. Recommended Enable and Disable Sequence

undervoltage lockout (UVLO)

UVLO prevents operation of the functions in the TPS9110 until the supply voltage exceeds the threshold voltage, eliminating abnormal power-up conditions internally and externally, and providing an orderly turn-on.

overtemperature shutdown

When the die temperature exceeds 160°C, the thermal protection circuit shuts off the TPS9110. When the die temperature drops below 150°C, the device can be restarted with the $\overline{ON}$ input.

charge pump driver

An unregulated inverting or doubler charge pump is implemented by connecting a network of two capacitors and two diodes to CP (see Figure 26). In the inverting configuration, the charge pump can power a liquid-crystal display (LCD) or provide gate bias for a GaAs power amplifier. A 5-V supply for flash-memory programming or powering the subscriber identity module (SIM) European applications can be achieved using the doubler configuration and an external LDO. A logic-low input to the charge-pump enable, $\overline{EN\_CP}$, turns on the oscillator and driver; a logic high turns them off. The charge pump driver can be turned on as soon as UVLO and OTP are valid and $\overline{ON}$ is toggled low. $\overline{EN\_CP}$ has an 10-μA internal pullup.

DISSIPATION RATING TABLE 1 – Free-Air Temperature

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – Case Temperature

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PW	4025 mW	32.2 mW/°C	2576 mW	2093 mW

MAXIMUM CONTINUOUS POWER DISSIPATION vs FREE-AIR TEMPERATURE

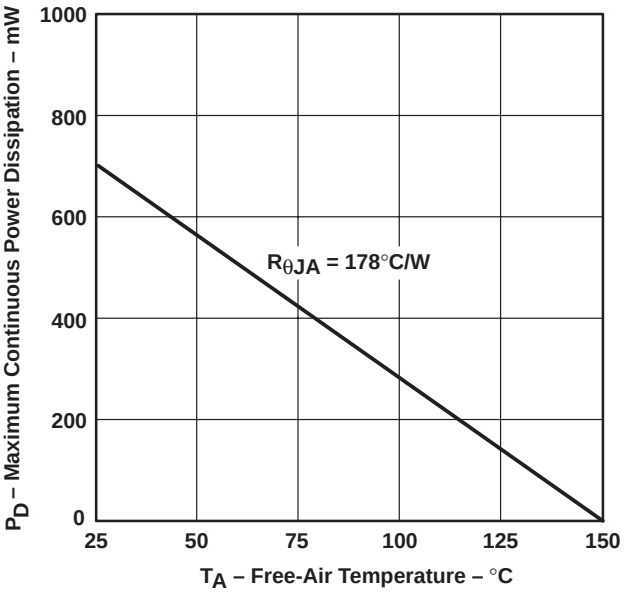


Figure 2

MAXIMUM CONTINUOUS POWER DISSIPATION vs CASE TEMPERATURE

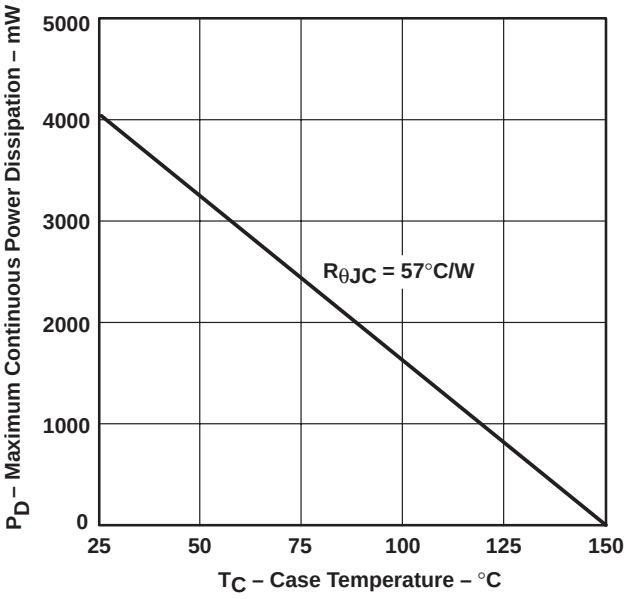


Figure 3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply voltage range, V_{CC}, VCP . . . . . –0.3 V to 12 V
Input voltage range at $\overline{OFF}$ . . . . . –0.3 V to 7 V
Input voltage range at PL, PA, PB, $\overline{EN}$, $\overline{EN\_A}$, $\overline{EN\_B}$, $\overline{ON}$, ON_REM, $\overline{EN\_CP}$ . . . . . –0.3 V to V_{CC}
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Peak output current . . . . . Internally limited
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}, VCP	3	10	V
Input voltage, $\overline{OFF}$	0	5	V
Input voltage at PL, PA, PB, $\overline{EN}$, $\overline{EN\_A}$, $\overline{EN\_B}$, $\overline{ON}$, ON_REM, $\overline{EN\_CP}$	0	V_{CC}	V
Reference output current	0	2	mA
Continuous regulator output current	0	100	mA
Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 μF (unless otherwise noted)

voltage reference (REF)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	T_A = 25°C,	I_O = 0		1.185		V
	4 V ≤ V_{CC} ≤ 10 V,	0 ≤ I_O ≤ 2 mA	1.161		1.209	V

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

LDO regulators

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage at VA, VB, VL (Vx)	T_A = 25°C		3.25	3.3	3.35	V
	0 ≤ $I_{O(Vx)}$ ≤ 100 mA,	3.5 V ≤ V_{CC} ≤ 10 V	3.2		3.4	V
	Px = V_{CC},	T_A = 25°C	2.95	3	3.05	V
	Px = V_{CC}, 3.2 V ≤ V_{CC} ≤ 10 V	0 ≤ $I_{O(Vx)}$ ≤ 100 mA,	2.9		3.10	V
Dropout voltage	$I_{O(Vx)}$ = 100 mA,	V_{CC} = 3.2 V		100	200	mV
Load regulation	$I_{O(Vx)}$ = 0 mA to 100 mA			30		mV
Line regulation	$I_{O(Vx)}$ = 100 mA,	V_{CC} = 3.5 V to 10 V		10		mV
Ripple rejection	f = 120 Hz			60		dB
Quiescent current (each regulator)				100		μA

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

charge pump driver

PARAMETER	MIN	TYP	MAX	UNIT
Frequency	50	100	150	kHz
Duty cycle		50%		
Output resistance		15	30	Ω

$\overline{\text{RESET}}$

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Input threshold voltage	VL voltage decreasing	2.871	2.93	2.989	V
Input threshold voltage	VL voltage decreasing, PL = V_{CC}	2.548	2.6	2.652	V
Timeout delay at $\overline{\text{RESET}}$	See Figure 5	125	250	375	ms
High-level output voltage	I_O = –40 µA	2.4			V
Low-level output voltage	I_O = 1 mA, V_{CC} = 1.5 V			0.4	V
	I_O = 3.2 mA			0.4	
Hysteresis			40		mV

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

logic inputs at $\overline{\text{EN\_A}}$, $\overline{\text{EN\_B}}$

PARAMETER	MIN	TYP	MAX	UNIT
High-level input voltage	2			V
Low-level input voltage			0.8	V
Input current	–20	–10	1	µA

logic inputs at PL, PA, PB, $\overline{\text{OFF}}$, ON_REM

PARAMETER	MIN	MAX	UNIT
High-level input voltage	2		V
Low-level input voltage		0.8	V
Input current	–1	1	µA

logic inputs at $\overline{\text{ON}}$‡

PARAMETER	MIN	MAX	UNIT
High-level input voltage	2		V
Low-level input voltage		0.8	V
Input current	–20	1	µA

‡ High and low level voltages are dependent on V_{CC} (see Figure 17).

logic inputs at $\overline{\text{EN}}$‡

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
High-level input voltage		2.4		V
Low-level input voltage			0.8	V
High-level output voltage	I_O = –50 µA $\overline{\text{OFF}}$ = 0	2.4		V
Low-level output voltage	I_O = 3.2 mA, $\overline{\text{ON}}$ = 0		0.4	V

‡ High and low-level input voltages are dependent on V_{CC} (see Figure 18).

logic outputs at ON

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
High-level output voltage	1-mA source current	2.4		V
Low-level output voltage	1-mA sink current		0.4	V

overtemperature shutdown

PARAMETER	MIN	TYP	MAX	UNIT
Temperature threshold		160		°C
Temperature hysteresis		10		°C

undervoltage lockout (UVLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Threshold voltage	V_{CC} increasing	1.80		2.52	V
Hysteresis			50		mV

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown	$\overline{OFF}$ = 0 V		0.5	10	μA
Operating	$\overline{EN\_CP}$ = VCP		0.7	1	mA

TPS9110Y electrical characteristics, T_J = 25°C, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 μF (unless otherwise noted)

voltage reference (REF)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	I_O = 0		1.185		V

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; the thermal effect must be taken into account separately.

LDO regulators

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage at VA, VB, VL (Vx)	$P_X = V_{CC}$	2.95	3	3.05	V
Dropout voltage	$I_{O(Vx)}$ = 100 mA, V_{CC} = 3.2 V		100		mV
Load regulation	$I_{O(Vx)}$ = 0 mA to 100 mA		30		mV
Line regulation	$I_{O(Vx)}$ = 100 mA, V_{CC} = 3.5 V to 10 V		10		mV
Ripple rejection	f = 120 Hz		60		dB
Quiescent current (each regulator)			100		μA

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

charge-pump driver

PARAMETER	MIN	TYP	MAX	UNIT
Frequency		100		kHz
Duty cycle		50%		
Output resistance		15		Ω

$\overline{RESET}$

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Threshold voltage	VL voltage decreasing		2.93		V
	VL voltage decreasing, PL = V_{CC}		2.6		
Delay	See Figure 5		250		ms
Hysteresis			40		mV

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

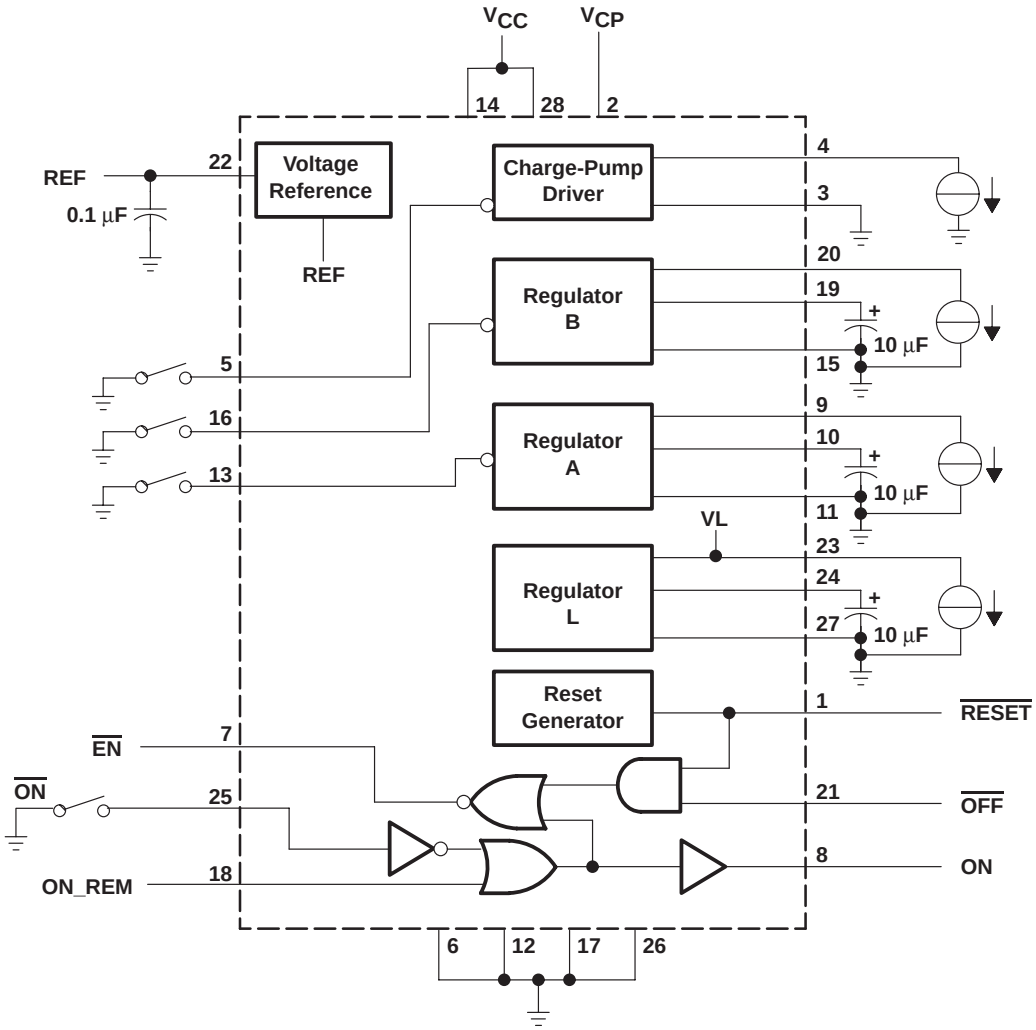


Figure 4. Test Circuit

PARAMETER MEASUREMENT INFORMATION

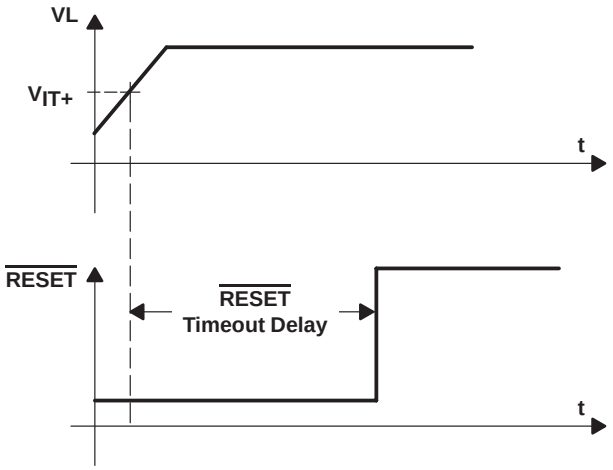


Figure 5. $\overline{RESET}$ Timing Diagram

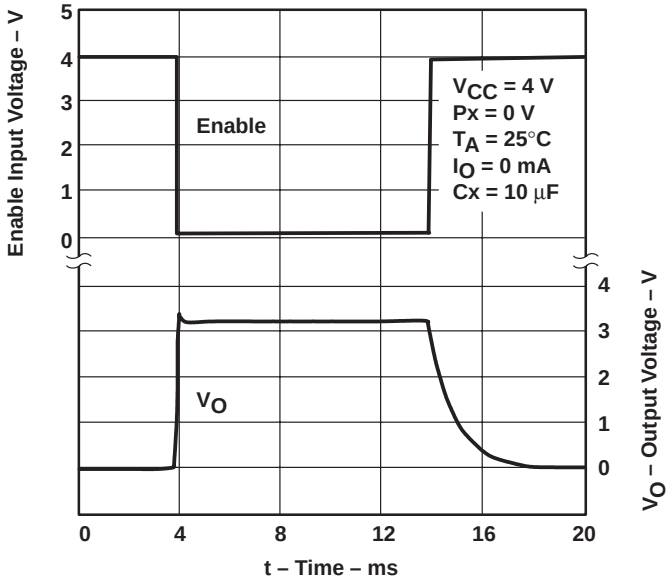


Figure 6. LDO-Regulator Output-Voltage Rise Time and Fall Time

PARAMETER MEASUREMENT INFORMATION

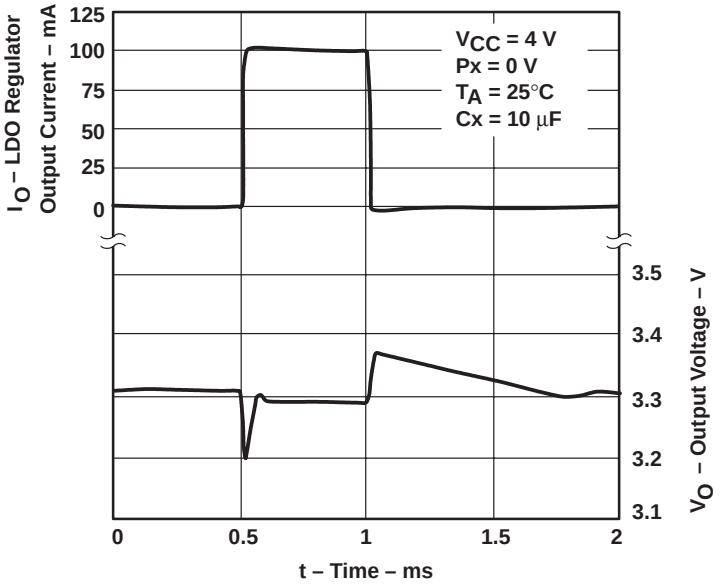


Figure 7. LDO-Regulator Load Transient, 1 mA to 100 mA Pulsed Load

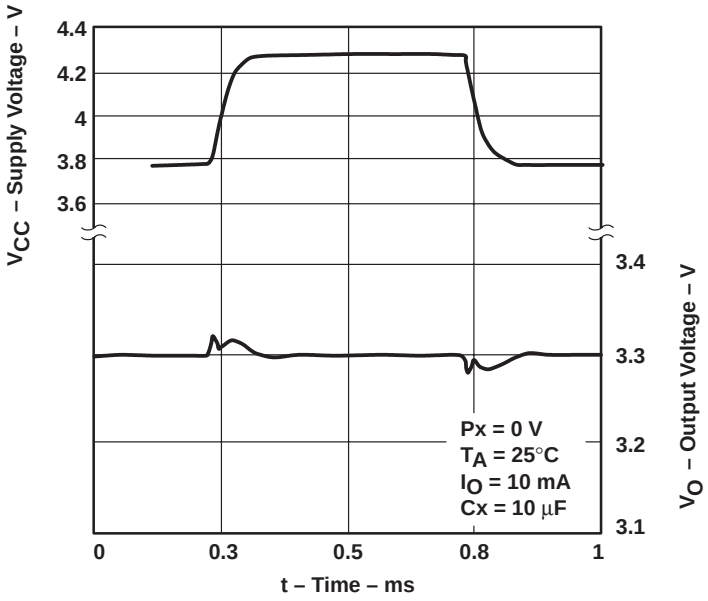


Figure 8. LDO-Regulator Line Transient

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{CC}	Quiescent current	vs Supply voltage	9
	Dropout voltage	vs Output current	10
		vs Junction temperature	11
ΔV_O	Change in output voltage	vs Junction temperature	12
V_O	Output voltage, VL	vs Supply voltage	13
ΔV_O	Change in output voltage	vs Supply voltage	14
ΔV_O	Change in output voltage	vs Output current	15
I_{CC}	Shutdown current	vs Supply voltage	16
	Input threshold voltage, $\overline{ON}$	vs Supply voltage	17
	Input threshold voltage, $\overline{EN}$	vs Supply voltage	18
	Input threshold voltage, ON_REM	vs Supply voltage	19
	Ripple rejection	vs Frequency	20
	Output spectral noise density	vs Frequency	21
	Change in frequency, CP	vs Junction temperature	22
r_O	Output resistance into CP	vs Supply voltage	23
r_O	Output resistance out of CP	vs Supply voltage	24

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE

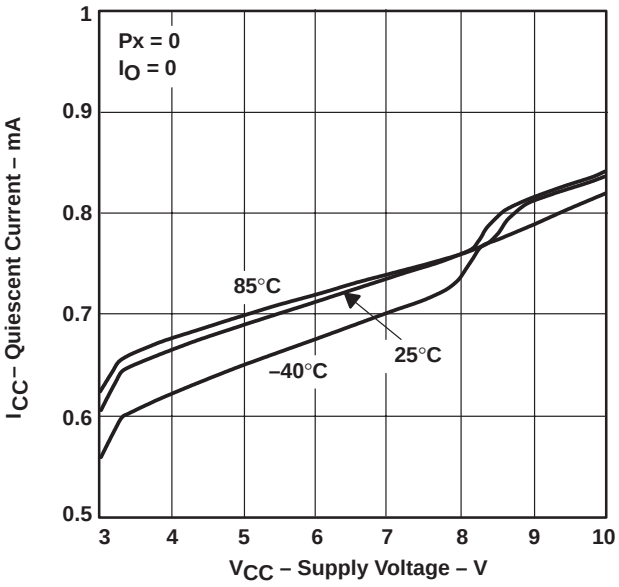


Figure 9

LDO REGULATORS
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

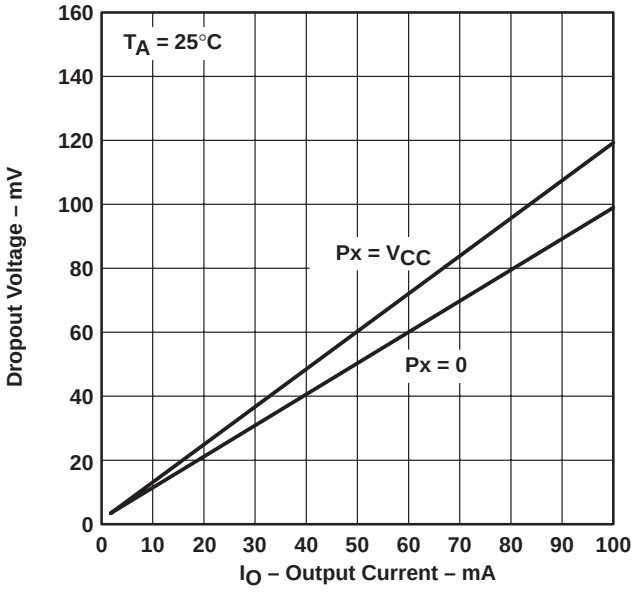


Figure 10

TYPICAL CHARACTERISTICS

LDO REGULATORS
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

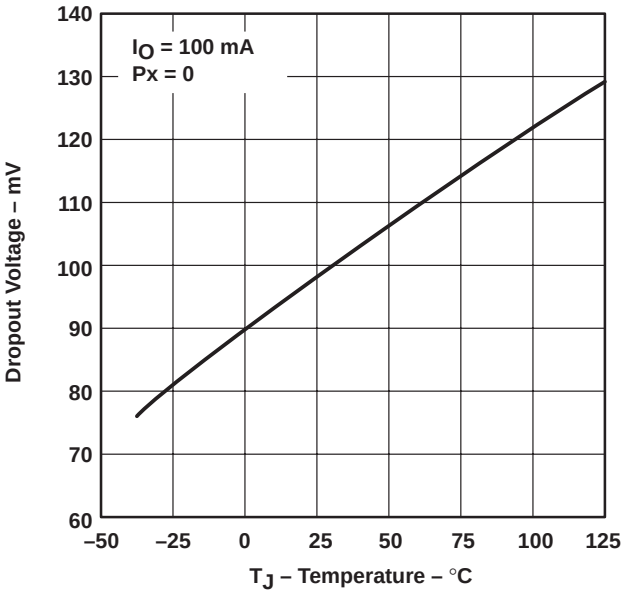


Figure 11

LDO REGULATORS
CHANGE IN OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

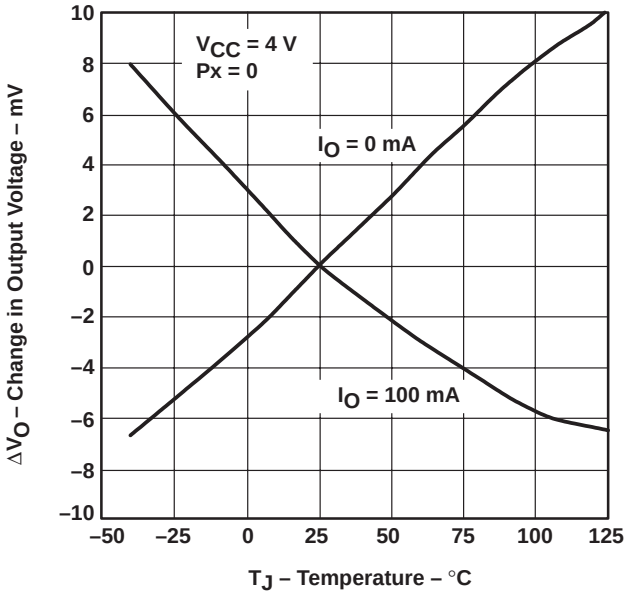


Figure 12

REGULATOR L
OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

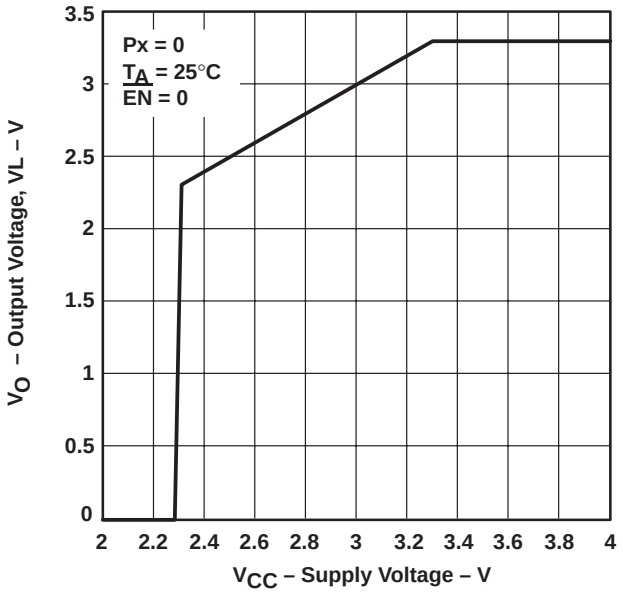


Figure 13

LDO REGULATORS
CHANGE IN OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

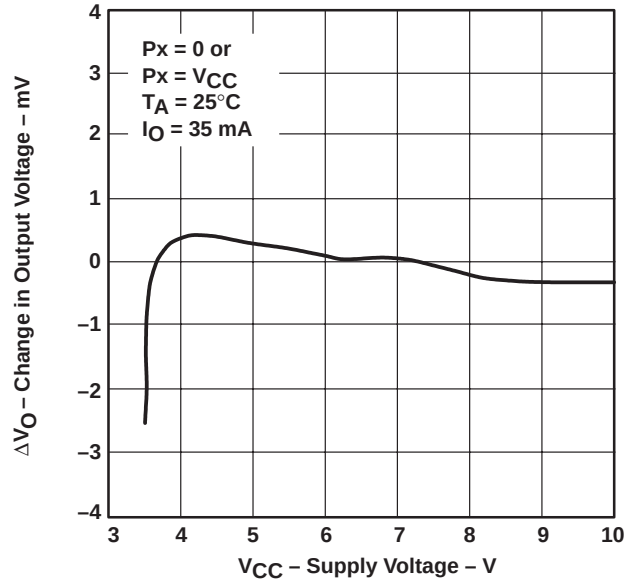


Figure 14

TYPICAL CHARACTERISTICS

LDO REGULATORS
CHANGE IN OUTPUT VOLTAGE vs OUTPUT CURRENT

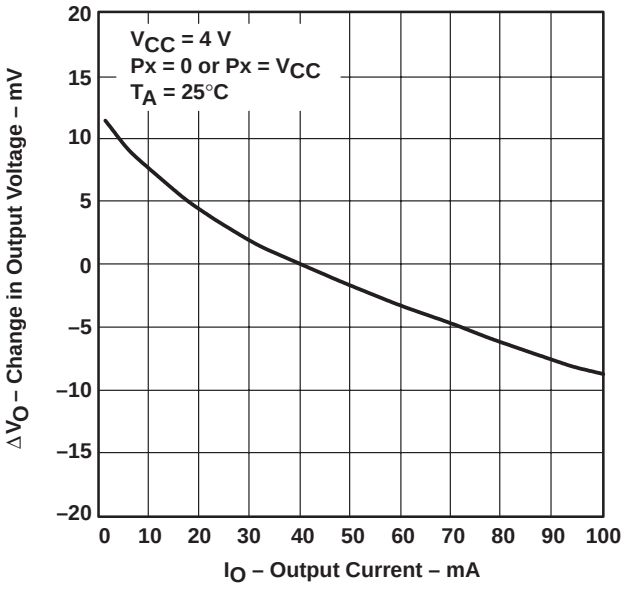


Figure 15

SHUTDOWN CURRENT vs SUPPLY VOLTAGE

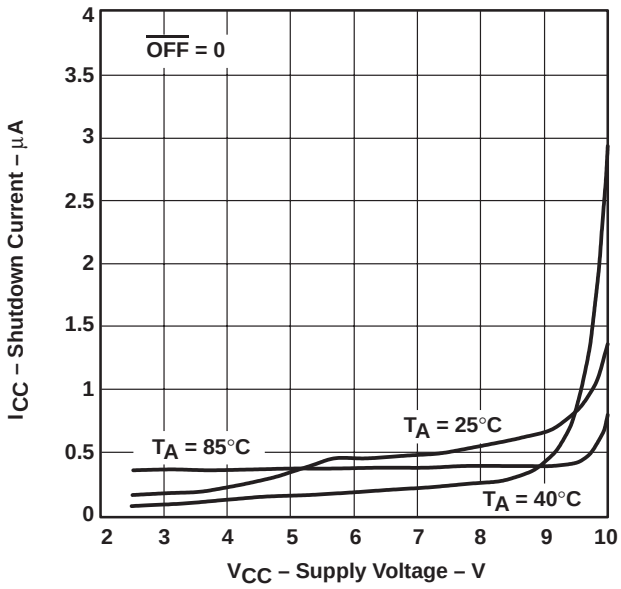


Figure 16

INPUT THRESHOLD VOLTAGE, $\overline{ON}$ vs SUPPLY VOLTAGE

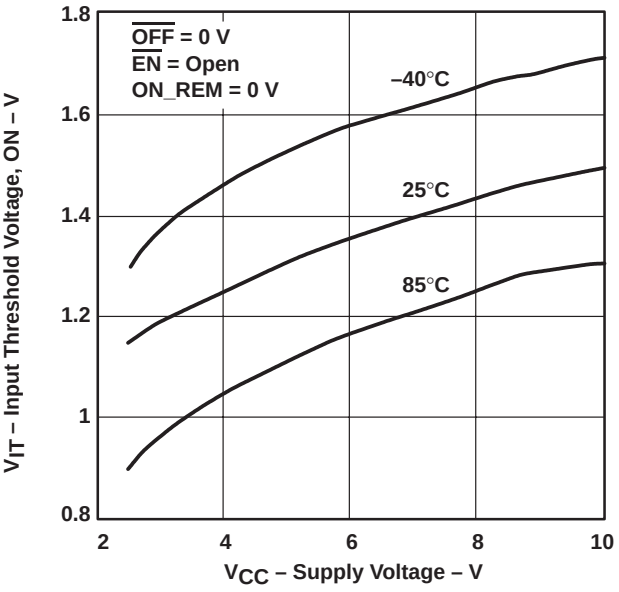


Figure 17

INPUT THRESHOLD VOLTAGE, $\overline{EN}$ vs SUPPLY VOLTAGE

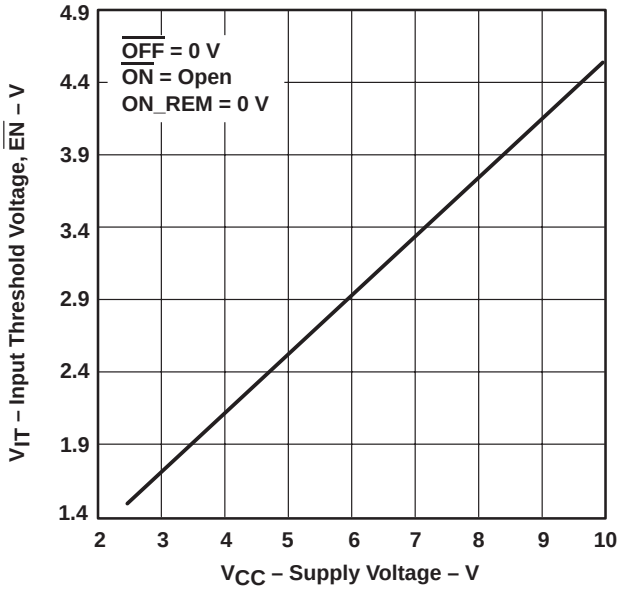


Figure 18

TYPICAL CHARACTERISTICS

INPUT THRESHOLD VOLTAGE, ON_REM vs SUPPLY VOLTAGE

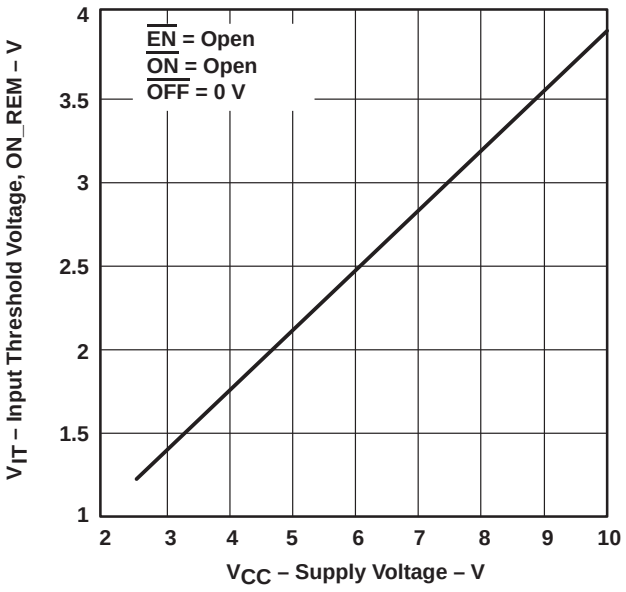


Figure 19

LDO REGULATORS
RIPPLE REJECTION vs FREQUENCY

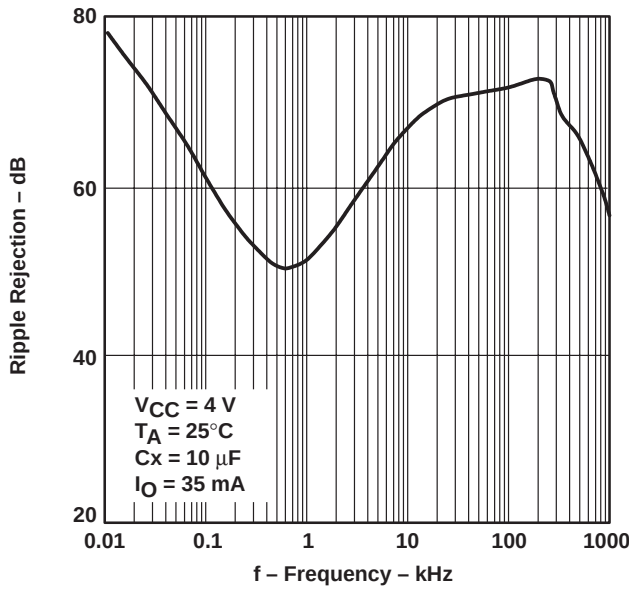


Figure 20

REGULATOR L
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

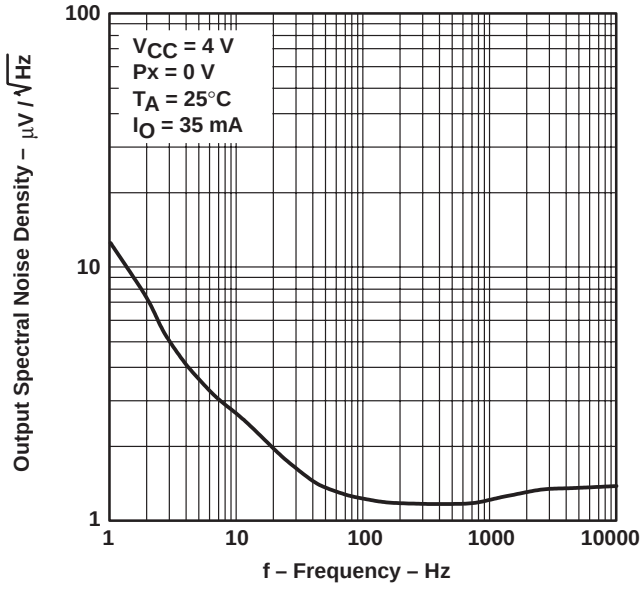


Figure 21

CHANGE IN FREQUENCY, CP vs JUNCTION TEMPERATURE

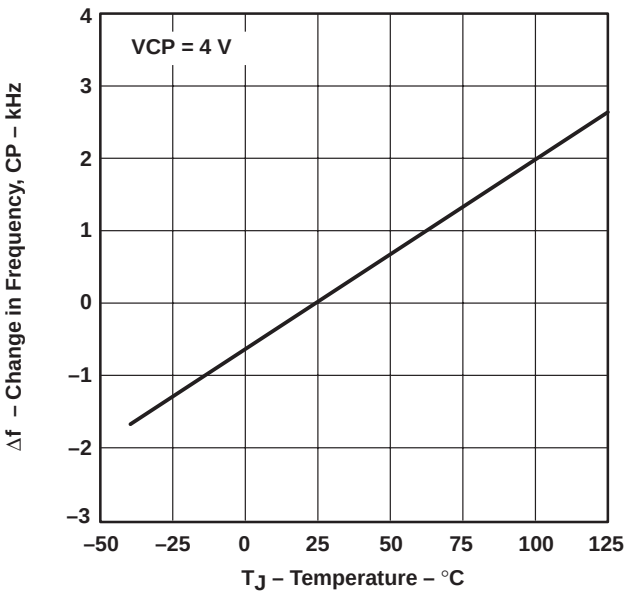


Figure 22

TYPICAL CHARACTERISTICS

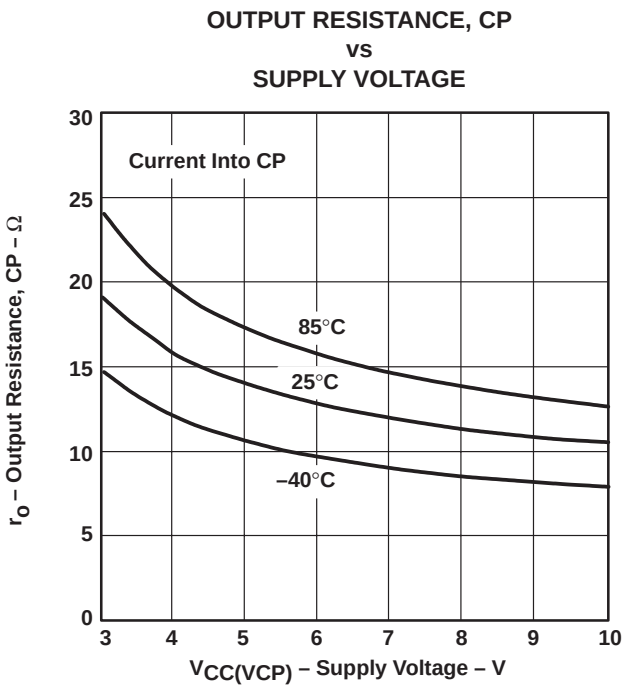


Figure 23

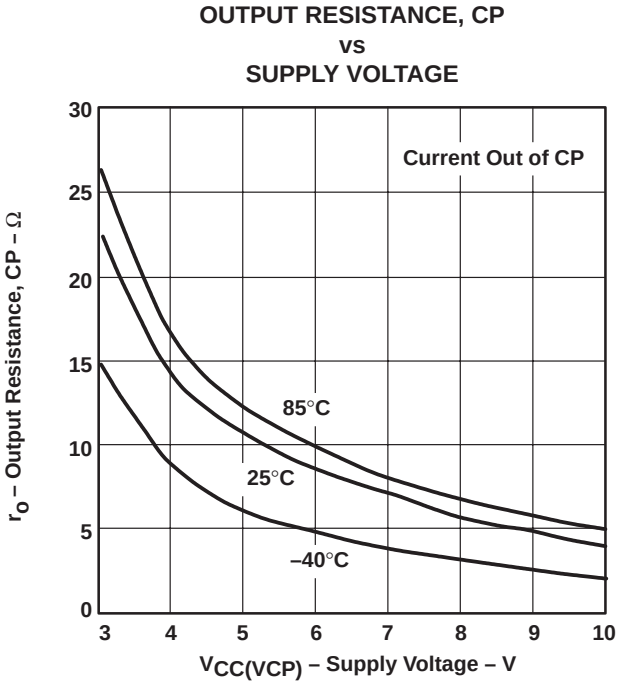


Figure 24

THERMAL INFORMATION

Using thermal resistance, junction-to-ambient ($R_{\theta JA}$), maximum power dissipation can be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

Where $T_{J(max)}$ is the maximum allowable junction temperature or 150°C.

This limit should then be applied to the internal power dissipation of the TPS9110. The equation for calculating total internal power dissipation of the TPS9110 is:

$$P_{D(max)} = \sum_{x} \left(V_I - V_X\right) \times I_X + V_I \times I_Q$$

Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

APPLICATION INFORMATION

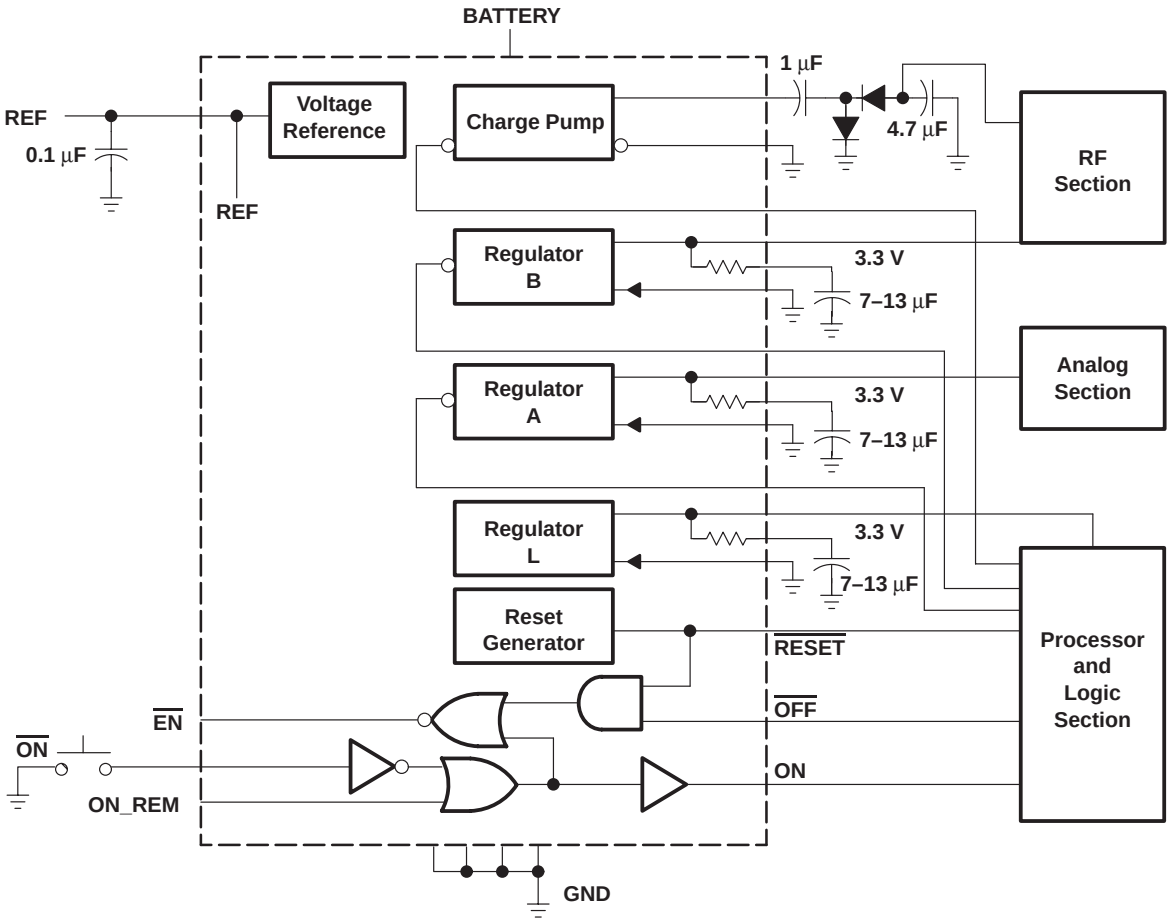


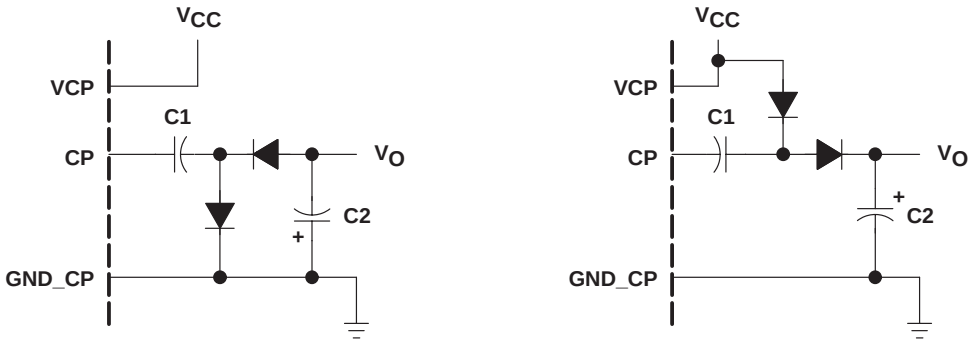
Figure 25. Typical Application

LDOs (VL, VA, VB) output capacitors

A 10-μF capacitor must be tied to Cx (CL, CA, or CB). The Cx terminal is connected internally to the output of the LDO through a 1-Ω resistor. The stability of LDOs is dependent on the ESR of the output filter capacitor. Most LDOs are designed to be stable over a narrow range of ESR with lower limits and upper limits, thus limiting the type of capacitor that can be used. With the use of the internal 1-Ω resistor, the lower ESR limit of the capacitor is eliminated, permitting the upper limit to be raised. Therefore, almost any tantalum or ceramic capacitor can be used, provided the ESR does not exceed 15 Ω over operating temperature range.

APPLICATION INFORMATION

charge pump design



a. Voltage Inverter

b. Voltage Doubler

Figure 26. Charge-Pump Configurations

The charge-pump terminal can drive either a voltage inverter or a voltage doubler. In either case only two capacitors and two signal diodes are needed. The output voltage is unregulated and a regulator may be added if needed.

The charge transfer of C1 is:

$$\Delta q = C1 \times (V_{CC} - V_O)$$

This occurs f times a second and the charge transfer per unit time (current) is:

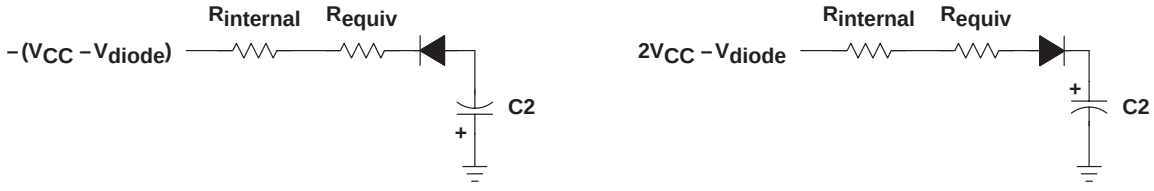
$$I = f \times C1 \times (V_{CC} - V_O)$$

Rewriting this equation in the form of I = V/R gives:

$$I = \frac{V_{CC} - V_O}{\frac{1}{f \times C1}}$$

where $\frac{1}{f \times C1}$ is an equivalent resistor.

An equivalent circuit can now be drawn taking the diodes into account.



a. Voltage Inverter

b. Voltage Doubler

Figure 27. Equivalent Circuit for Charge Pump

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APPLICATION INFORMATION

charge-pump design (continued)

The output voltage for the doubler is then:

$$V_O = 2 \times V_{CC} - 2 \times V_{diode} - I_O \times R_{total}$$

and the output voltage for the inverter is:

$$V_O = -(V_{CC} - 2 \times V_{diode}) + I_O \times R_{total}$$

To determine the size of C1 use:

$$C = \frac{I}{f \times \Delta V}$$

where f = 100,000 and ΔV = ripple voltage.

For an output current of 10 mA calculate:

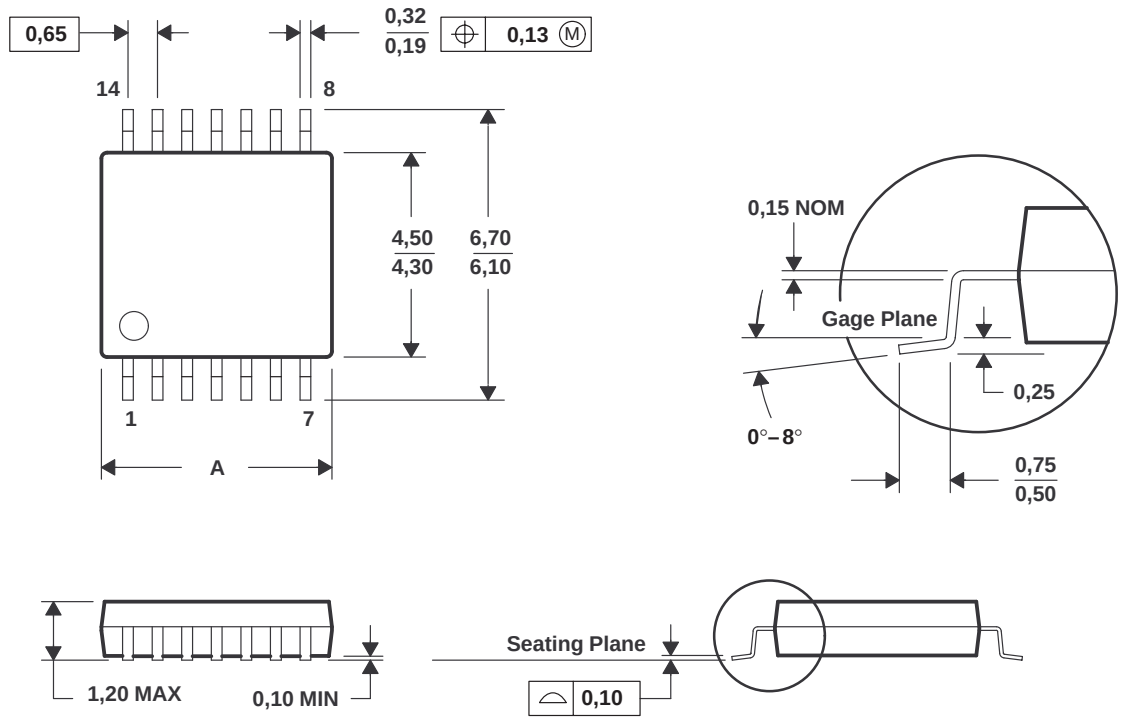
$$C1 = \frac{0.01\ A}{100\ kHz \times 0.1\ V_{ripple}} = 1\mu F$$

Because of losses caused by diode switching and ESR, the calculated capacitance should be multiplied by 1.5 to 2. A 2-μF capacitance should drive a 10-mA voltage doubler or inverter.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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