BGF106C

SIM Card Interface Filter and ESD Protection

Small Signal Discretes



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Revision History: 2009-04-14, V2.0

Previous Version: 2009-03-31, V1.0

Page	Subjects (major changes since last revision)
all	target status removed
5	Table 1: maximum voltage on all pins increased to 5.5 V

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Features

- · ESD protection circuit and interface filter for SIM cards
- ESD protection according to IEC61000-4-2 for \pm 15 kV contact discharge on external IOs
- Wafer level package with SnAgCu solder balls
- 400 μm solder ball pitch
- RoHS and WEEE compliant package



WLP-8-11-N-3D



Description

BGF106C is an ESD protection circuit and filtering interface for SIM cards. All external IOs are protected against ESD pulses of ± 15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green lead-free and halogen-free package with a size of only 1.2 mm x 1.2 mm and a total height of 0.6 mm

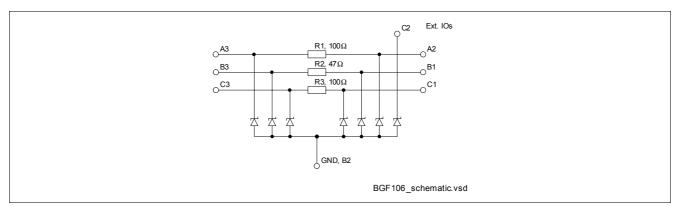


Figure 1 Schematic

Туре	Package	Marking	Chip
BGF106C	WLP-8-11	6C	N0727



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Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage at all pins to GND	V_{P}	0	_	5.5	V	_
Operating temperature range	T_{OP}	-40	_	+85	°C	_
Storage temperature range	T_{STG}	-65	_	+150	°C	_
Summed up input power for all pins	P_{in}	_	_	60	mW	T _S < 70 °C
Electrostatic discharge according to IEC610	000-4-2		<u>'</u>			
Contact discharge at internal pins A3, B3, C3 to any other pin	V_{ESD}	-2	_	2	kV	_
Contact discharge at external pins A2, B1, C1, C2 to GND	V_{ESD}	-15	-	15	kV	_

Table 2 Electrical Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Resistors R_1 , R_3	R _{1,3}	80	100	120	Ω	_
Resistor R ₂	R_2	37.6	47	56.4	Ω	_
Reverse current of ESD protection diodes	I_{R}		1 2	100 1000	nA nA	V = 3 V V = 5 V
Breakdown voltage of ESD diodes	$V_{(BR)}$	6.5	7.8	_	V	$I_{(BR)} = 1 \text{ mA}$
Line capacitance Capacitance of all lines to GND	C_{T}	-	16.5	20	pF	V = 0 V

¹⁾ at $T_{\rm A}$ = 25 °C



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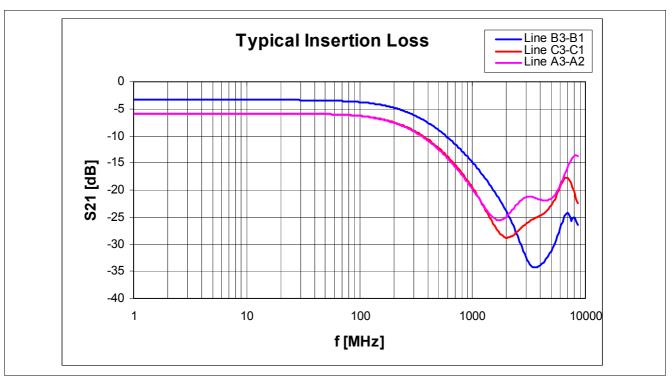


Figure 2 Insertion loss, $Z_S = Z_L = 50 \Omega$

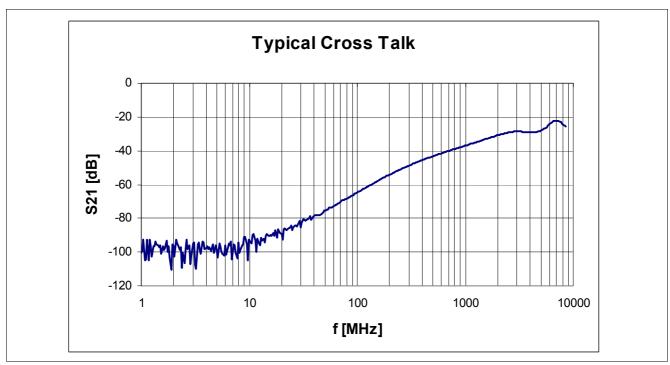


Figure 3 Cross talk, Z_S = Z_L =50 Ω (all unused input and output pins are terminated with 50 Ω)



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Package Outlines

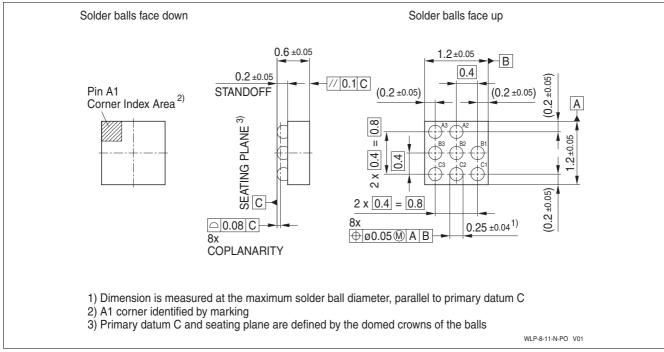


Figure 4 WLP-8-11 (Wafer Level Package)

Footprint

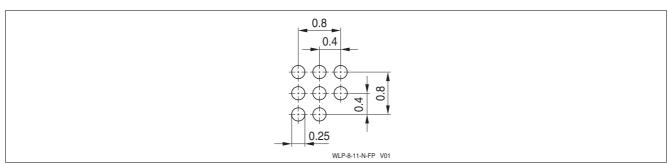


Figure 5 Recommended PCB pad design for reflow soldering

Tape

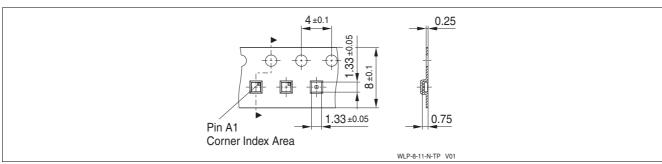


Figure 6 Tape for BGF106C / WLP-8-11

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