Preliminary Data Sheet
June 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7230A Primary Access Framer/Controller

Features

- Framing formats
  - — DS1 extended superframe (ESF)
  - — DS1 superframe (SF): D4; *SLC*®-96; T1DM DDS; T1DM DDS with FDL access
  - — DS1 independent transmit and receive framing modes when using the ESF and D4 formats
  - — ITU-CEPT 2.048 Mbits/s basic frame
  - — ITU-CEPT selectable CRC-4 multiframe alignment algorithms: 100 ms timer; 400 ms interworking timer. Optional basic frame resynchronization with >915 CRC-4 checksum errors
  - — ITU-CEPT automatic received E-bit processing; optional detection of permanently received E bit = 0 events in a five-second interval
  - — Selectable automatic transmission for E bit to the line
- Line codes
  - — DS1: alternate mark inversion (AMI); binary eight zero code suppression (B8ZS); per-channel zero code suppression (ZCS)
  - — DS1 independent transmit and receive path line code formats when using AMI/ZCS and B8ZS coding
  - — ITU-CEPT: AMI; high-density bipolar 3 (HDB3) encoding and decoding double bipolar violation monitoring with optional monitoring of 4-bit interval without positive or negative pulses error indication
- Signaling
  - — DS1: extended superframe 2-state, 4-state, and 16-state per-channel robbed bit
  - — DS1: D4 superframe 2-state and 4-state per-channel robbed bit
  - — DS1: *SLC*-96 superframe 2-state, 4-state, and 9-state per-channel robbed bit
  - — DS1: channel 24 message-oriented signaling
  - — ITU-CEPT: common channel signaling (CCS)
  - — ITU-CEPT: channel associated signaling (CAS)
  - — ITU-CEPT: international remote switching module (IRMS)
  - — Transparent (all data channels)
- Programmable elastic store buffer depth
  - — Two-frame (64-byte) default
  - — 6-byte option
- Digital phase comparator with selectable reference signal using either the system clock or the receive line clock
- Alarm reporting and performance monitoring
  - — ANSI and AT&T standard error checking
  - — Programmable ANSI yellow alarm processing
  - — ITU standard error checking
  - — Selectable interrupts enables
  - — Error counters: Bipolar violations
    Errored frame alignment signals
    Errored CRC checksum block
  - — Errored seconds, severely errored seconds, and unavailable seconds processing
  - — Programmable automatic and on-demand alarm signal generation
  - — Multiple loopback modes
  - — Selectable test patterns for line transmission
  - — Programmable squelch and idle codes
- System interface
  - — One frame synchronization input signal
  - — One system interface clock
  - — Programmable clock edge for latching frame synchronization signal
  - — 2.048 Mbits/s, 2.048 MHz concentration highway interface (CHI) default mode
  - — Optional 2.048 Mbits/s, 4.096 MHz 32 time slots mode
  - — Optional 4.096 Mbits/s, 4.096 MHz 32 time slots mode
  - — Optional 4.096 Mbits/s, 8.196 MHz 32 time slots mode
  - — Programmable bit and byte offset
  - — Programmable clock edge for receive and transmit data
  - — Programmable CHI master mode for the generation of the CHI FS from internal logic with timing derived from the receive line clock signal
- Selectable microprocessor interface
  - — 16 MHz read and write access with no wait-states
  - — Programmable *Intel** and *Motorola*† interface modes
  - — Demultiplexed address and data bus
  - — Directly addressable internal registers
- Hardware reset
- Software reset
- 3-statable outputs

* *Intel* is a registered trademark of Intel Corporation.
† *Motorola* is a registered trademark of Motorola, Inc.

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Functional Description

The Lucent Technologies T7230A Primary Access Controller/Framer (PAC) provides a complete T1 or E1 digital framing solution within one package. The T7230A can interface to devices using the Lucent Technologies Microelectronics Group system CHI; for example, the T7270 time-slot interchanger or T7115A synchronous protocol data formatter and DS1/T1 or ITU-CEPT line interface devices, such as the T7290A DSI/E1 line interface unit.

The line interface is a dual-rail interface that supports AMI, T1 B8ZS, per-channel T1 ZSC, and ITU-CEPT HDB3 line code formats. Optionally, the T7230A can transmit and receive single-rail line data.

Framing formats supported include T1D4, T1DM, and *SLC*-96 superframing and extended superframing; ITU-CEPT basic framing; and ITU-CEPT time slot 0 and time slot 16 multiframing.

Alarm monitoring by the receive framer includes detection of loss of receive clock, red, yellow, and blue (AIS) alarms. These alarms are detected as defined by ANSI, AT&T, and ITU standards. The transmit framer detects loss of transmit clock.

Performance monitoring as specified by AT&T, ANSI, and ITU is provided through counters monitoring frame bit errors, bipolar violation, CRC errors, errored events, errored seconds, bursty errored seconds, severely errored seconds, and unavailable or failed seconds.

In-band loopback activation and deactivation codes can be transmitted to the line. In-band loopback activation and deactivation codes are detected.

Remote, payload, and line loopback modes are programmable.

The signaling formats supported are T1 per-channel robbed-bit signaling (RBS), channel-24 message-oriented signaling (MOS), ITU-CEPT channel-associated signaling (CAS), ITU-CEPT common channel signaling (CCS), and international remote switching module (IRMS). In the T1 RBS mode, voice and data channels are programmable. The entire payload can be forced into a no signaling, i.e., data only by programming one control bit.

Channelized data and its corresponding signaling information can be accessed through the system interface (concentration highway interface).

Extraction and insertion of the facility data link in ESF, T1DM, *SLC*-96, or ITU-CEPT modes is provided through a four-port serial interface.

A two-frame elastic store buffer for jitter attenuation performs controlled slips and provides indication of slip direction. This buffer can be programmed to operate as a function of the receive line clock and can be reduced to 11 bytes in length.

The system interface is a 2.048 Mbits/s data 2.048 MHz clock concentration highway interface (CHI) serial bus. This interface can be reconfigured into several modes: a 2.048 Mbits/s data/4.096 MHz clock; a 4.096 Mbits/s data/4.096 MHz clock; or a 4.096 Mbits/s data/8.192 MHz clock.

Accessing internal registers is done through a demultiplexed address and data bus microprocessor interface using either the *Intel* 80188 (or 80X88) interface protocol with independent read and write signals or the *Motorola* MC680X0 interface protocol with address and data strobe signals.

Functional Description (continued)

The T7230A is manufactured using low-power CMOS technology and is packaged in an 68-pin plastic-leaded-chip-carrier (PLCC) or an 80-pin thin quad flat package (TQFP).

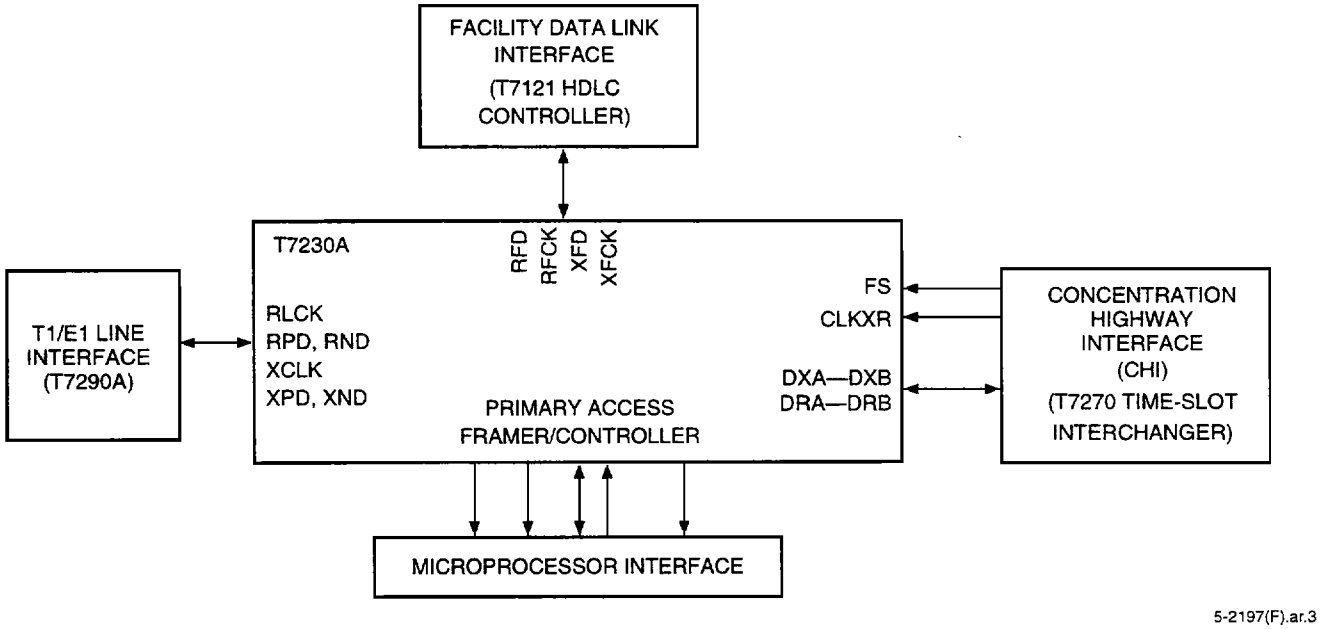

Figure 1. Basic T7230A System Interface Configuration

Functional Description (continued)

The block diagram of the T7230A is shown in Figure 2.

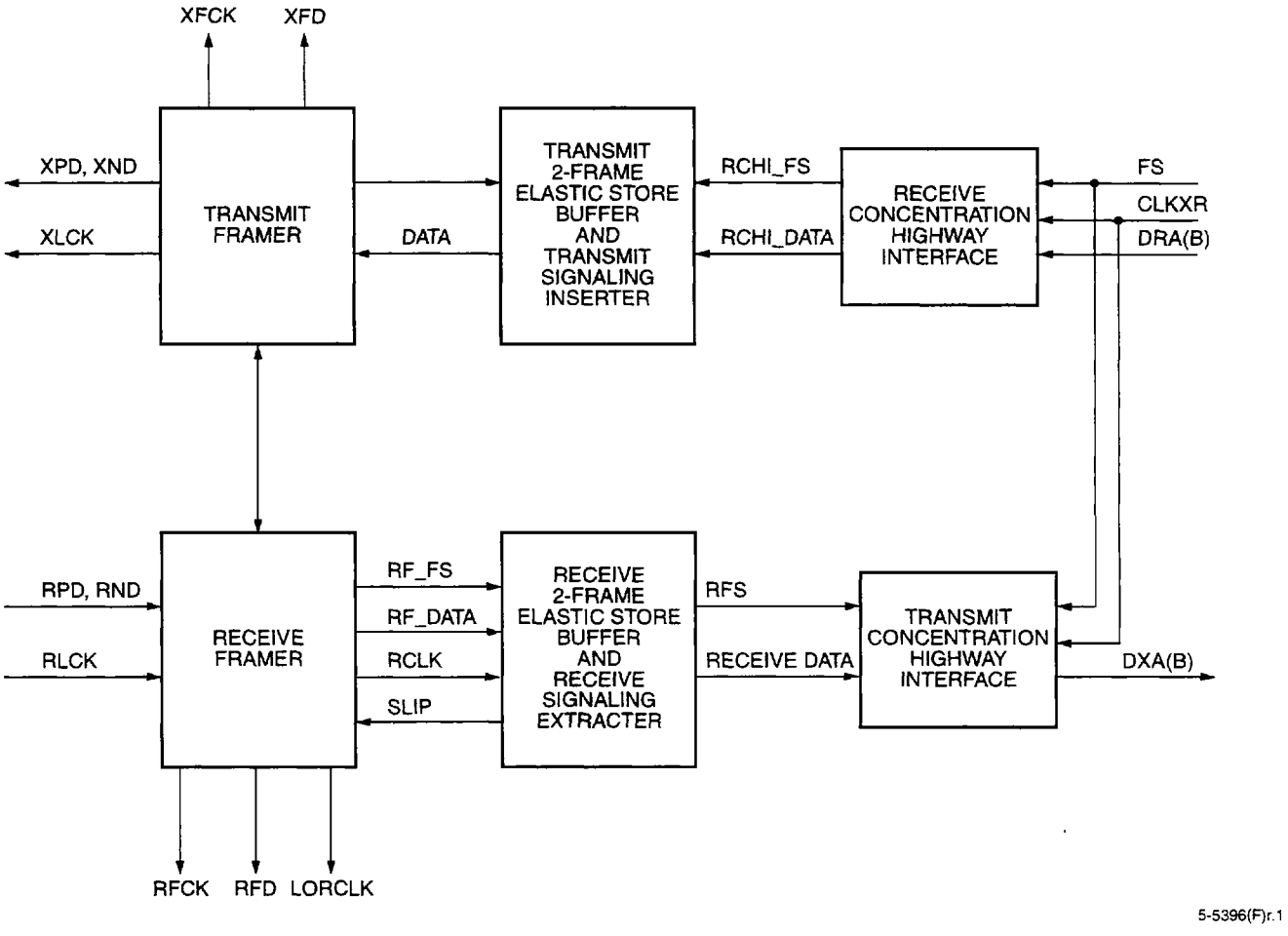

Figure 2. Functional Block Diagram of the T1/E1 Primary Access Framer/Controller (PAC)

Pin Information

The 68-pin plastic leaded chip carrier (PLCC) package option type pin assignment for the T7230A is illustrated in Figure 3.

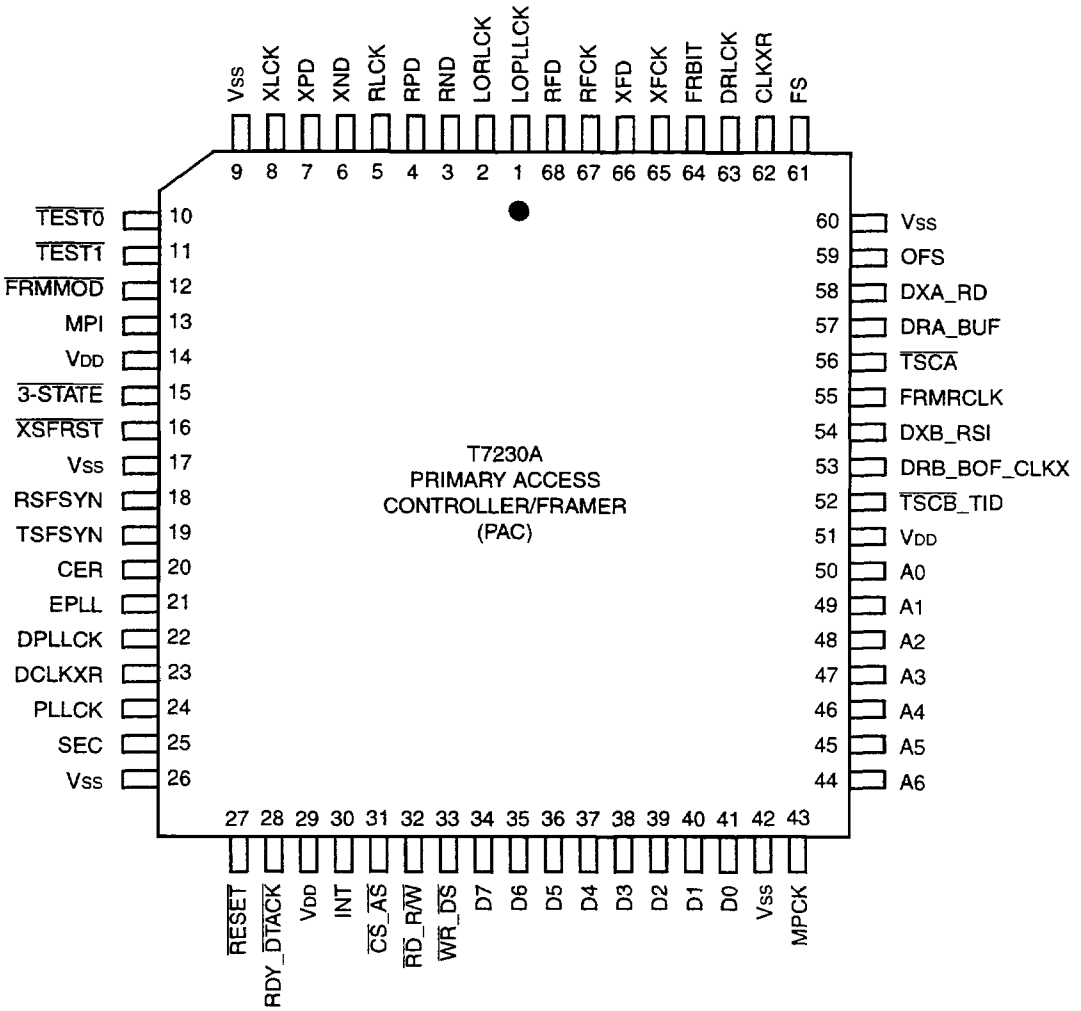

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Figure 3. The T7230A's 68-Pin Plastic Leaded Chip Carrier (PLCC) Package Option Pin Assignments

Pin Information (continued)

Available in an 80-pin thin quad flat package (TQFP) package option type, T7230A's pin assignment is illustrated in Figure 4.

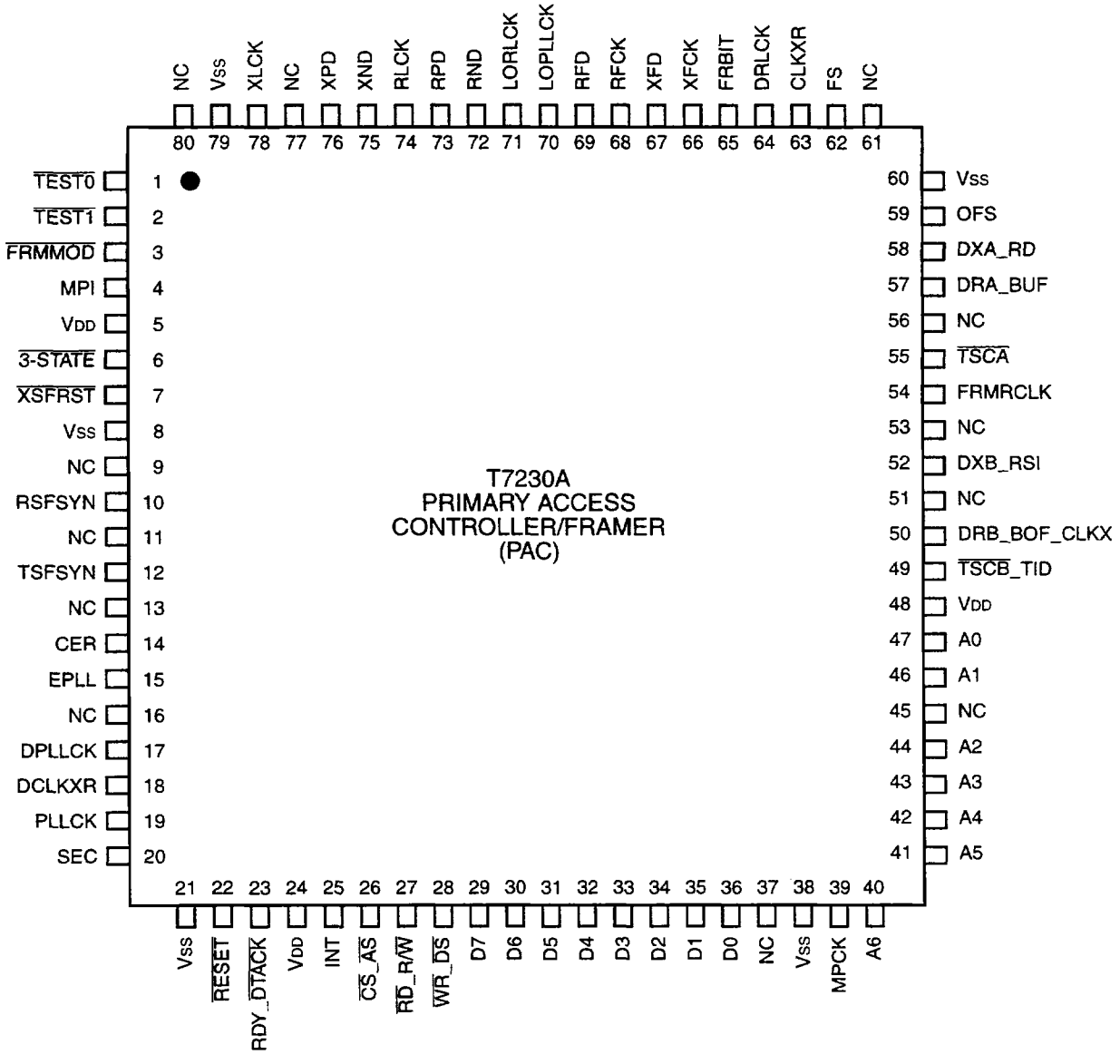

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Figure 4. The T7230A's 80-Pin Thin Quad Flat Package (TQFP) Package Option Pin Assignments

Table 1 shows the list of T7230A pins and a functional description for each.

Pin Information (continued)

Table 1. Pin Descriptions for the 68-Pin Package

Pin	Symbol	Type[1]	Name and Function
1	LOPLLCK	O	**Loss of Transmit Clock.** The T7230A drives this pin high when it detects PLLCK stuck in a 0 state or a 1 state for an interval greater than 250 µs.
2	LORLCK	O	**Loss of Receive Clock.** The T7230A drives this pin high when it detects RLCK stuck in a 0 state or a 1 state for an interval greater than 250 µs.
3	RND	I	**Receive Negative-Rail Data.** Dual-rail, non-return-to-zero serial data latched by the rising edge of RLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s. In single-rail mode, if RND = 1 at the rising edge of RLCK, the BPV counter increments by one.
4	RPD	I	**Receive Positive-Rail Data.** Dual-rail, non-return-to-zero serial data latched by the rising edge of RLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s. In single-rail mode, RPD is receive data.
5	RLCK	I	**Receive Line Interface Clock.** 1.544 MHz DS1 or 2.048 MHz input signal used by the receive framer.
6	XND	O	**Transmit Negative-Rail Data.** Dual-rail, non-return-to-zero serial data latched out by the rising edge of XLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s.
7	XPD	O	**Transmit Positive-Rail Data.** Dual-rail, non-return-to-zero serial data latched out by the rising edge of XLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s.
8	XLCK	O	**Transmit Line Interface Clock.** 1.544 MHz DS1 or 2.048 MHz input signal used by the transmit framer.
9	VSS	—	**Ground.**
10	$\overline{\text{TEST0}}$	I^u	**Test 0 (Active-Low). Manufacture Testing Only.**
11	$\overline{\text{TEST1}}$	I^u	**Test 1 (Active-Low). Manufacture Testing Only.**
12	$\overline{\text{FRMMOD}}$	I^u	**Framer Mode.** Strap this pin to Vss (GROUND) to enable the framer mode.
13	MPI	I^u	**Microprocessor Interface.** Strap to VDD to enable the *Intel* 80X86/88 protocol. Strap to Vss to enable the *Motorola* 680X0 protocol.
14	VDD	—	**5 V Supply.**
15	$\overline{\text{3-STATE}}$	I^u	**3-State (Active-Low).** Asserting this pin low forces all outputs into a high-impedance state.
16	$\overline{\text{XSFRST}}$	I^u	**Transmit Signaling Superframe Reset (Active-Low).** Assert this pin low to reset the DS1 signaling superframe counter and force a new signaling superframe structure.
17	VSS	—	**Ground.**
18	RSFSYN	O	**Receive Signaling Superframe Sync.** A 3 ms interval in DS1. A 2 ms interval in ITU-CEPT. Sourced from the CHI, this is an 8-bit wide pulse; sourced from the framer, this is a 1-bit wide pulse.
19	TSFSYN	O	**Transmit Signaling Superframe Sync.** A 3 ms interval in DS1. A 2 ms interval in ITU-CEPT. Sourced from the CHI, this is an 8-bit wide pulse; sourced from the framer, this is a 1-bit wide pulse.

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions for the 68-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
20	CER	O	**Receive CRC Error.** Indication of a receive checksum error. In ESF, this pin is asserted at the onset of the CRC-6 error and remains asserted for the duration of the extended superframe. In CEPT, this pin is asserted once for the errored checksum block for a 1-byte interval.
21	EPLL	O	**Error Phase-Lock Loop Signal.** The error signal proportional to the phase difference between DCLKXR and DPLLCK as detected from the internal PLL circuitry.
22	DPLLCK	O	**Divided-Down Phase-Lock Loop Clock.** 32 kHz or 8 kHz clock signal derived from the PLLCK input signal.
23	DCLKXR	O	**Divided-Down CHI Clock.** 32 kHz or 8 kHz clock signal derived from the CLKXR input signal.
24	PLLCK	I	**Phase-Lock Loop Clock.** This clock signal is used to clock the transmit framer. This signal should be phase-locked to the CLKXR clock signal. DS1—1.544 MHz for low-frequency PLL mode. DS1—6.167 MHz for high-frequency PLL mode. CEPT—2.048 MHz for low-frequency PLL mode. CEPT—8.192 MHz for high-frequency PLL mode.
25	SEC	O	**Second Pulse.** A one-second timer with an active-high pulse. The duration of the pulse is one RLCK cycle. Used for performance monitoring.
26	VSS	—	**Ground.**
27	$\overline{\text{RESET}}$	I^u	**Reset (Active-Low).** Asserting this pin low for at least 2.5 ms will reset the entire device; this includes all internal counters and control registers.
28	RDY_$\overline{\text{DTACK}}$	O	**Ready_Data Transfer Acknowledge.** In the *Intel* interface mode, this pin is asserted high to indicate the completion of a read or write access; this pin is forced into a high-impedance state while $\overline{\text{CS}}$ is high. In the *Motorola* interface mode, this pin is asserted low to indicate the completion of a read or write access; this pin is forced to a 1 state otherwise.
29	VDD	—	**5 V Supply.**
30	INT	O	**Interrupt.** INT is asserted high, indicating an internal interrupt condition/event has been generated. Otherwise, INT is in the 0 state. Interrupt events/conditions are maskable through the control registers.
31	$\overline{\text{CS}}$_$\overline{\text{AS}}$	—	**Chip Select_Address Strobe (Active-Low).** In the *Intel* interface mode, this pin must be asserted low to initiate a read or write access and kept low for the duration of the access; asserting $\overline{\text{CS}}$ low forces RDY from its high-impedance state into a 0 state. In the *Motorola* interface mode, this pin must be asserted low to initiate a read or write access and kept low for the duration of the access.

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions for the 68-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
32	$\overline{RD}$_R/$\overline{W}$	I	**Read_Read/Write.** While $\overline{RD}$ is low in the *Intel* interface mode, the T7230A drives the data bus with the contents of the addressed register. In the *Motorola* interface mode, this signal is asserted high for read accesses or asserted low for write accesses.
33	$\overline{WR}$_$\overline{DS}$	I	**Write_Data Strobe (Active-Low).** In the *Intel* mode, the value present on the data bus is latched into the addressed register on the positive edge of the signal applied to $\overline{WR}$. In the *Motorola* mode, when $\overline{AS}$ = 0 and R/$\overline{W}$ = 0 (write), the value present on the data bus is latched into internal flip-flops on the positive edge of the signal applied to $\overline{DS}$; when $\overline{AS}$ = 0 and R/$\overline{W}$ = 1 (read), the T7230A drives the data bus with the contents of the addressed register while $\overline{DS}$ = 0.
34—41	D7—D0	I/O	**Microprocessor Data Bus.** Bidirectional data bus used for read and write accesses. While the T7230A is not driving the data bus, the T7230A will force these pin into an high-impedance state.
42	VSS	—	**Ground.**
43	MPCK	I	**Microprocessor Clock.** 16 MHz microprocessor clock. Used only for timing the internal RDY signal.
44—50	A6—A0	I	**Microprocessor Address Bus.** Address bus used to access internal registers.
51	VDD	—	**5 V Supply.**
52	$\overline{TSCB}$_TID	I/O	**CHI Time-Slot Control for Port B.** The T7230A drives this pin low to enable external bus drivers for active CHI time slots. **TID.** In the framer mode ($\overline{FRMMOD}$ = 0), this is the input data signal for the transmit framer.
53	DRB_BOF_CLKX	I	**Receive CHI Data Port B.** Serial input system data at 2.048 Mbits/s or 4.096 Mbits/s. **Buffer Overflow.** In framer mode ($\overline{FRMMOD}$ = 0), this may be used in performance monitoring to indicate an overflow event from an external elastic store.
54	DXB_RSI	O	**Transmit CHI Data Port B.** Serial output system data at 2.048 Mbits/s or 4.096 Mbits/s. This port is forced into a high-impedance state for all inactive time slots. **Receive Signaling Inhibit.** In framer mode ($\overline{FRMMOD}$ = 0), this pin is forced to a 1-state for the duration of a loss of frame, loss of superframe (DS1), or loss of time slot 16 multiframe (CEPT) alignment state.
55	FRMRCLK	O	**Framer Receive Line Clock.** Framer receive line clock used in the receive framer section, derived from RLCK (same phase).
56	$\overline{TSCA}$	O	**CHI Time-Slot Control for Port A (Active-Low).** The T7230A drives this pin low to enable external bus drivers for active CHI time slots.

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions for the 68-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
57	DRA_BUF	I	**Receive CHI Data Port A.** Serial input system data at 2.048 Mbits/s or 4.096 Mbits/s. **Buffer Underflow.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this may be used in performance monitoring to indicate an underflow event from an external elastic store.
58	DXA_RD	O	**Transmit CHI Data Port A.** Serial output system data at 2.048 Mbits/s or 4.096 Mbits/s. This port is forced into a high-impedance state for all inactive time slots. **Receive Data.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this is the serial unirail output data from the receive framer at 1.544 Mbits/s (DS1) or 2.048 Mbits/s (CEPT) rates.
59	OFS	O	**Output CHI Frame Sync.** In the CHI master mode, the T7230A's receive CHI circuit generates an 8 kHz frame sync on this pin for use on the CHI.
60	Vss	—	**Ground.**
61	FS	I	**CHI Frame Sync.** 8 kHz frame sync from a CHI master.
62	CLKXR	I	**CHI Transmit/Receive Clock.** 2.048/4.096/8.192 MHz CHI clock signal. The PLLCK signal should be phase-locked to CLKXR.
63	DRLCK	O	**Divided-Down Receive Line Clock.** 8 kHz clock signal derived from the RLCK input signal.
64	FRBIT	O	**Receive Framing Bit.** In DS1 framing formats, this pin outputs the value of the framing bit associated with the current CHI frame. The value is valid for the duration of the CHI frame. In CEPT mode, this pin is forced to a 1 state.
65	XFCK	O	**Transmit Facility Data Link Clock.** In DS1-DDS with data link access, this is an 8 kHz clock signal. Otherwise, this is a 4 kHz clock signal.
66	XFD	I	**Transmit Facility Data Link.** Serial input facility data link bit stream for insertion into the transmit line data stream by the transmit framer. In DS1-DDS with data link access, this is an 8 kbits/s signal. Otherwise, this is a 4 kbits/s signal.
67	RFCK	O	**Receive Facility Data Link Clock.** In DS1-DDS with data link access, this is an 8 kHz clock signal. Otherwise, this is a 4 kHz clock signal.
68	RFD	O	**Receive Facility Data Link.** Serial output facility data link bit stream extracted from the receive line data stream by the receive framer. In DS1-DDS with data link access, this is an 8 kbits/s signal. Otherwise, this is a 4 kbits/s signal. During a loss of frame alignment, the receive framer will force this pin to a 1 state.

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 2. Pin Descriptions for the 80-Pin Package

Pin	Symbol	Type[1]	Name and Function
1	$\overline{\text{TEST0}}$	I^u	**TEST 0 (Active-Low). Manufacture Testing Only.**
2	$\overline{\text{TEST1}}$	I^u	**TEST 1 (Active-Low). Manufacture Testing Only.**
3	$\overline{\text{FRMMOD}}$	I^u	**Framer Mode.** Strap this pin to Vss (GROUND) to enable the framer mode.
4	MPI	I^u	**Microprocessor Interface.** Strap to VDD to enable the *Intel* 80X86/88 protocol. Strap to Vss to enable the *Motorola* 680X0 protocol.
5	VDD	—	**5 V Supply.**
6	$\overline{\text{3-STATE}}$	I^u	**3-State (Active-Low).** Asserting this pin low forces all outputs into a high-impedance state.
7	$\overline{\text{XSFRST}}$	I^u	**Transmit Signaling Superframe Reset (Active-Low).** Assert this pin low to reset the DS1 signaling superframe counter and force a new signaling superframe structure.
8	Vss	—	**Ground.**
9	NC	—	**No Connect.**
10	RSFSYN	O	**Receive Signaling Superframe Sync.** A 3 ms interval in DS1. A 2 ms interval in ITU-CEPT. Sourced from the CHI, this is an 8-bit wide pulse; sourced from the framer, this is a 1-bit wide pulse.
12	TSFSYN	O	**Transmit Signaling Superframe Sync.** A 3 ms interval in DS1. A 2 ms interval in ITU-CEPT. Sourced from the CHI, this is an 8-bit wide pulse; sourced from the framer, this is a 1-bit wide pulse.
13	NC	—	**No Connect.**
14	CER	O	**Receive CRC Error.** Indication of a receive checksum error. In ESF, this pin is asserted at the onset of the CRC-6 error and remains asserted for the duration of the extended superframe. In CEPT, this pin is asserted once for the errored checksum block for a 1-byte interval.
15	EPLL	O	**Error Phase-Lock Loop Signal.** The error signal proportional to the phase difference between DCLKXR and DPLLCK as detected from the internal PLL circuitry.
16	NC	—	**No Connect.**
17	DPLLCK	O	**Divided-Down Phase-Lock Loop Clock.** 32 kHz or 8 kHz clock signal derived from the PLLCK input signal.
18	DCLKXR	O	**Divided-Down CHI Clock.** 32 kHz or 8 kHz clock signal derived from the CLKXR input signal.
19	PLLCK	I	**Phase-Lock Loop Clock.** This clock signal is used to clock the transmit framer. This signal should be phase-locked to the CLKXR clock signal. DS1—1.544 MHz for low-frequency PLL mode. DS1—6.167 MHz for high-frequency PLL mode. CEPT—2.048 MHz for low-frequency PLL mode. CEPT—8.192 MHz for high-frequency PLL mode.
20	SEC	O	**Second Pulse.** A one-second timer with an active-high pulse. The duration of the pulse is one RLCK cycle. Used for performance monitoring.

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 2. Pin Descriptions for the 80-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
21	VSS	—	**Ground.**
22	$\overline{\text{RESET}}$	I^u	**Reset (Active-Low).** Asserting this pin low for at least 2.5 ms will reset the entire device, this includes all internal counters and control registers.
23	RDY_$\overline{\text{DTACK}}$	O	**Ready_Data Transfer Acknowledge.** In the *Intel* interface mode, this pin is asserted high to indicate the completion of a read or write access; this pin is forced into a high-impedance state while $\overline{\text{CS}}$ is high. In the *Motorola* interface mode, this pin is asserted low to indicate the completion of a read or write access; this pin is forced to a 1 state otherwise.
24	VDD	—	**5 V Supply.**
25	INT	O	**Interrupt.** INT is asserted high indicating an internal interrupt condition/ event has been generated. Otherwise, INT is in the 0 state. Interrupt events/ conditions are maskable through the control registers.
26	$\overline{\text{CS}}$_$\overline{\text{AS}}$	—	**Chip Select_Address Strobe (Active-Low).** In the *Intel* interface mode, this pin must be asserted low to initiate a read or write access and kept low for the duration of the access; asserting $\overline{\text{CS}}$ low forces RDY from its high-impedance state into a 0 state. In the *Motorola* interface mode, this pin must be asserted low to initiate a read or write access and kept low for the duration of the access.
27	$\overline{\text{RD}}$_R/$\overline{\text{W}}$	I	**Read_Read/Write.** While $\overline{\text{RD}}$ is low in the *Intel* interface mode, the T7230A drives the data bus with the contents of the addressed register. In the *Motorola* interface mode, this signal is asserted high for read accesses or asserted low for write accesses.
28	$\overline{\text{WR}}$_$\overline{\text{DS}}$	I	**Write_Data Strobe (Active-Low).** In the *Intel* mode, the value present on the data bus is latched into the addressed register on the positive edge of the signal applied to $\overline{\text{WR}}$. In the *Motorola* mode, when $\overline{\text{AS}}$ = 0 and R/$\overline{\text{W}}$ = 0 (write), the value present on the data bus is latched into internal flip-flops on the positive edge of the signal applied to $\overline{\text{DS}}$; when $\overline{\text{AS}}$ = 0 and R/$\overline{\text{W}}$ = 1 (read), the T7230A drives the data bus with the contents of the addressed register while $\overline{\text{DS}}$ = 0.
29—36	D7—D0	I/O	**Microprocessor Data Bus.** Bidirectional data bus used for read and write accesses. While the T7230A is not driving the data bus, the T7230A will force these pin into a high-impedance state.
37	NC	—	**No Connect.**
38	VSS	—	**Ground.**
39	MPCK	I	**Microprocessor Clock.** 16 MHz microprocessor clock. Used only for timing the internal RDY signal.
40—44 46—47	A6—A0	I	**Microprocessor Address Bus.** Address bus used to access internal registers.
45	NC	—	**No Connect.**
48	VDD	—	**5 V Supply.**

1. I^u indicates an internal pull-up.

Pin Information (continued)

Table 2. Pin Descriptions for the 80-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
49	$\overline{\text{TSCB}}$_TID	I/O	**CHI Time-Slot Control for Port B.** The T7230A drives this pin low to enable external bus drivers for active CHI time slots. **TID.** In the framer mode ($\overline{\text{FRMMOD}}$ = 0), this is the input data signal for the transmit framer.
50	DRB_BOF_CLKX	I	**Receive CHI Data Port B.** Serial input system data at 2.048 Mbits/s or 4.096 Mbits/s. **Buffer Overflow.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this may be used in performance monitoring to indicate an overflow event from an external elastic store.
51	NC	—	**No Connect.**
52	DXB_RSI	O	**Transmit CHI Data Port B.** Serial output system data at 2.048 Mbits/s or 4.096 Mbits/s. This port is forced into a high-impedance state for all inactive time slots. **Receive Signaling Inhibit.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this pin is forced to a 1 state for the duration of a loss of frame, loss of superframe (DS1), or loss of time slot 16 multiframe (CEPT) alignment state.
54	FRMRCLK	O	**Framer Receive Line Clock.** Framer receive line clock used in the receive framer section, derived from RLCK (same phase).
55	$\overline{\text{TSCA}}$	O	**CHI Time-Slot Control for Port A (Active-Low).** The T7230A drives this pin low to enable external bus drivers for active CHI time slots.
56	NC	—	**No Connect.**
57	DRA_BUF	I	**Receive CHI Data Port A.** Serial input system data at 2.048 Mbits/s or 4.096 Mbits/s. **Buffer Underflow.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this may be used in performance monitoring to indicate an underflow event from an external elastic store.
58	DXA_RD	O	**Transmit CHI Data Port A.** Serial output system data at 2.048 Mbits/s or 4.096 Mbits/s. This port is forced into a high-impedance state for all inactive time slots. **Receive Data.** In framer mode ($\overline{\text{FRMMOD}}$ = 0), this is the serial unirail output data from the receive framer at 1.544 Mbits/s (DS1) or 2.048 Mbits/s (CEPT) rates.
59	OFS	O	**Output CHI Frame Sync.** In the CHI master mode, the T7230A's receive CHI circuit generates an 8 kHz frame sync on this pin for use on the CHI.
60	V_{SS}	—	**Ground.**
61	NC	—	**No Connect.**
62	FS	I	**CHI Frame Sync.** 8 kHz frame sync from a CHI master.
63	CLKXR	I	**CHI Transmit/Receive Clock.** 2.048/4.096/8.192 MHz CHI clock signal. The PLLCK signal should be phase-locked to CLKXR.
64	DRLCK	O	**Divided-Down Receive Line Clock.** 8 kHz clock signal derived from the RLCK input signal.

1. I^u indicates an internal pull-up.

Pin Information (continued)

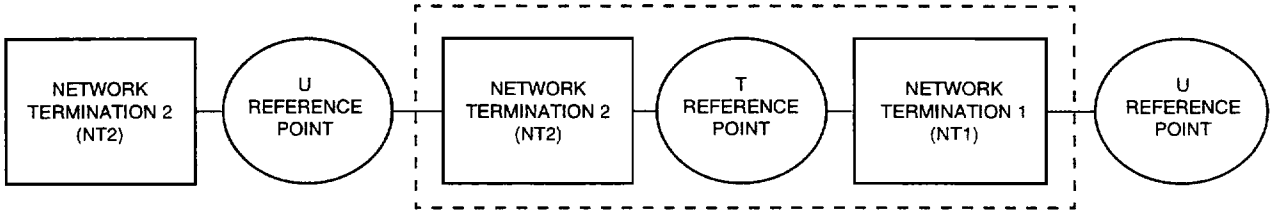
Table 2. Pin Descriptions for the 80-Pin Package (continued)

Pin	Symbol	Type[1]	Name and Function
65	FRBIT	O	**Receive Framing Bit.** In DS1 framing formats, this pin outputs the value of the framing bit associated with the current CHI frame. The value is valid for the duration of the CHI frame. In CEPT mode, this pin is forced to a 1 state.
66	XFCK	O	**Transmit Facility Data Link Clock.** In DS1-DDS with data link access, this is an 8 kHz clock signal. Otherwise, this is a 4 kHz clock signal.
67	XFD	I	**Transmit Facility Data Link.** Serial input facility data link bit stream for insertion into the transmit line data stream by the transmit framer. In DS1-DDS with data link access, this is an 8 kbits/s signal. Otherwise, this is a 4 kbits/s signal.
68	RFCK	O	**Receive Facility Data Link Clock.** In DS1-DDS with data link access, this is an 8 kHz clock signal. Otherwise, this is a 4 kHz clock signal.
69	RFD	O	**Receive Facility Data Link.** Serial output facility data link bit stream extracted from the receive line data stream by the receive framer. In DS1-DDS with data link access, this is an 8 kbits/s signal. Otherwise, this is a 4 kbits/s signal. During a loss of frame alignment, the receive framer will force this pin to a 1 state.
70	LOPLLCK	O	**Loss of Transmit Clock.** The T7230A drives this pin high when it detects PLLCK stuck in a 0 state or a 1 state for an interval greater than 250 µs.
71	LORLCK	O	**Loss of Receive Clock.** The T7230A drives this pin high when it detects RLCK stuck in a 0 state or a 1 state for an interval greater than 250 µs.
72	RND	I	**Receive Negative-Rail Data.** Dual-rail, non-return-to-zero serial data latched by the rising edge of RLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s. In single-rail mode, if RND = 1 at the rising edge of RLCK, the BPV counter increments by one.
73	RPD	I	**Receive Positive-Rail Data.** Dual-rail, non-return-to-zero serial data latched by the rising edge of RLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s. In single-rail mode, RPD is receive data.
74	RLCK	I	**Receive Line Interface Clock.** 1.544 MHz DS1 or 2.048 MHz input signal used by the receive framer.
75	XND	O	**Transmit Negative-Rail Data.** Dual-rail, non-return-to-zero serial data latched out by the rising edge of XLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s.
76	XPD	O	**Transmit Positive-Rail Data.** Dual-rail, non-return-to-zero serial data latched out by the rising edge of XLCK. Data rates: DS1—1.544 Mbits/s; CEPT—2.048 Mbits/s.
77	NC	—	**No Connect.**
78	XLCK	O	**Transmit Line Interface Clock.** 1.544 MHz DS1 or 2.048 MHz input signal used by the transmit framer.
79	Vss	—	**Ground.**
80	NC	—	**No Connect.**

1. I[u] indicates an internal pull-up.

ISDN Primary Rate Interface

The integrated services digital network (ISDN) primary rate interface (PRI) specification is defined in two ways. One is based on the North American T1 network and is defined in the AT&T Technical Reference 41449 [7]. The other is based on the European CEPT digital trunk facility and is defined in ITU Recommendation I.431 [8]. Both specifications deal with the physical layer (layer 1) characteristics of the network interface at the S and T reference points for the 1.544 Mbits/s and 2.048 Mbits/s ISDN accesses. The ITU Recommendation I.431 is derived from ITU Recommendations G.703 [9], G.704 [10], and G.733[10] that contain the electrical characteristics and the frame structures already used by the PCM equipment, digital multiplexers, and digital switch exchange.



5-4555(F)r.1

Notes:
TE1 is a fully integrated terminal capable of handling ISDN protocols.

S reference point is a subscriber-side demarcation point for primary access at 1.544 Mbits/s or 2.048 Mbits/s.

NT1 and NT2 provide the network termination functions that connect the subscriber to the network. NT1 provides network access, and NT2 provides subscriber-side termination.

The T reference point is an internal point in the switching system that separates the NT1 and NT2 functions. If the NT1 and NT2 functions are located within the switch, there is only one network termination (NT) and no physical interface T.

U reference point defines the interface at the network side.

Figure 5. ISDN Primary Rate Interface Reference Points

For both 1.544 Mbits/s and 2.048 Mbits/s primary rate transport, only the point-to-point configuration is required between the NT and TE. The maximum point-to-point distance depends on the type of interconnecting wire pair. ITU Recommendation G.703 [9] contains the electrical characteristics of transmitted and received pulses.

The following types of channels, as defined in ITU Recommendation I.412 [11], can be transported across the digital interface using time-multiplexing techniques:

- B channels (64 kbits/s)
- H0 channels (384 kbits/s)
- H11 channels (1.536 Mbits/s)
- H12 channels (1.920 Mbits/s)
- D or E channels (64 kbits/s)

In addition, other functions such as bit timing, byte (octet) timing, frame alignment, and maintenance are provided across the interface.

In the ISDN structure, traffic channels are combined with appropriate framing and housekeeping information into one composite digital signal for each direction of transmission. Interfaces for the ISDN primary rate access are active at all times; hence, no special activation or deactivation procedures are required.

The electrical specifications of the 1.544 Mbits/s interface are the same as those described in ITU Recommendation G.703 [9] and the AT&T Technical Reference 62411 [5]. In particular, the binary eight zero code suppression line code is recommended for 1.544 ISDN applications. The frame structure is the same as extended superframe (ESF). A frame contains 24 eight-bit time slots. Users' traffic (voice or data channels) is transported in the 8-bit time slots. Time slot 24 is assigned to the D channel or E channel when either of these channels are present.

ISDN Primary Rate Interface (continued)

The time slots assigned to the other channels (B, H0, or H11) are numbered 1 to 23 or 1 to 24, depending on the presence of a D or E channel. The timing procedures, based on providing satisfactory customer service, imply that the NT derives its timing from the network clock and the TE synchronizes its timing to a signal received from the NT.

The electrical charcteristics of the 2.048 Mbits/s interface are also described in the ITU Recommendation G.703. Framing characteristics are described in the ITU Recommendation G.704. The frame structure consists of 32 time slots, numbered 0 to 31. Time slot 0 contains the frame alignment signal. Time slot 16 contains the D or E channel when either is present. The remaining time slots (1—15 and 17—31) are available for the other channels (B, H0, or H12). Timing procedures are the same as those for the 1.544 Mbits/s interface.

Line Interface

Physical Interface

The transmit line interface for the T7230A consists of the XPD, XND, XFD, XFCK, and XLCK pins. The receive line interface consists of the RPD, RND, RFD, RFCK and RLCK pins. When programmed for single-rail mode, the transmit framer drives XPD with valid data while XND is forced to ZERO. The receive framer accepts data on RPD as valid non-return-to-zero single-rail data; RND = 1 on the rising edge of RLCK will cause the BPV counter to increment by one. Figure 6 shows the timing for the transmit and receive line interfaces.

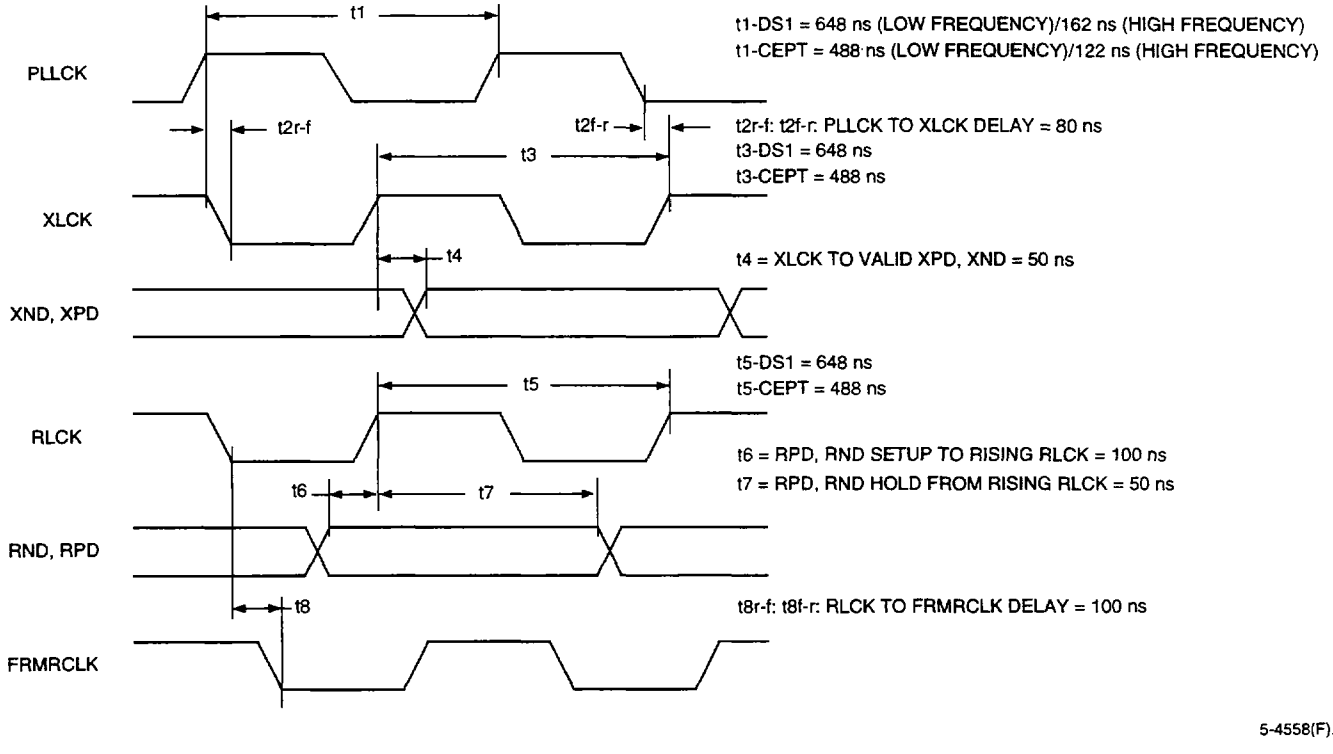


Figure 6. Transmit Framer XLCK to XND, XPD and Receive Framer RND, RPD to RLCK Timing

Line Interface (continued)

Physical Interface (continued)

Figure 7 shows the facility data link timing for XFD-XFCK and RFD-RFCK signals.

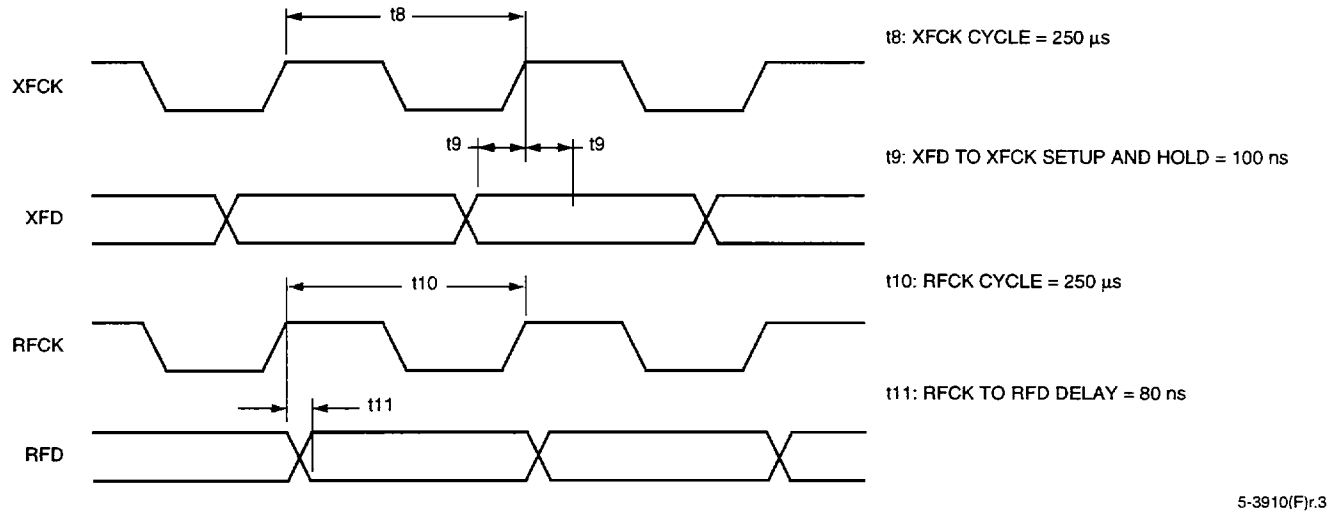


Figure 7. T7230A Facility Data Link Timing

Line Encoding

Single Rail

The XPD output transmits the data in binary form while the XND output is forced to a 0 state. The RPD input receives binary data while pulses on the RND input are counted as bipolar violations in the BPV register. This scheme is shown in Table 3.

Table 3. Single-Rail Encoding

Bit Stream	1011	0000	0111	1010
Single-Rail Data (RPD)	1011	0000	0111	1010

Alternate Mark Inversion (AMI)

The default line code used for T1 is alternate mark inversion (AMI). The coding scheme represents a 1 with a pulse or mark on the positive or negative rail and a 0 with no pulse on either rail. This scheme is shown in Table 4.

Table 4. AMI Encoding

Input Bit Stream	1011	0000	0111	1010
AMI Data	+0+–	0000	0+–+	–0+0

The T1 "ones density rule" states that:

- In every 24 bits of information to be transmitted, there must be at least three pulses, and no more than 15 zeros may be transmitted consecutively.

AT&T Technical Reference 62411 for digital transmissions requires that:

- In every 8 bits of information, at least one pulse must be present.

Line Interface (continued)

DS1 Zero Code Suppression (ZCS)

Zero code suppression is a technique known as pulse stuffing in which the least significant bit (LSB) of each time slot is forced to a logic 1 state (or stuffed with a one). The scheme, shown in Table 5, limits the data rate of each time slot from 64 kbits/s to 56 kbits/s.

The T7230A default ZCS format stuffs the seventh bit of those time slots programmed for robbed-bit signaling (as defined in the signaling control registers with the F and G bits) that contain all zeros.

In the framer mode or when TSIG = 1, ZCS is applied to all transmit time slots.

Table 5. DS1 ZCS Encoding

Input Bit Stream	00000000	01010000	00000000	00000000
AMI Data (framer mode)	00000010	01010010	00000010	00000010
T7230A Default AMI	00000010	01010000	00000000 (data time slot)	00000010

T1 Binary 8 Zero Code Suppression

The T7230A default line code is B8ZS. Clear channel transmission can be accomplished using binary 8 zero code suppression (B8ZS). Eight consecutive 0s are replaced with the B8ZS code. This code consists of two bipolar violations in bit position 4 and 7 and valid bipolar marks in bit positions 5 and 8. The receiving end recognizes this code and replaces it with the original string of eight 0s. Table 6 shows the encoding of a string of 0s using B8ZS. B8ZS can be used in any DS1 frame.

Table 6. DS1 B8ZS Encoding

Bit Positions	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**—**	**—**	**—**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Before B8ZS	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
After B8ZS	0	0	0	V	B	0	V	B	B	0	B	0	0	0	V	B	0	V	B

High-Density Bipolar of Order 3 (HDB3)

The line code used for CEPT is described in ITU Rec. G.703 Section 6.1 as high-density bipolar of order 3 (HDB3). HDB3 uses a substitution code that acts on strings of four 0s. The substitute HDB3 codes are 000V and B00V, where V represents a violation of the bipolar rule and B represents an inserted pulse conforming to the AMI rule defined in ITU Rec. G.701, item 9004. The choice of the B00V or 000V is made such that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no direct current (dc) component is introduced. The substitute codes follow each other if the string of 0s continues. The choice of the first substitute code is arbitrary. A line code error is as a bipolar violation and consists of two pulses of the same polarity that are not defined as one of the two substitute codes. An example is shown in Table 7.

Table 7. ITU HDB3 Coding and DCPAT Binary Coding

Input Bit Stream	1011	0000	01	0000	0000	0000	0000
HDB3-Coded Data	1011	000V	01	000V	B00V	B00V	B00V
HDB3-Coded Levels	–0+–	000–	0+	000+	–00–	+00+	–00–
HDB3 with 5 BPVs	–0+–	–000 1-BPV	0+	+00+ 3-BPV	0—— 5-BPV	+00+	–00–

Frame Formats

The T7230A supports the North American T1 framing format of superframe (D4, *SLC*-96, and digital data service-DDS) and extended superframe (ESF). The T7230A also supports the ITU CEPT-E1 basic format with and without CRC-4 multiframe formatting. This section describes the various framing formats.

T1 Framing Structures

T1 is a digital transmission line that multiplexes twenty-four 64 kbits/s time slots (DS0) onto a serial link. The T1 system is the lowest level of hierarchy on the North American T-carrier system, as shown in Table 8.

Table 8. T-Carrier Hierarchy

T Carrier	DS0 Channels	Bit Rate (Mbits/s)	T1 Hierarchy
T1	24	1.544	DS1
T1-C	48	3.152	DS1C
T2	96	6.312	DS2
T3	672	44.736	DS3
T4	4032	274.176	DS4

Frame, Superframe, and Extended Superframe Definitions

Each time slot (DS0) is comprised of 8 bits sampled every 125 µs (8 kHz). Multiplexing 24 of these 8-bit samples together produces a 192-bit (24 DS0s) frame. A framing bit is added to the beginning of each frame to allow for detection of frame boundaries and the transport of additional maintenance information. This 193-bit frame, also referred to as a DS1 frame, is repeated every 125 µs to yield the 1.544 Mbits/s T1 data rate. DS1 frames are bundled together to form superframes and extended superframes as shown in Figure 8.

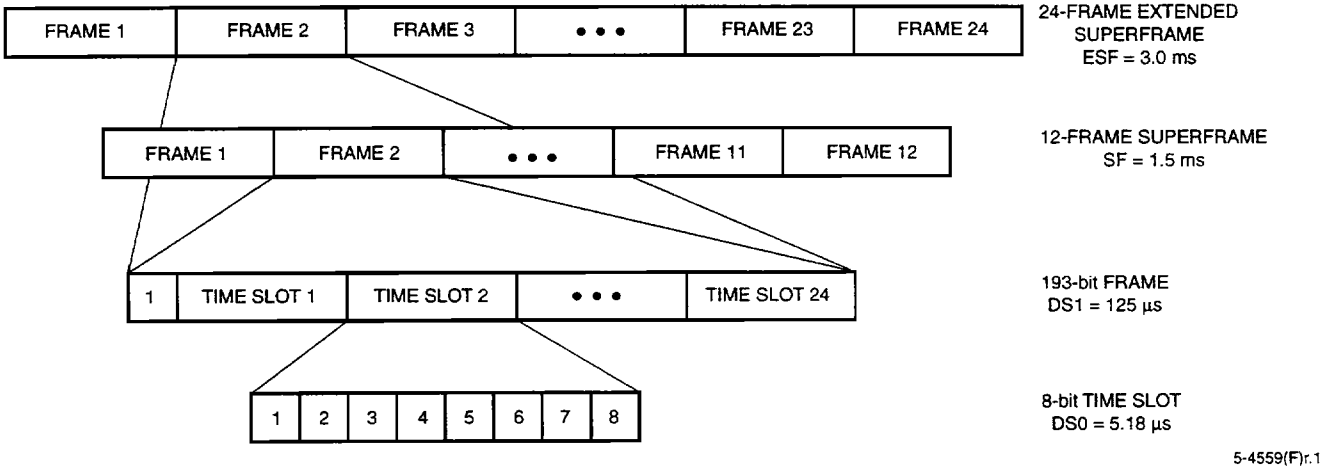


Figure 8. T1 Frame Structure

Frame Formats (continued)

T1 Framing Structures (continued)

D4 Frame Format

D4 superframe format consists of 12 DS1 frames. Table 9 shows the structure of the D4 superframe.

Table 9. D4 Superframe Format

Framing Bits				Bit Used in Each Time Slot			Signaling Options		
Frame Number	Bit Number	Terminal Frame FT	Signal Frame FS	Traffic (all channels)	Remote Alarm	Signal-ing	None	2 State	4 State
1	0	1	—	1—8	2	—	—	—	—
2	193	—	0	1—8	2	—	—	—	—
3	386	0	—	1—8	2	—	—	—	—
4	579	—	0	1—8	2	—	—	—	—
5	772	1	—	1—8	2	—	—	—	—
6	965	—	1	1—7	2	8	—	A	A
7	1158	0	—	1—8	2	—	—	—	—
8	1351	—	1	1—8	2	—	—	—	—
9	1544	1	—	1—8	2	—	—	—	—
10	1737	—	1	1—8	2	—	—	—	—
11	1930	0	—	1—8	2	—	—	—	—
12	2123	—	0	1—7	2	8	—	A	B

Notes:
The F bit of frame 1 is transmitted first.

Frames 6 and 12 contain the robbed-bit signaling information in bit 8 of each channel, when enabled for voice.

Signaling option none uses bit 8 for traffic data.

The remote alarm forces bit 2 of each time slot to a 0 state when enabled.

The remote alarm Japanese forces framing bit 12 (bit number 2123) to a 1 state when enabled.

The T7230A receive framer uses both the FT and FS framing bits during its frame alignment procedure. In addition, a stomp mode may be programmed to set all processed receive signaling bits to a 1 state to reduce the possibility of emulating the D4 framing pattern within the actual frame.

Digital Data Service (DDS) Frame Format

The superframe format for DDS is the same as that given for D4. DDS is intended to be used for data-only traffic, and as such, the system should ensure that the T7230A is in the nonsignaling mode (TSIG = 1). DDS uses channel 24 to transmit the remote frame alarm and data link bits. The format for channel 24 is shown in Table 10.

Table 10. DDS Channel 24 Format

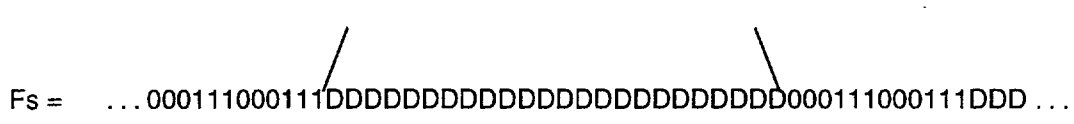
Channel 24 =	10111YD0
Y =	Remote frame alarm: 1= no alarm state; 0 = alarm state
D =	Data link bits (8 kbits/s)

Frame Formats (continued)

T1 Framing Structures (continued)

SLC-96 Frame Format

SLC-96 superframe format consists of 12 DS1 frames similar to D4. The FT pattern is exactly the same as D4. The FS uses that same structure as D4 but incorporates a data link 24-bit word every 12 FS bits.



Frame Formats (continued)

T1 Framing Structures (continued)

The T7230A transmit framer inserts the data at the transmit facility input port (XFD) into the Fs bits of the framing bit. The transmit framer synchronizes on XFD = 0011100111 . . . and forces a superframe based on this pattern. It is the system's responsibility to ensure valid XFD data. The valid XFD pattern is shown in Table 11. Table 12 shows the encoding for the line switch field.

Table 11. *SLC*-96 Data Link Block Format

Data Link Block	Bit Definition	Bit Value
D1	C1 – concentrator bit	0 or 1
D2	C2 – concentrator bit	0 or 1
D3	C3 – concentrator bit	0 or 1
D4	C4 – concentrator bit	0 or 1
D5	C5 – concentrator bit	0 or 1
D6	C6 – concentrator bit	0 or 1
D7	C7 – concentrator bit	0 or 1
D8	C8 – concentrator bit	0 or 1
D9	C9 – concentrator bit	0 or 1
D10	C10 – concentrator bit	0 or 1
D11	C11 – concentrator bit	0 or 1
D12	Spoiler bit 1	0
D13	Spoiler bit 2	1
D14	Spoiler bit 3	0
D15	M1 – maintenance bit	0 or 1
D16	M2 – maintenance bit	0 or 1
D17	M3 – maintenance bit	0 or 1
D18	A1 – alarm bit	0 or 1
D19	A2 – alarm bit	0 or 1
D20	S1 – line-switch bit	Defined in Table 12
D21	S2 – line-switch bit	Defined in Table 12
D22	S3 – line-switch bit	Defined in Table 12
D23	S4 – line-switch bit	Defined in Table 12
D24	Spoiler bit 4	1

Table 12. *SLC*-96 Line Switch Message Codes

S1	S2	S3	S4	Code Definition
1	1	1	1	Idle
1	1	1	0	Switch line A receive
1	1	0	1	Switch line B transmit
1	1	0	0	Switch line C transmit
1	0	1	0	Switch line D transmit
0	1	0	1	Switch line B transmit and receive
0	1	0	0	Switch line B transmit and receive
0	0	1	0	Switch line B transmit and receive

Frame Formats (continued)

T1 Framing Structures (continued)

Extended Superframe

The extended superframe format consists of 24 DS1 frames. The F bits are used for frame alignment, extended superframe alignment, error checking, and facility data link transport. Table 13 shows the ESF frame format.

Table 13. Extended Superframe (ESF) Structure

Frame Bit					Bit Use in Each Time Slot		Signaling Option			
Frame Number	Bit Number	FE	DL	CRC-6	Traffic	Signaling	None	2-State	4-State	16-State
1	0	—	D	—	1—8	—	—	—	—	—
2	193	—	—	C_1	1—8	—	—	—	—	—
3	386	—	D	—	1—8	—	—	—	—	—
4	579	0	—	—	1—8	—	—	—	—	—
5	772	—	D	—	1—8	—	—	—	—	—
6	965	—	—	C_2	1—7	8	—	A	A	A
7	1158	—	D	—	1—8	—	—	—	—	—
8	1351	0	—	—	1—8	—	—	—	—	—
9	1544	—	D	—	1—8	—	—	—	—	—
10	1737	—	—	C_3	1—8	—	—	—	—	—
11	1930	—	D	—	1—8	—	—	—	—	—
12	2123	1	—	—	1—7	8	—	A	B	B
13	2316	—	D	—	1—8	—	—	—	—	—
14	2509	—	—	C_4	1—8	—	—	—	—	—
15	2702	—	D	—	1—8	—	—	—	—	—
16	2895	0	—	—	1—8	—	—	—	—	—
17	3088	—	D	—	1—8	—	—	—	—	—
18	3281	—	—	C_5	1—7	8	—	A	A	C
19	3474	—	D	—	1—8	—	—	—	—	—
20	3667	1	—	—	1—8	—	—	—	—	—
21	3860	—	D	—	1—8	—	—	—	—	—
22	4053	—	—	C_6	1—8	—	—	—	—	—
23	4246	—	D	—	1—8	—	—	—	—	—
24	4439	1	—	—	1—7	8	—	A	B	D

Notes:
The F bit of frame 1 is transmitted first.

Frames 6, 12, 18, and 24 contain the robbed-bit signaling information in bit 8 of each voice channel, when enabled.

Signaling option none uses bit 8 for traffic data.

The C_1 to C_6 bits are the cyclic redundancy check-6 (CRC-6) checksum bits calculated over the previous extended superframe.

The remote alarm is a repeated 0000000011111111 pattern in the DL when enabled.

The ESF format allows for nondisruptive error detection and nonservice affecting diagnostics on T1 circuits. ESF format consists of 24 framing bits: 6 for framing synchronization (2 kbits/s); 6 for error detection (2 kbits/s); and 12 for facility data link information such as in-service monitoring and diagnostics (4 kbits/s).

Cyclic redundancy checking is performed over the entire ESF (4,632 data bits, all 24 framing bits are set to 1 during calculations). The use of CRC-6 allows for the detection of 63 out of 64 possible errors.

Frame Formats (continued)

T1 Framing Structures (continued)

The T7230A monitors the CRC-6 errors and tracks the performance categories defined in the AT&T Technical Reference 54016:

1. Errored events: any loss of frame alignment or CRC-6 errored checksum
2. Errored seconds: a 1 second period with a loss of frame event
3. Bursty errored seconds: a 1 second interval with more than 2 but less than 320 CRC-6 errors
4. Severely errored seconds: a 1 second interval with a loss of frame event, or 320 or more CRC-6 errors, or eight or more framing bit errors (SF format)

The T7230A maintains counters for each of these categories that can be accessed through the microprocessor interface.

The ESF remote frame alarm consists of a repeated pattern of eight 0s followed by eight 1s transmitted to the line interface in the data link position of the framing bits transmit frames.

T1 Loss of Frame Alignment (LFA)

Loss of frame alignment condition for the frame, superframe, or the extended superframe formats is caused by the inability of the receive framer to maintain the proper sequence of frame bits. The number of errored framing bits required to detect a loss of frame alignment is given in Table 14.

Table 14. T1 Loss of Frame Alignment Criteria

Format	Number of errored framing bits that will cause a loss of frame alignment state.
D4: Frame (AT&T)	2 errored frame bits (FT or FS) out of 4 consecutive frame bits.
D4: Frame (ANSI)	2 errored frame bits (FT or FS) out of 6 consecutive frame bits.
D4: SF	2 errored FS bits out of 4 consecutive FS bits.
SLC-96: Frame	2 errored frame bits (FT or FS) out of 4 consecutive frame bits.
SLC-96: SF	2 errored FS bits out of 4 consecutive FS bits.
DDS: Frame	4 errored frame bits (FT or FS) out of 12 consecutive frame bits.
ESF: (AT&T)	2 errored FE bits out of 4 consecutive FE bits.
ESF: (ANSI)	2 errored FE bits out of 6 consecutive FE bits.

The T7230A indicates the loss of frame and superframe states by setting the LFA (red alarm) and LSFA bits, respectively, in the status registers for the duration of the states. Once set, the local system may give an indication of its local LFA state to the remote end by transmitting a remote frame alarm (RFA or yellow alarm). In addition, while in the LFA state, the local end may transmit the alarm indication signal (AIS or blue alarm) to its system interface.

Frame Formats (continued)

T1 Frame Recovery Alignment Algorithms

While in the LFA state, a read of the LFA status register will cause the Loss_of_Frame_Alignment_from_Last_Read (LFALR) status bit to be set. LFALR will remain set while the current LFA state is active. The receive framer will force LFALR bit to **0** when frame alignment is established.

When in a loss of frame alignment state, the receive framer searches for a new frame alignment and forces its internal circuitry to this new alignment. The T7230A's synchronization circuit inhibits realignment in T1 framing formats when repetitive data patterns emulate the T1 frame alignment patterns. The loss of frame alignment will always force a loss of superframe alignment. T1 frame synchronization will not occur until all emulators disappear and only one valid pattern exists. Superframe alignment is established only after frame alignment has been determined in the D4 and *SLC*-96 frame format. Table 15 gives the requirements for establishing T1 frame and superframe alignment.

Table 15. T1 Frame Alignment Procedures

Frame Format	Alignment Procedure	Alignment Times (ms)
D4: frame	Using the FT frame position as the reference point, frame alignment is established when 24 consecutive FT and FS frame bit pairs (48 total frames) are received error-free. Once frame alignment is established, then superframe alignment is determined.	6
D4: superframe	After frame alignment is determined, two valid superframe bit sequences using only the FS bits must be received error-free to establish superframe alignment.	3
SLC-96: frame	Using the FT frame position as the reference point, frame alignment is established when 24 consecutive FT frame bits (48 total frames) are received error-free. Once frame alignment is established, superframe alignment is determined.	6
SLC-96: superframe	After frame alignment is determined, superframe alignment is established on the first valid superframe bit sequence using the FS bits that exist for two consecutive superframe periods.	6
DDS: frame	Using the FT frame position as the reference point, frame alignment is established when six consecutive FT and FS frame bits and the DDS FAS in time slot 24 are received error-free. In the DDS format, there is no search for a superframe structure.	0.75
ESF	Frame alignment is established simultaneously using the FE framing bit. Alignment is established when 24 consecutive FE bits are received error-free. Once frame alignment is established, the receive framer will force an LFA state whenever 32 consecutive CRC-6 errors are detected. This condition is indicated in the status registers (see Table 37, Interrupt Status Register (SR0), on page 71).	12

Frame Formats (continued)

T1 Robbed-Bit Signaling

Robbed-bit signaling, used in ESF and SF framing formats, "robs" the eighth bit of the voice channels of every sixth frame. The signaling bits are designated A, B, C, and D, depending on the signaling format used. The robbed bit signaling format is defined by programming the state of the F and G bits in the transmitted signaling registers. In the associated signaling mode, the T7230A can be programmed to use either the F and G bits obtained from the system interface, i.e., the concentration highway interface or from the F and G bits in the transmitted signaling registers.

The received channels robbed-bit signaling format is defined by the corresponding transmit signaling F and G bits.

Table 16. Robbed-Bit Signaling Options

G	F	Robbed-Bit Signaling Format	Frame			
			6	12	18	24
0	0	16-State	A	B	C	D
0	1	4-State	A	B	A	B
1	0	Data channel (no signaling)	PAYLOAD DATA			
1	1	2-State	A	A	A	A

The robbed-bit signaling format for each of the 24 T1 channels is programmed on a per-channel basis by setting the F and G bits in the transmit signaling direction.

SLC-96 9-State Signaling

The *SLC*-96 9-state signaling format is enabled by setting both the F and G bits in the signaling registers to the 0 state. In this state, A and B signaling bits can either be 0 or 1 or toggling. The transmitted A (B) signaling bit to the line interface can be made to toggle by writing A = 0 and C = 1 (B = 0 and D = 1) in the transmit signaling register. Writing A = C = 0 (B = D = 0) in the transmit signaling registers forces the signaling state A = 0 (B = 0) to be transmitted to the line interface. Writing A = 1 (B = 1) in the transmit signaling registers forces A = 1 (B = 1) to be transmitted to the line interface. Table 17 shows the state of the transmitted A and B bits to the line as a function of the A and B bit settings in the transmit signaling registers.

Table 17. *SLC*-96 9-State Signaling Format

Transmit Signaling Registers Settings					Transmit to the Line Signal Bits	
***SLC*-96 Signaling States**	**A**	**B**	**C**	**D**	**A = f(A, C)**	**B = f(B, D)**
State 1	0	0	0	0	0	0
State 2	0	0	0	1	0	T
State 3	0	1	0	X	0	1
State 4	0	0	1	0	T	0
State 5	0	0	1	1	T	T
State 6	0	1	1	X	T	1
State 7	1	0	X	0	1	0
State 8	1	0	X	1	1	T
State 9	1	1	X	X	1	1

Frame Formats (continued)

CEPT 2.048 Basic Frame Structure

The ITU Rec. G.704 Section 2.3.1 defined frame length is 256 bits, numbered 1 to 256. The frame repetition rate is 8 kHz. The allocation of bits numbered 1 to 8 of the frame is shown in Table 18.

Table 18. Allocation of Bits 1 to 8 of the FAS Frame and the NOT FAS Frame

Basic Frames	Bit 1 (MSB)	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8 (LSB)
Frame Alignment Signal (FAS)	Si	0	0	1	1	0	1	1
Not Frame Alignment Signal	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

The function of each bit in Table 18 is described below:

1. The Si bits are reserved for international use. A specific use for these bits is described in the CRC-4 Multiframe section. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border.
2. Bit 2 of the frames not containing the FAS (i.e., the NOT FAS frames) is fixed to 1 to assist in avoiding simulations of the frame alignment signal.
3. Bit 3 of the NOT FAS is the remote alarm indication (A bit). In undisturbed operation, A bit = 0; in alarm condition, A bit = 1.
4. Bits 4—8 of the NOT FAS may be recommended by ITU for use in specific point-to-point applications. Bit Sa4 may be used as a message-based data link for operations, maintenance, and performance monitoring. If the data link is accessed at intermediate points with consequent alterations to the Sa4 bit, the CRC-4 bits must be updated to retain the correct end-to-end path termination functions associated with the CRC-4 procedure. The receive framer does not implement the CRC-4 modifying algorithm described in ITU Rec. G.706 Annex C. Bits Sa4—Sa8, where these are not used, should be set to 1 on links crossing an international border.
5. MSB = most significant bit. This bit is transmitted first.
6. LSB = least significant bit. This bit is transmitted last.

The T7230A may be programmed in a frame transparent mode. This mode transmits the received system data to the line transparently, i.e., the FAS and NOT FAS time slots are not modified by the transmit framer. The system-frame sync (FS) is used to define time slot 0 through the transmit framer. While in this mode the receive framer will **not** align to the received line data. Setting PR8 bits[0:5] to 1 forces the transmit and receive framers into this state.

CEPT Loss of Basic Frame Alignment (LFA)

Frame alignment is assumed to be lost when:

1. As described in ITU Rec. G.706 Section 4.1.1, three consecutive incorrect frame alignment signals have been received.
2. So as to limit the effect of spurious frame alignment signals, when bit 2 in time slot 0 in NOT FAS frames have been received with an error on three consecutive occasions.
3. Optionally, as described in ITU Rec. G.706 Section 4.3.2, by exceeding a count of >914 errored CRC-4 blocks out of 1000, with the understanding that a count of ≥915 errored CRC blocks indicates false frame alignment.
4. On demand via the control registers.

Frame Formats (continued)

CEPT Loss of Basic Frame Alignment (LFA) (continued)

In the LFA state:

1. No additional FAS or NOT FAS errors are processed.
2. The received remote frame alarm (received A-bit) is deactivated.
3. All NOT-FAS bit (Si bit, A bit and Sa4 to Sa8 bits) processing is halted.
4. Receive Sa6 status bits are set to 0.
5. Receive Sa6 code monitoring and counting is halted.
6. RFD = 1 and RFCK maintains previous alignment.
7. Optionally, the remote alarm indication (A = 1) may be automatically transmitted to the line.
8. Optionally, the alarm indication signal (AIS) may be automatically transmitted to the system.
9. If CRC-4 is enabled, loss of CRC-4 multiframe alignment is forced.
10. If CRC-4 is enabled, the monitoring and processing of CRC-4 checksum errors is halted.
11. If CRC-4 is enabled, all monitoring and processing of received E-bit information is halted.
12. If CRC-4 is enabled, deactivate the receive continuous E-bit alarm, i.e., force CREB = 0.
13. If CRC-4 is enabled, optionally, E = 0 is transmitted to the line for the duration of loss of CRC-4 multiframe alignment.
14. If channel associated or common channel signaling is enabled, loss of the signaling multiframe alignment is forced.
15. If channel associated or common channel signaling is enabled, updating of the signaling data is halted.

CEPT Loss of Frame Alignment Recovery Algorithm

As defined in ITU Rec. G.706.4.1.2, frame alignment will be assumed to have been recovered when the following sequence is detected:

1. For the first time, the presence of the correct frame alignment signal in frame n.
2. The absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a 1 in frame n + 1.
3. For the second time, the presence of the correct frame alignment in the next frame, n + 2.

Failure to meet 2 or 3 above will initiate a new basic frame search in frame n +2.

Frame Formats (continued)

CEPT Loss of Frame Alignment Recovery Algorithm (continued)

As defined in ITU Rec. G.704, the CEPT 2.048 frame, CRC-4 multiframe, and channel associated signaling multiframe structures are illustrated in Figure 9.

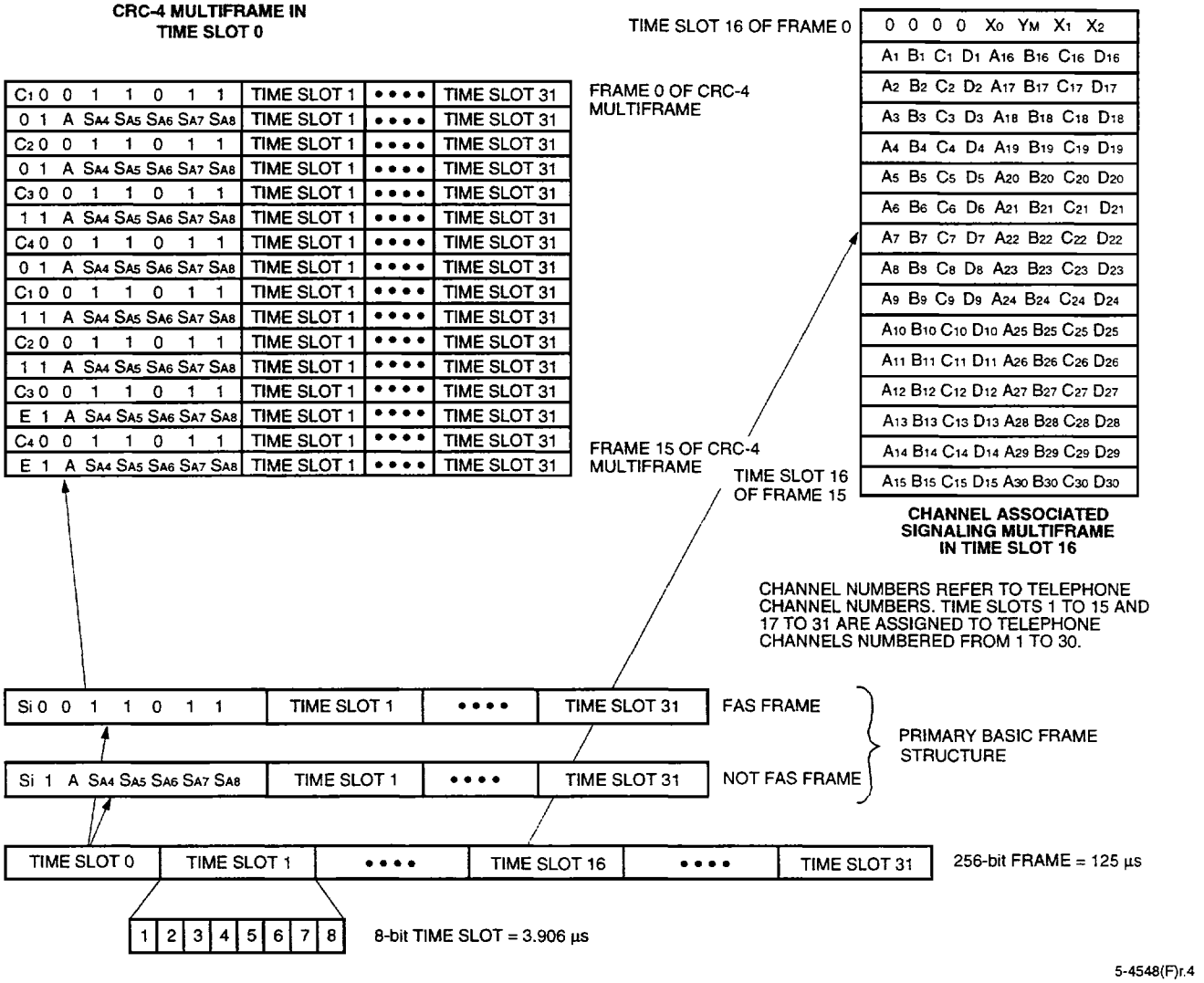


Figure 9. ITU 2.048 Basic Frame, CRC-4 Multiframe, and Channel Associated Signaling Multiframe Structures

Frame Formats (continued)

CEPT Time Slot 0 CRC-4 Multiframe Structure

The CRC-4 multiframe is in bit 1 of the frame. As described in ITU Rec. G.704 Section 2.3.3.1, where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 of each frame may be used for a cyclic redundancy check-4 (CRC-4) procedure as detailed below. The allocation of bits 1—8 of the frame is shown in Table 19 for the complete CRC-4 multiframe.

Table 19. ITU CRC-4 Multiframe Structure of the T7230A

	Submultiframe (SMF)	Frame Number	Bits							
			1	2	3	4	5	6	7	8
Multiframe	I	0	C1	0	0	1	1	0	1	1
		1	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		2	C2	0	0	1	1	0	1	1
		3	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		4	C3	0	0	1	1	0	1	1
		5	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		6	C4	0	0	1	1	0	1	1
		7	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	II	8	C1	0	0	1	1	0	1	1
		9	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		10	C2	0	0	1	1	0	1	1
		11	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		12	C3	0	0	1	1	0	1	1
		13	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
		14	C4	0	0	1	1	0	1	1
		15	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

Notes:
C1 to C4 = cyclic redundancy check-4 (CRC-4) bits.

E = CRC-4 error indication bits.

Sa4 to Sa8 = spare bits.

A = remote frame alarm (RFA) bit (active-high); referred to as the A bit.

The CRC-4 multiframe consists of 16 frames numbered 0 to 15 and is divided into two eight-frame submultiframes (SMF), designated SMF-I and SMF-II that signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the CRC-4 block size (2048 bits). In those frames containing the frame alignment signal (FAS), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C1, C2, C3, and C4 in each SMF. In those frames not containing the frame alignment signal (NOT FAS), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E). The multiframe alignment signal is defined in ITU Rec. G.704 Section 2.3.3.4, as 001011. Transmitted E bits should be set to 0 until both basic frame and CRC-4 multiframe alignment are established. Thereafter, the E bits should be used to indicate received errored submultiframes by setting the binary state of one E bit from 1 to 0 for each errored submultiframe. The received E bits will always be taken into account, by the receive E-bit processor*, even when the SMF that contains them is found to be errored. In the case where there exists equipment that does not use the E bits, the state of the E bits should be set to a binary 1 state.

The CRC-4 word, located in submultiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of the submultiframe N – 1.

* The receive E-bit processor will halt the monitoring of the received E bit during the loss of CRC-4 multiframe alignment.

Frame Formats (continued)

CEPT Time Slot 0 CRC-4 Multiframe Structure (continued)

Representing the contents of the submultiframe check block as a polynomial, the first bit in the block, i.e., frame 0, bit 1 or frame 8, bit 1, is taken as being the most significant bit and the least significant bit in the check block is frame 7 or frame 15, bit 256. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder. The encoding procedure, as described in ITU Rec. G.704 Section 2.3.3.5.2, follows:

1. The CRC-4 bits in the SMF are replaced by binary 0s.
2. The SMF is then acted upon the multiplication/division process referred to above.
3. The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

The decoding procedure, as described in ITU Rec. G.704 Section 2.3.3.5.3, follows:

1. A received SMF is acted upon by the multiplication/division process referred to above, after having its CRC-4 bits extracted and replaced by 0s.
2. The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.
3. If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error-free.

CEPT Loss of CRC-4 Multiframe Alignment (LTS0MFA)

Loss of basic frame alignment forces the receive framer into a loss of CRC-4 multiframe alignment state. This state is reported by way of the status registers, and once basic frame alignment is achieved, a new search for CRC-4 multiframe alignment is initiated. During a loss of CRC-4 multiframe alignment state:

1. The CRC-4 error counter is halted.
2. The CRC-4 error monitoring circuit for errored seconds and severely errored seconds is halted.
3. The received E-bit monitoring circuit is halted.
4. Receive continuous E-bit monitoring is halted.
5. All receive Sa6 code monitoring and counting functions are halted.
6. Optionally, A = 1 may be automatically transmitted to the line.
7. Optionally, E = 0 may be automatically transmitted to the line.

Frame Formats (continued)

CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms

Several optional algorithms exist in the receive framer.

CRC-4 Multiframe Alignment Algorithm with 8 ms Timer

The default algorithm is as described in ITU Rec. G.706 Section 4.2. The recommendation states that if a condition of assumed frame alignment has been achieved, CRC-4 multiframe alignment is deemed to have occurred if at least two valid CRC-4 multiframe alignment signals can be located within 8 ms, the time separating two CRC-4 multiframe signals being 2 ms or a multiple of 2 ms. The search for the CRC-4 multiframe alignment signal is made only in bit 1 of NOT FAS frames. If multiframe alignment cannot be achieved within 8 ms, it is assumed that frame alignment is due to a spurious frame alignment signal and a new parallel search for basic frame alignment is initiated. The new search for the basic frame alignment is started at the point just after the location of the assumed spurious frame alignment signal. During this parallel search for basic frame alignment, there is no indication to the system of an RLFA state. The receive framer will continuously search for CRC-4 multiframe alignment if no other CRC-4 multiframe algorithm is used. Once found, the receive framer will force its internal timing to this new alignment, if it is different from the original primary basic frame alignment:

1. During the search for CRC-4 multiframe alignment, traffic is allowed through upon, and synchronized to, the initially determined primary basic frame alignment.
2. Upon detection of the CRC-4 multiframe, the basic frame alignment associated with the CRC-4 multiframe alignment replaces, if necessary, the initially determined basic frame alignment.

CRC-4 Multiframe Alignment Algorithm with 100 ms Timer

This CRC-4 multiframe reframe mode starts a 100 ms timer upon detection of basic frame alignment. This is a parallel timer to the 8 ms timer. If CRC-4 multiframe alignment cannot be achieved within the time limit of 100 ms owing to the CRC-4 procedure not being implemented at the transmitting side, then an indication is given, and actions are taken equivalent to those specified for loss of basic frame alignment, namely:

1. Optional automatic transmission of A = 1 to the line while in loss of CRC-4 multiframe state.
2. Optional automatic transmission of E = 0 to the line while in loss of CRC-4 multiframe state.
3. Optional automatic transmission of AIS to the system while in loss of CRC-4 multiframe state.

Frame Formats (continued)

CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms (continued)

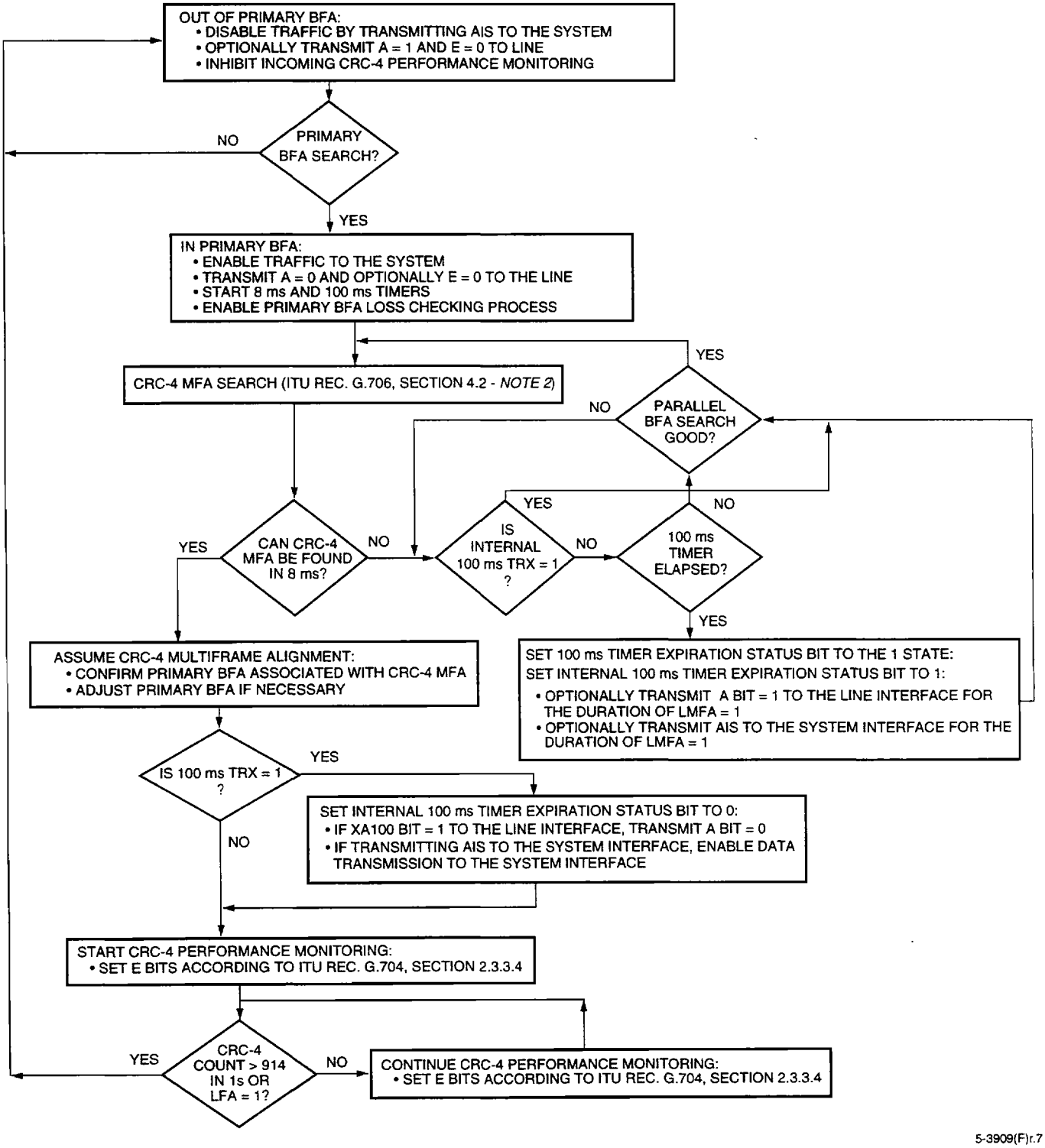


Figure 10. Receive CRC-4 Multiframe Search Algorithm Using the 100 ms Internal Timer

Frame Formats (continued)

CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms (continued)

CRC-4 Multiframe Alignment Search Algorithm with 400 ms Timer

This receive CRC-4 multiframe reframe mode is the modified CRC-4 multiframe alignment algorithm described in ITU Rec. 706 Annex B, where it is referred to as CRC-4-to-Non-CRC-4 equipment interworking. A flow diagram of this algorithm is illustrated in Figure 11. When the interworking algorithm is enabled, it supersedes the algorithm described in option 2 above. This algorithm assumes that a valid basic frame alignment signal is consistently present but the CRC-4 multiframe alignment cannot be achieved by the end of the total CRC-4 multiframe alignment search period of 400 ms, if the remote end is a non-CRC-4 equipment. In this mode, the following consequent actions are be taken:

1. An indication that there is no incoming CRC-4 multiframe alignment signal.
2. CRC-4 data is transmitted to the distant end with both E bits set to zero.

This algorithm allows the identification of failure of CRC-4 multiframe alignment generation/detection, but with correct basic framing, when interworking between equipment each having the modified CRC-4 multiframe alignment algorithm.

As described in ITU Rec. G.706 Section B.2.3:

1. A 400 ms timer starts on the initial recovery of the primary basic frame alignment.
2. The 400 ms timer reset if and only if:
   A. The criteria for loss of basic frame alignment as described in ITU Rec. G.706 Section 4.1.1 is achieved.
   B. If 915 out of 1000 errored CRC-4 blocks are detected resulting in a loss of basic frame alignment as described in ITU Rec. G.706 Section 4.3.2.
   C. On-demand reframe is requested.
   D. The receive framer is programmed to the non-CRC-4 mode.
3. The loss of basic frame alignment checking process runs continuously irrespective of the state of the CRC-4 multiframe alignment process below it.
4. A new search for frame alignment is initiated if CRC-4 multiframe alignment cannot be achieved in 8 ms as described in ITU Rec. G.706 Section 4.2. This new search for basic frame alignment will not reset the 400 ms timer or invoke consequent actions associated with loss of the primary basic frame alignment. In particular, all searches for basic frame alignment are carried out in parallel with, and independent of, the primary basic frame loss checking process. All subsequent searches for CRC-4 multiframe alignment are associated with each basic framing sequence found during the parallel search.
5. During the search for CRC-4 multiframe alignment, traffic is allowed through upon, and synchronized to, the initially determined primary basic frame alignment.
6. Upon detection of the CRC-4 multiframe before the 400 ms timer elapsing, the basic frame alignment associated with the CRC-4 multiframe alignment replaces, if necessary, the initially determined basic frame alignment*.
7. If CRC-4 multiframe alignment is not found before the 400 ms timer elapses, it is assumed that a condition of interworking between equipment with and without CRC-4 capability exists and the actions described above are taken.
8. If the 2.048 Mbits/s path is reconfigured at any time, then it is assumed that the (new) pair of path terminating equipment will need to re-establish the complete framing process, and the algorithm is reset.

* The basic frame may be aligned to the primary basic frame or may not be aligned to the primary basic frame. If the later, the new basic frame alignment is forced and one frame of transmitted system data is corrupted.

Frame Formats (continued)

CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms (continued)

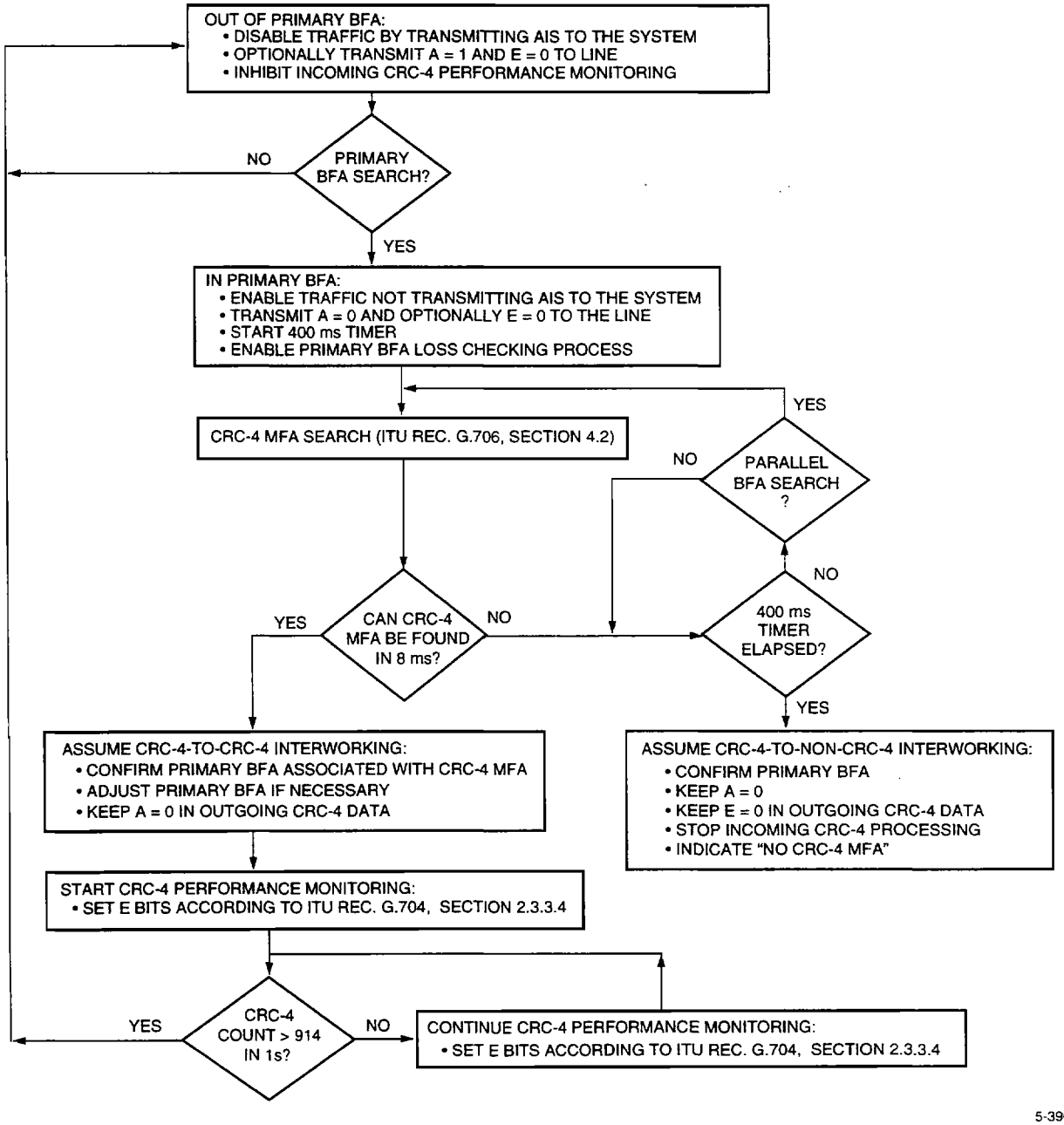


Figure 11. T7230A Receive CRC-4 Multiframe Search Algorithm for Automatic, CRC-4/Non-CRC-4 Equipment Interworking as Defined by ITU (From ITU Rec. G.706, Annex B.2.2 - 1991)

Frame Formats (continued)

CEPT Time Slot 16 Multiframe Structure

The T7230A supports three CEPT signaling modes: channel associated signaling (CAS) or per-channel signaling (PSC0 and PSC1); common channel signaling (CCS); and international remote switching module (ISM) signaling.

Channel Associated Signaling

The channel associated signaling (CAS) mode utilizes time slot 16 of the FAS and NOT FAS frames. The CAS format is a multiframe consisting of 16 frames where frame 0 of the multiframe contains the multiframe alignment pattern of four zeros in bits 1 through 4. Table 20 illustrates the CAS multiframe structure of time slot 16. The T7230A can be programmed to force the transmitted line CAS multiframe alignment pattern to be transmitted in the FAS frame by selecting the PCS0 option or in the NOT FAS frame by selecting the PCS1 option. Alignment of the transmitted line CAS multiframe to the CRC-4 multiframe is arbitrary. The receive line CAS alignment is defined by the received data.

Table 20. ITU CEPT Time Slot 16 Channel Associated Signaling Multiframe Structure

	Frame Number	Bits							
		1	2	3	4	5	6	7	8
Time Slot 16 Channel Associated Signaling Multiframe	0	0	0	0	0	X_0	Y_M	X_1	X_2
	1	A_1	B_1	C_1	D_1	A_{17}	B_{17}	C_{17}	D_{17}
	2	A_2	B_2	C_2	D_2	A_{18}	B_{18}	C_{18}	D_{18}
	3	A_3	B_3	C_3	D_3	A_{19}	B_{19}	C_{19}	D_{19}
	4	A_4	B_4	C_4	D_4	A_{20}	B_{20}	C_{20}	D_{20}
	5	A_5	B_5	C_5	D_5	A_{21}	B_{21}	C_{21}	D_{21}
	6	A_6	B_6	C_6	D_6	A_{22}	B_{22}	C_{22}	D_{22}
	7	A_7	B_7	C_7	D_7	A_{23}	B_{23}	C_{23}	D_{23}
	8	A_8	B_8	C_8	D_8	A_{24}	B_{24}	C_{24}	D_{24}
	9	A_9	B_9	C_9	D_9	A_{25}	B_{25}	C_{25}	D_{25}
	10	A_{10}	B_{10}	C_{10}	D_{10}	A_{26}	B_{26}	C_{26}	D_{26}
	11	A_{11}	B_{11}	C_{11}	D_{11}	A_{27}	B_{27}	C_{27}	D_{27}
	12	A_{12}	B_{12}	C_{12}	D_{12}	A_{28}	B_{28}	C_{28}	D_{28}
	13	A_{13}	B_{13}	C_{13}	D_{13}	A_{29}	B_{29}	C_{29}	D_{29}
	14	A_{14}	B_{14}	C_{14}	D_{14}	A_{30}	B_{30}	C_{30}	D_{30}
	15	A_{15}	B_{15}	C_{15}	D_{15}	A_{31}	B_{31}	C_{31}	D_{31}

Notes:
Frame 0 bits 1—4 define the time slot 16 multiframe alignment.

X0—X2 = time slot 16 spare bits.

Ym = time slot 16 remote multiframe alarm (RMA) bit (1 = alarm condition).

Frame Formats (continued)

CEPT Time Slot 16 Multiframe Structure (continued)

IRSM Signaling

This signaling mode is similar to the channel associated signaling mode, i.e., time slot 16 contains the signaling multiframe information (ABCD signaling bits). In addition, time slot 0 Sa5 to Sa8 bit positions of the NOT FAS frame contains per-channel control information. The format of the time slot 0 per-channel control information is illustrated in Table 21. The IRSM mode forces the transmit framer to align the time slot 16 multiframe to the FAS frame (PCS0 mode).

Table 21. CEPT IRSM Signaling Multiframe Structure

Frame Number	IRSM Bits in Time Slot 0								Bits in Time Slot 16							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
0	Si	0	0	1	1	0	1	1	0	0	0	0	X_0	Y_M	X_1	X_2
1	Si	1	A	D	E_0	E_1	E_{16}	E_{17}	A_1	B_1	C_1	D_1	A_{17}	B_{17}	C_{17}	D_{17}
2	Si	0	0	1	1	0	1	1	A_2	B_2	C_2	D_2	A_{18}	B_{18}	C_{18}	D_{18}
3	Si	1	A	D	E_2	E_3	E_{18}	E_{19}	A_3	B_3	C_3	D_3	A_{19}	B_{19}	C_{19}	D_{19}
4	Si	0	0	1	1	0	1	1	A_4	B_4	C_4	D_4	A_{20}	B_{20}	C_{20}	D_{20}
5	Si	1	A	D	E_4	E_5	E_{20}	E_{21}	A_5	B_5	C_5	D_5	A_{21}	B_{21}	C_{21}	D_{21}
6	Si	0	0	1	1	0	1	1	A_6	B_6	C_6	D_6	A_{22}	B_{22}	C_{22}	D_{22}
7	Si	1	A	D	E_6	E_7	E_{22}	E_{23}	A_7	B_7	C_7	D_7	A_{23}	B_{23}	C_{23}	D_{23}
8	Si	0	0	1	1	0	1	1	A_8	B_8	C_8	D_8	A_{24}	B_{24}	C_{24}	D_{24}
9	Si	1	A	D	E_8	E_9	E_{24}	E_{25}	A_9	B_9	C_9	D_9	A_{25}	B_{25}	C_{25}	D_{25}
10	Si	0	0	1	1	0	1	1	A_{10}	B_{10}	C_{10}	D_{10}	A_{26}	B_{26}	C_{26}	D_{26}
11	Si	1	A	D	E_{10}	E_{11}	E_{26}	E_{27}	A_{11}	B_{11}	C_{11}	D_{11}	A_{27}	B_{27}	C_{27}	D_{27}
12	Si	0	0	1	1	0	1	1	A_{12}	B_{12}	C_{12}	D_{12}	A_{28}	B_{28}	C_{28}	D_{28}
13	Si	1	A	D	E_{12}	E_{13}	E_{28}	E_{29}	A_{13}	B_{13}	C_{13}	D_{13}	A_{29}	B_{29}	C_{29}	D_{29}
14	Si	0	0	1	1	0	1	1	A_{14}	B_{14}	C_{14}	D_{14}	A_{30}	B_{30}	C_{30}	D_{30}
15	Si	1	A	D	E_{14}	E_{15}	E_{30}	E_{31}	A_{15}	B_{15}	C_{15}	D_{15}	A_{31}	B_{31}	C_{31}	D_{31}

Notes:
Si = time slot 0 control bits. If programmed for CRC-4 mode, then these bits contain the CRC-4 multiframe pattern, checksum, and E-bit information.

Ei = IRSM per-channel control bits.

X0—X2 = time slot 16 spare bits.

Ai—Di = time slot 16 channel associated signaling bits.

Frame Formats (continued)

CEPT Loss of Time Slot 16 Multiframe Alignment (LTS16MFA)

Loss of basic frame alignment forces the receive framer into a loss of time slot 16 signaling multiframe alignment state. As defined in ITU Rec. G.732 Section 5.2, time slot 16 signaling multiframe is assumed lost when two consecutive time slot 16 multiframe 4-bit all-zero patterns are received with an error. In addition, the time slot 16 multiframe is assumed lost when, for a period of two multiframes, all bits in time slot 16 are in state 0. This state is reported in the status registers. Once basic frame alignment is achieved, the T7230A will initiate a search for the time slot 16 multiframe alignment. During a loss of time slot 16 multiframe alignment state:

1. The updating of the signaling data is halted.
2. The received control bits forced to the binary 1 state.
3. The received remote multiframe alarm indication status bit is forced to the binary 0 state.
4. Optionally, the transmit framer can transmit the time slot 16 signaling remote multiframe alarm.
5. Optionally, the receive framer can transmit the alarm indication signal (AIS) in the system transmit time slot 16 data.

CEPT Loss of Time Slot 16 Multiframe Alignment Recovery Algorithm

The time slot 16 multiframe alignment recovery algorithm is as described in ITU Rec. G.732 Section 5.2. The recommendation states that if a condition of assumed frame alignment has been achieved, time slot 16 multiframe alignment is deemed to have occurred when the 4-bit time slot 16 multiframe pattern of 0000 is found in time slot 16 for the first time and the preceding time slot 16 contained at least one bit in the binary 1 state.

CEPT Time Slot 0 FAS/NOT FAS Control Bits

FAS/NOT FAS Si- and E-Bit Source

The Si bit can be used as an 8 kbits/s data link to and from the remote end, or in the CRC-4 mode, it is used to provide added protection against false frame alignment. In the LFA state, receive Si = 1 in the status registers. The sources for the Si bit that are transmitted to the line by order of priority are:

1. Non-CRC-4 mode: the SiF control bit in bit 1 of all FAS frames and the SiNF control bit in bit 1 of all NOT FAS frames. This is the default transmission mode.
2. The CHI system interface. This option requires the received system data (DRA or DRB) to maintain a biframe alignment pattern where frames containing Si bit information for the NOT FAS frames have bit 2 of time slot 0 in the binary 1 state followed by frames containing Si bit information for the FAS frames have bit 2 of time slot 0 in the binary 0 state. This ensures the proper alignment of the Si received system data to the transmit line Si data. Whenever this requirement is not met by the system, the T7230A transmit framer will enter a loss of biframe alignment condition (indication is given in the status registers) and then search for the pattern; in the loss of biframe alignment state, transmitted line data is corrupted (only when the system interface is sourcing stand or Si data). When the transmit framer locates a new biframe alignment pattern, an indication is given in the status registers and the transmit framer resumes normal operations.
3. A secondary option assumes that every time slot 0 of DRA (or DRB) consists of the NOT FAS Sa bits (every two frames contain the same NOTFAS data in time slot 0). The transmit framer transmits the Sa bits transparently from either the even or odd frame of DRA. The choice of even or odd frames is arbitrary.
4. CRC-4 mode:[1]
   A. If not automatically transmitting E bits to the distant end (default):
      a. Bit 1 of frame 13 = the SiF control bit, and bit 1 of frame 15 = the SiNF control bit.
   B. If automatically transmitting E bits (ATERCRCE = 1) to the line interface, the Si bits in frames 13 and 15 are controlled by the state of the receive framer such that:
      a. One transmitted E bit is set to 0 by the transmit framer, as described in ITU Rec. G.704 Section 2.3.3.4, for each received errored CRC-4 submultiframe detected by the receive framer,
      b. As described in ITU Rec. G.704 Section 2.3.3.4, both E bits are set to 0 while in a received loss of CRC-4 multiframe alignment state[2].
      c. When the 400 ms timer is enabled[3] and this 400 ms timer has expired, as described in ITU Rec. G.706 Section B.2.2, both E bits are set to 0 for the duration of the loss of CRC-4 multiframe alignment state[3].

Otherwise, the E bits are transmitted to the line in the 1 state.

1. The receive E-bit processor will halt the monitoring of received E-bits during loss of CRC-4 multiframe alignment.
2. Whenever loss of frame alignment occurs, then loss of CRC-4 multiframe alignment is forced. Once frame alignment is established, then and only then is the search for CRC-4 multiframe alignment initiated. The receiver framer unit, when programmed for CRC-4, can be in a state of LFA and LMFA or LMFA only, but can never be in a LFA only state.
3. The CRC-4 interworking algorithm can only be enabled if and only if the receive framer is in the CRC-4 mode.

CEPT Time Slot 0 FAS/NOT FAS Control Bits (continued)

NOT FAS A-Bit Sources

The A bit, as described in ITU Rec. G.704 Section 2.3.2 Table 4a/G.704, is the remote alarm indication bit. In undisturbed conditions, this bit is set to 0 and transmitted to the line. In the LFA state, receive A bit = 1 in the status registers. The A bit is set to 1 and transmitted to the line for the following conditions:

1. Setting the transmit A bit = 1 control bit.
2. *Optionally for the following alarm conditions:*
   A. The duration of loss of basic frame alignment as described in ITU Rec. G.706 Section 4.1.1[1], or ITU Rec. G.706 Section 4.3.2[2], or due to on-demand reframe from control register (XALFA).
   B. The duration loss of CRC-4 multiframe alignment (XALMFA).
   C. The duration loss of CRC-4 multiframe alignment after either the 100 ms or 400 ms timer expires.

1. LFA is due to three consecutive frames with incorrect frame alignment signals having been received or three consecutive frames not containing the frame alignment signals with bit 2 received with an error.
2. LFA is due to detecting 915 out of 1000 received CRC-4 errored blocks.

NOT FAS Sa-Bit Sources

The Sa bits in the NOT FAS frame can be a 4 kbits/s data link to and from the remote end. The sources for the Sa bits are by order of priority.

1. The Sa control register (default source).
2. The facility data link interface.
3. The CHI system interface.
   A. This is the default mode and requires the received system data (DRA or DRB) to maintain a biframe alignment pattern where frames containing Sa bit information have bit 2 of time slot 0 in the binary 1 state followed by frames not containing Sa bit information having bit 2 of time slot 0 in the binary 0 state. This ensures the proper alignment of the Sa received system data to the transmit line Sa data. Whenever this requirement is not met by the system, the T7230A transmit framer will enter a loss of biframe alignment condition (indication is given in the status registers) and then search for the pattern; in the loss of biframe alignment state, transmitted line data is corrupted (only when the system interface is sourcing Sa or Si data). When the transmit framer locates a new biframe alignment pattern, an indication is given in the status registers and the transmit framer resumes normal operations.
   B. When PR3, bit 1 = 1 and PR6, bit 6 = 1, the transmit framer will align its NOT FAS time slot to either the odd-numbered framers from the receive CHI interface and transmit the Sa bit positions in this frame as valid Sa data. The choice of even or odd is arbitrary. The "other" frame is ignored.

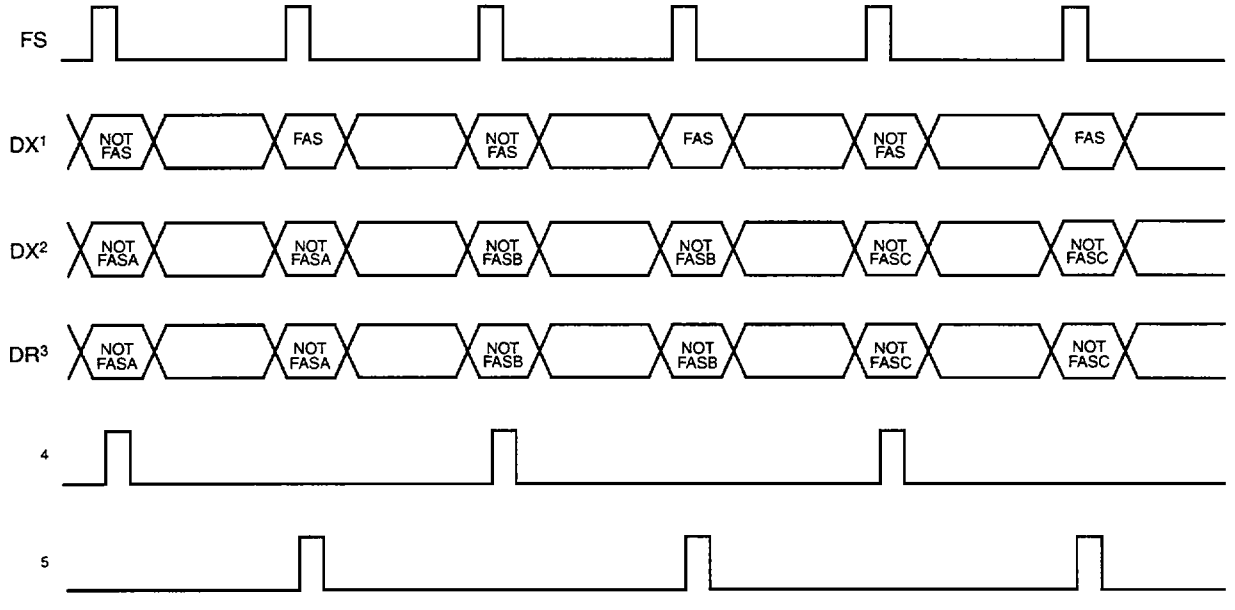
CEPT Time Slot 0 FAS/NOT FAS Control Bits (continued)

NOT FAS Sa-Bit Sources (continued)

The receive Sa data is always present at:

1. The system transmit interface.

When in CEPT format, and PR3, bit 1 = 1, the receive framer will copy its NOT FAS time slot 0 into time slot 0 of both the NOT FAS and the FAS frames that appear on the system interface (DRA, DRB).



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1. Normal transmission of FAS and NOT FAS time slot 0 data from the system transmit port of the T7230A.
2. Double NOT FAS transmission time slot 0 data from the system transmit port if the T7230A: PR3, bit 1 = 1.
3. Double NOT FAS reception time slot 0 data from the system receive port of the T7230A: PR3, bit 1 = 1 and PR6, bit 6 = 1.
4. The transmit framer arbitrarily assigns these frames as NOT FAS frames and transmits the Sa bit to the line.
5. Or, the transmit framer arbitrarily assigns these frames as NOT FAS frames and transmits the Sa bit to the line.

Note: If PR6, bit 6 = 1 and PR3, bit 1 = 0, then the transmit framer will always look for the alternating 10 pattern in bit 2 of time slot 0 to determine the FAS and NOT FAS frames.

Figure 12. CEPT AFS and NOT FAS System Interface Format

2. The Sa status register.

The selected Sa bit for facility data link interface is always present at the receive facility data link interface. In the LFA state, RFD = 1.

CEPT Time Slot 0 FAS/NOT FAS Control Bits (continued)

Sa Facility Data Link Access

The data link interface may be used to source one of the Sa bits. When enabled, this transmit access mode supersedes all access modes for the selected Sa bit. The receive Sa data is always present at the receive facility data link output pin, RFD, along with a valid clock signal at the receive facility clock output pin, RFCK. During an LFA state, the RFD signal is forced to a 1 state and RFCK continues to toggle on the basic frame alignment. When basic frame alignment is found, RFD is as received from the selected RSa bit position and RFCK is forced (if necessary) to the new alignment. The data rate for this access mode is 4 kHz.

Microprocessor Sourcing of the Si and Sa4 to Sa8 Bits

The microprocessor sourcing mode for the Si and Sa4 to Sa8 bits is the control register. Programming PR6, bit 6 to 1 enables the information in the control register corresponding to the Sa4 to Sa8 bits to be transmitted to the line. Programming PR7, bit 6 to 1 enables the information in the control registers corresponding to the Si bits to be transmitted to the line. The receive Si and Sa4 to Sa8 bits from the last valid NOT FAS frame are always in the NOT FAS status register.

CEPT Time Slot 16 X0—X2 Control Bits

The three X bits in frame 0 of the time slot 16 multiframe can be used as a 0.5 kbits/s data link to and from the remote end. The transmitted line X bits are sourced from the control registers. In the LMFA state, receive X bits = 1 in the status registers.

Signaling Access

Signaling information can be accessed by three different methods: transparently through the CHI, through the control registers, or through the CHI associated signaling mode.

Transparent Signaling (TSIG = 1)

Data at the received DRA and DRB interface passes through the T7230A undisturbed. The system is responsible for placing (inserting) the signaling information in the appropriate time slot and frames. The T7230A generates a signaling multiframe in the transmit and receive direction to facilitate the access of signaling information at the system interface.

Microprocessor Control Registers

The information written into the F and G bits of the transmit signaling control registers define the robbed-bit signaling mode for each channel for both the transmit and receive directions (TSIG = 0) in the T1 framing formats. The per-channel programming allows the system to mix voice channels with data channels within the same frame. Note that a receive-channel robbed-bit signaling mode is defined by the state of the F and G bits in the transmit signaling control registers for that channel.

The microprocessor transmit signaling registers may be used in the associated signaling mode. In this mode (TSR-ASM mode), the system writes into the F and G bits[1] of the transmit signaling registers to program the robbed-bit signaling state mode of each transmit and received DS0. This mode is enabled by programming PR10, bit 5 to 1 in any DS1 mode.

In the common channel signaling mode, data written in the transmit signaling registers is transmitted in channel 24 of the transmit line bit stream. The F and G bits are ignored in this mode. The received signaling data from channel 24 in T1 format or channel 16 in CEPT format, is stored in the receive signaling registers (RS0—RS23 for T1; RS0—RS16 for CEPT).

1. All other bits in the signaling registers are ignored, while the F and G bits in the received DR stream are ignored.

Signaling Access (continued)

Associated Signaling Mode

Signaling information in the associated signaling mode (ASM) is allocated an 8-bit system time slot in conjunction with the data information for a particular channel. The system data rate in the ASM mode is 4.096 Mbits/s. Each system channel consists of an 8-bit payload time slot followed by its associated 8-bit signaling time slot. The format of the signaling byte is identical to the signaling registers. In the default ASM mode, writing the transmit signaling registers will corrupt the transmit signaling data. In the TSR-ASM mode, the system must write into the F and G bits[1] of the transmit signaling registers to program the robbed-bit signaling state mode of each DS0.

In the TSR-ASM mode, the system writes into the F and G bits[1] of the transmit signaling registers to program the robbed-bit signaling state mode of each transmit and received DS0. This mode is enabled by programming PR10, bit 5 to 1 in any DS1 mode. The F and G bits in the system data are ignored.

The received signaling data can be obtained from both the system interface and the receive signaling registers. The associated signaling mode is valid for both the T1 and CEPT framing formats. Table 22 illustrates the ASM time slot format for valid channels.

Table 22. Associated Signaling Mode CHI 2-Byte Time-Slot Format

ASM CHI Time Slot															
PAYLOAD DATA								SIGNALING INFORMATION							
1	2	3	4	5	6	7	8	A	B	C	D	E*	F†	G†	P‡

* In the CEPT IRSM format, this bit position contains the per-channel E0-31 control information. In all other formats this bit is ignored.
† In the DS1-TSR-ASM mode and CEPT frame formats, these bits are ignored.
‡ The P bit is the parity-sense bit calculated over the 8 data bits, the ABCD (and E bits), and the P bit. The identical sense of the received system P bit in the transmitted signaling data is echoed back to the system in the received signalling information.

The T1 framing formats require rate adaption from the line-interface 1.544 Mbits/s bit stream to the system-interface 4.096 Mbit/s bit stream. The rate adaption results in the need for stuffed time slots on the system interface. Table 23 illustrates the ASM format for T1 stuffed channels used by the T7230A. The stuffed data byte contains the programmable idle code (default = FEhex), while the signaling byte is ignored.

Table 23. Associated Signaling Mode CHI 2-Byte Time-Slot Format for Stuffed Channels

ASM CHI Time Slot															
PAYLOAD DATA								SIGNALING INFORMATION							
1	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X

1. All other bits in the signaling registers are ignored, while the F and G bits in the received DR stream are ignored.

Alarms and Performance Monitoring

The T7230A receive framer monitors the receive line data for alarm conditions and error events and presents this information to the system through the microprocessor interface status registers. The transmit framer, to a lesser degree, monitors the receive system data and presents the information to the system through the microprocessor interface status registers. The updating of the status registers is controlled by the receive line clock signal. When the T7230A determines that the RLCK signal is lost, the updating of all status information is clocked by the internal system clock derived from the CHI CLKXR signal.

Although the precise method of detecting or generating alarm and error signals differs between framing modes, the functions are essentially the same. The alarm conditions monitored on the received line interface are:

1. **Loss of frame alignment.** The loss of frame alignment (LFA) indicates that the receive frame alignment for the line has been lost and the data cannot be properly extracted. The LFA for the various framing formats as defined in Table 24.

Table 24. Loss of Frame Alignment Alarm Conditions

Framing Format	Activation Criteria
Superframe: D4	Two incorrect received framing bits out of four (or six).
Superframe: *SLC*-96	Two incorrect received FT framing bits out of four.
Superframe: DDS	Four incorrect received framing bits out of 12.
Extended Superframe (ESF)	Two incorrect received FE framing bits out of four (or six).
CEPT	Three consecutive incorrect FAS patterns or three consecutive incorrect NOT FAS patterns or more than 914 received CRC-4 checksum errors.

2. **Yellow alarm** or the **remote frame alarm.** The T7230A detects an incoming remote frame alarm (commonly referred to as a yellow alarm) as for the different framing formats is shown in Table 25.

Table 25. Remote Frame Alarm Conditions

Framing Format	Activation Criteria
Superframe: D4	Bit 2 of all time slots in the 0 state.
Superframe: D4-Japanese	The twelfth framing bit in the 1 state.
Superframe: DDS	Bit 6 of time slot 24 in the 0 state.
Extended Superframe (ESF)	An alternating pattern of eight 1s followed by eight 0s.
CEPT: Basic Frame	Bit 3 of the NOT FAS frame in the 1 state.
CEPT: Signaling Multiframe	Bit 6 of the time slot 16 signaling frame 0.

Alarms and Performance Monitoring (continued)

3. **Alarm Indication Signal** (AIS). The T7230A's receive framer detects an incoming alarm indication signal as defined in Table 26.

Table 26. Alarm Indication Signal Conditions

Framing Format	Activation Criteria
T1	The incoming signal has two or fewer zeros in each of two consecutive double-frame periods (386 bits). AIS is cleared if each of two consecutive double-frame periods contains three or more zeros.
CEPT ETSI	As described in Draft prETS 300 233:1992 section 8.2.2.4, loss of frame alignment occurs and the reception of 512 bit periods containing two or less binary 0s.
CEPT ITU	As described in ITU Rec. G.775, the incoming signal has two or fewer zeros in each of two consecutive double-frame periods (512 bits). AIS is cleared if each of two consecutive double-frame periods contains three.

4. The slip condition is defined as the state in which the receive framer write address pointer and the transmit concentration highway interface read address pointer (to the elastic store buffer) are within an invalid range[1].
   A. The negative slip (slip-O) alarm indicates the receive line clock (RLCK) — system clock (CLKXR) monitoring circuit detects a state of overflow caused by the frequency of RLCK being greater than the frequency of CLKXR. One system frame is deleted.
   B. The positive slip (slip-U) alarm indicates the line clock (RLCK) — system clock (CLKXR) monitoring circuit detects a state of underflow caused by the frequency of CLKXR being greater than frequency of RLCK. One system frame is repeated.
5. The **loss of receive clock** (LORLCK) alarm is asserted when an interval of 250 µs has expired with no transition of RLCK detected. The alarm is disabled on the first transition of RLCK. The T7230A's receive framer cannot extract the receive clock from the pulses it receives from the receive line interface but depend on the receive line interface to provide a valid receive line clock signal on RLCK. In the loss of receive clock state, the status registers will be clocked by a 2 MHz internal clock signal derived from the CLKXR input signal.
6. The **loss of transmit clock** (LOXLCK) alarm is asserted when an interval of 250 µs has expired with no transition of PLLCK is detected[2]. The alarm is disabled on the first transition of PLLCK.

1. The invalid pointer range is 1 to 3 byte for DS1 and 6 bytes for CEPT.
2. There is no transmission of line data while LOXLCK = 1.

Alarms and Performance Monitoring (continued)

7. The **continuous E-bit** alarm (CON-E) is asserted when the receive framer detects:
   - A. Five consecutive seconds where each 1 second interval contains ≥991 received E bits = 0 events.
   - B. Simultaneously no LFA occurred.
   - C. No A bit = 1 was received.
   - D. Neither Sa6_Fhex nor Sa6_Ehex codes were detected.

   The five second timer is started when:

   - E. CRC-4 multiframe alignment is achieved.
   - F. A = 0 is detected.
   - G. Neither Sa6_Fhex nor Sa6_Ehex is detected.

   The five second counter is restarted when:
   - H. LFA occurs, or
   - I. ≤990 E bit = 0 events occurred in 1 second, or
   - J. An A bit = 1, is detected, or
   - K. A valid Sa6_Fhex or Sa6_Ehex code was detected.

   This alarm is disabled when:

   - L. LFA occurs.
   - M. or ≤990 E bit = 0 events occurred in 1 second, or
   - N. An A bit = 1 is detected, or
   - O. The Sa6_Fhex or Sa6_Ehex code was detected.

8. **Failed state** alarm or the **unavailable state alarm.**
   - A. The default mode asserts this alarm bit upon detection of ten consecutive severely errored second events and deasserts this alarm bit upon detection of ten consecutive seconds that were not severely errored. The corresponding performance counters are incremented appropriately.
   - B. Optionally, the T7230A can be programmed to process the unavailable state at the onset of the unavailable state (at the beginning of the ten consecutive severely error interval), and inhibit the increment of the severely errored and errored seconds counters for the duration of the unavailable state. In this mode, the contents of the performance counters contains information delayed by ten seconds.

Alarms and Performance Monitoring (continued)

9. The **4-bit Sa6 codes** (Sa6_hex) are asserted if three consecutive 4-bit patterns have been detected. The alarms are disabled when three consecutive 4-bit Sa6 codes have been detected that are different from the pattern previously detected. The receive framer monitors the Sa6 bits for ten special codes described in ETS Draft prETS 300 233:1992 Section 9.2. The Sa6 codes are defined in Table 27 and Table 28. The Sa6 codes in Table 27 may be recognized as an asynchronous bit stream in either non-CRC-4 or CRC-4 modes; the receive framer must be in the basic frame alignment state. In the CRC-4 mode, the receive framer may be forced to recognize the received Sa6 codes in Table 27 synchronously to the CRC-4 submultiframe structure; the receive framer must be in the CRC-4 multiframe alignment state. The Sa6 codes in Table 28 are only recognized synchronously to the CRC-4 submultiframe and when the receive framer is in CRC-4 multiframe alignment. The detection of three consecutive 4-bit patterns are required to indicate a valid received Sa6 code. In the receive Sa6 status register, multiple Sa6 bit positions may be set. However, one and only one Sa6 bit position can remain set after the initial read to this register. Once set, any three-nibble (12-bit) interval that contains any other Sa6 code will clear the current Sa6 code setting. Interrupts may be generated by the six 4-bit Sa6 codes given in Table 27 and Table 28.

Table 27. Sa6 Bit Coding Recognized by the T7230A Receive Framer

Code	First Receive Bit (MSB)			Last Received Bit (LSB)
Sa6_8hex	1	0	0	0
Sa6_Ahex	1	0	1	0
Sa6_Chex	1	1	0	0
Sa6_Ehex	1	1	1	0
Sa6_Fhex	1	1	1	1
Sa6_Xhex	All other bit combinations.			

Table 28 defines the three 4-bit Sa6 codes that are always detected synchronously to the CRC-4 submultiframe structure, and are only used for counting NT1 events.

Table 28. Sa6 Bit Coding of NT1 Interface Events Recognized by the T7230A Receive Framer

Code	First Receive Bit (MSB)			Last Received Bit (LSB)	Event at NT1
Sa6_1hex	0	0	0	1	E = 0
Sa6_2hex	0	0	1	0	CRC-Error
Sa6_3hex	0	0	1	1	CRC-Error & E = 0

Alarms and Performance Monitoring (continued)

The reference points for receive CRC-4, E-bit, and Sa6 decoding are illustrated in Figure 13.

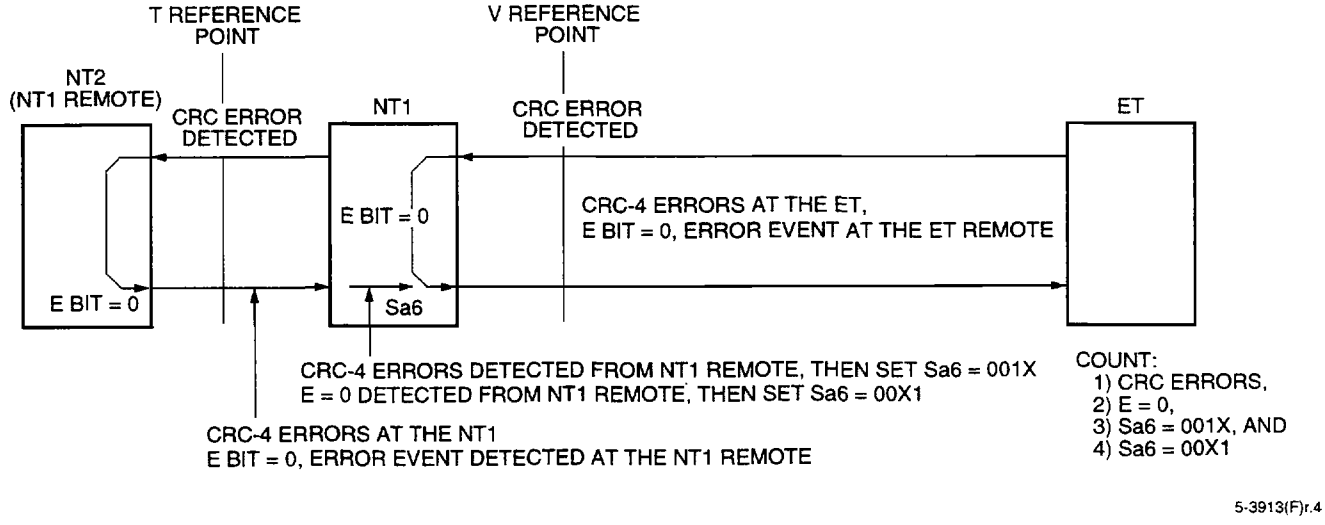


Figure 13. The T and V Reference Points for a Typical CEPT E1 Application

Alarms and Performance Monitoring (continued)

The error events monitored by the T7230A are as follows:

Table 29. The T7230A Event Counters Definition

Error Event	T7230A Mode	Definition	Counter Size (bits)
Bipolar Violations (BPVs)	AMI	Any bipolar violation	16
	B8ZS or HDB3	Any nonvalid BPV	
	CEPT HDB3	Any 4-bit interval with no 1 pulse	
Frame Alignment Errors (FERs)	SF: D4	Any FT or FS bit error	8
	SF: *SLC*-96	Any FT bit error	
	SF: DDS	Any FT, FS or time slot 24 FAS bit error	
	ESF	Any FE bit error	
	CEPT	Any FAS (0011011) or NOT FAS (bit 2) bit error	
CRC Checksum Errors	ESF or CEPT with CRC	Any received checksum in error	16
Excessive CRC Errors	ESF	32 consecutive checksum errors	NONE
	CEPT with CRC	Greater than 914 CRC-4 checksum errors in a one second interval	
Error Events	All	Any loss of frame alignment event or slip	16
	ESF or CEPT with CRC	Any incorrect receive CRC checksum	
Error Second Events	All	Any loss of frame alignment event or slip event within a one second interval	16
	ESF or CEPT with CRC	Any incorrect receive CRC checksum within a one second interval	
Bursty Error Second Events	ESF	Greater than 1 but less than 320 CRC-6 checksum errors within a one second period	16
	CEPT with CRC	Greater than 1 but less than 915 CRC-4 checksum errors within a one second period	
	CEPT with no CRC	Greater than 1 but less than 16 FAS or NOT FAS bit errors within a one second period	
Severely Error Second Events	All	Loss of frame alignment or slip within a one second period	16
	SF	8 or more framing bit errors within a one second period	
	ESF	320 or more CRC-6 checksum errors within a one second period	
	CEPT with CRC	915 or more CRC-4 checksum errors within a one second period	
	CEPT with no CRC	16 or more FAS or NOT FAS bit errors within a one second period	
Unavailable Second Events	All	A one second period in the unavailable state	16

A receive framer enters an unavailable state condition whenever it has detected ten consecutive seconds each being severely errored. When in the unavailable state, the receive framer resumes an available state condition whenever ten consecutive seconds have been detected, none of which were severely errored.

Alarms and Performance Monitoring (continued)

Loopback and Transmission Modes

There are three primary loopback and transmission test modes supported by T7230A:

1. System loopback (SLB)
2. Line loopback (LLB)
3. Payload loopback (PLLB)

In detail:

1. The SLB mode loops the receive system data back to the system after:
   A. The transmit framer processes the data.
   B. The receive framer processes the data.

   In this mode, AIS be transmitted to the line interface.
2. The LLB mode loops the receive line data back to the transmit line without removing bipolar violations. The receive data is processed by the receive framer and transmitted to the system interface.
3. The PLLB mode loops the receive line data back to the transmit line after the bipolar violations are removed and substitutes all receive framing data with the transmit framing data.

Figure 14 illustrates the various loopback modes.

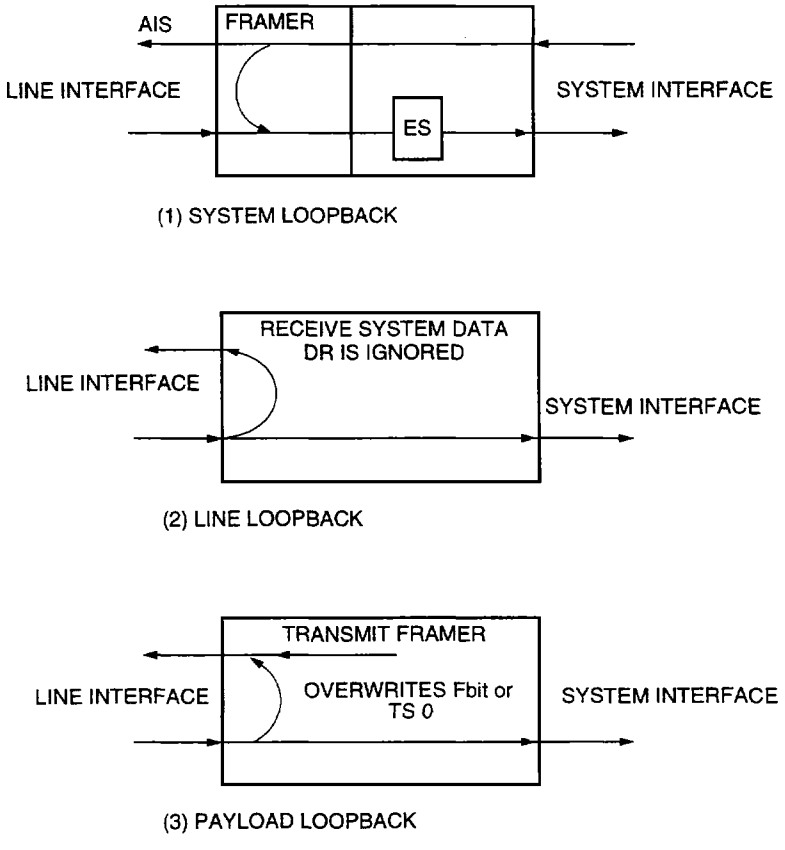


Figure 14. T7230A's Loopback and Test Transmission Modes

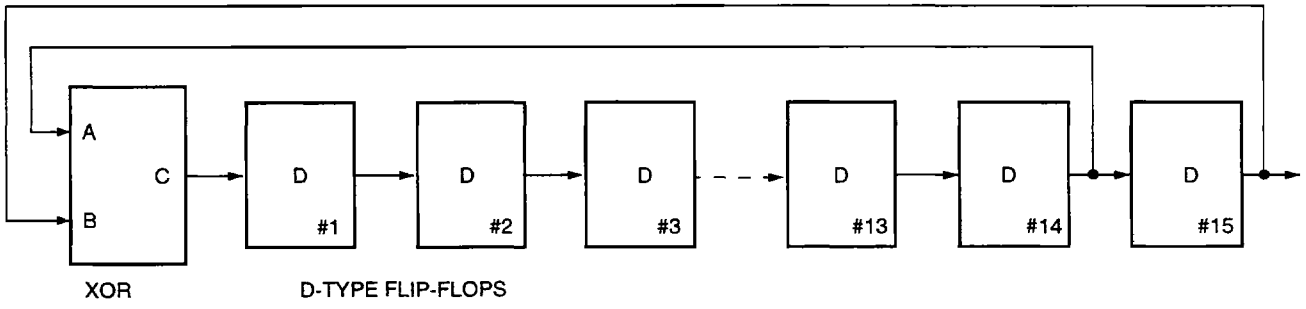
Alarms and Performance Monitoring *(continued)*

Transmit Line Test Patterns

The transmit framer can be programmed to transmit various test patterns. These test patterns, when enabled, overwrite the receive CHI data. The test pattern is:

1. The unframed-AIS pattern consists of a continuous bit stream of 1s (. . . 111111 . . .).
2. The unframed-auxiliary pattern consists of a continuous bit stream of alternating 1s and 0s (. . . 10101010).
3. The framed-AIS (high-density) test pattern consists of:
   A. A continuous 1 pattern in time slots.
   B. Valid framing bits.
   C. CRC bits resulting from the pattern.
4. The framed walking-one (low-density) test signal consists of (T1 only):
   A. A repeating one-in-eight (00000001) pattern resulting in a walking-one pattern after the F bit is inserted.
   B. Valid framing bits inserting into the pattern.
   C. Valid transmit facility data link (XFDL) bit information (ESF).
   D. CRC-6 bits that result from the above pattern in the payload bits (if ESF enabled).
5. The quasi-random test signal consists of:
   A. A pattern produced by means of a 20-stage shift register with feedback taken from the 17th and 20th stages via an exclusive OR gate to the first stage. The output is taken from the 20th stage and is forced to a 1 state whenever the next 14 stages (19 through 6) are all 0. The pattern length is 1,048,575 or $2^{20} - 1$ bits. This signal is described in detail in AT&T Technical Reference 62411 [5] Appendix.
   B. Valid framing bits.
   C. Valid transmit facility data link (XFDL) bit information (ESF).
6. The pseudorandom test pattern consists of:
   A. A $2^{15} - 1$ pattern inserted in the entire payload (time slots 1—31), as described by ITU Rec. 0.151 and illustrated in Figure 15.
   B. Valid FAS and NOT FAS* time slots.
   C. Valid CRC-4 bits.
7. The idle code test pattern consists of:
   A. The programmable idle code in time slots 1—31.
   B. Valid FAS and NOT FAS* time slots.
   C. Valid CRC bits.

*The transmit Si, E, A, and Sa4 through Sa8 bits are transmitted as defined in the control registers.



A	B	C
0	0	0
1	0	1
1	1	0
0	1	1

TRUTH TABLE FOR THE XOR GATE

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Figure 15. 15-Stage Shift Register Used to Generate the Pseudorandom Signal

Alarms and Performance Monitoring (continued)

Automatic and On-Demand Commands

Various signals and test patterns can be transmitted automatically as a result of various alarm conditions or by demand. After reset, all automatic transmissions are disabled. The user can enable the automatic or on-demand actions by setting the proper bits in the automatic and on-demand action register. Table 30 shows the programmable automatically transmitted signals and the triggering mechanisms for each. Table 31 shows on-demand transmit alarm signals and test modes. For a more detailed description, see bit descriptions for the automatic and on-demand action registers.

Table 30. T7230A Automatic Enable Commands

Action	Symbol	Trigger
Transmit Remote Frame Alarm	AXRFA	Defined by enable register.
Transmit E Bit	AXEBIT	Defined by enable register.
Transmit AIS to System	AXAISS	LFA.
Transmit Remote Multiframe Alarm	AXRMFA	LMFA (CEPT).
Transmit AIS in Time Slot 16 to System	AXTS16AISS	LMFA (CEPT).
Automatic Enable of LLB-on and LLB-off	ALLBEN	LLB on-code and off-code.
Automatic Receive Signaling Inhibit	ARSI	LMFA, FERs, or SLIPs.

Alarms and Performance Monitoring (continued)

Automatic and On-Demand Commands (continued)

Table 31. T7230A On-Demand Commands

Type	Symbol	Mode	Action
Transmit Remote Frame Alarm	DXRFA	SF: DDS	Bit 6 = 0 in time slot 24.
		SF: D4	Bit 2 = 0 of all time slots.
		SF: D4-Japanese	F bit 12 = 1.
		ESF	Alternating eight 1s followed by eight 0s in the FDL F-bit position.
		CEPT	Transmit A bit = 1 to line.
Transmit Remote Multiframe Alarm	DXRMFA	CEPT	Frame 0, bit 6 = 1 of the time slot 16 multiframe.
Transmit Data Link Squelch	XDLSQ	All except SF: *SLC-96*	Transmit XDL = 1.
Transmit Signals	DXSG[3:0]	All	Transmit test patterns to line.
Transmit Channel Squelch	DXCHSQ	SF: DDS	Squelch the transmit line channels with the UC code.
		Non-DDS	Squelch the transmit line channels with the idle code.
Transmit System Channel Squelch	DRCHSQ	SF: DDS	Squelch the receive channels with the MOS code.
		Non-DDS	Squelch the receive channels with the idle code.
Transmit System Signaling Channel Squelch	DRSCHSQ	CEPT	Squelch the time slot 16 receive channels with the AIS code.
Receive Signaling Inhibit	DRSI	All	Suspend the updating of the receive signaling registers.
Receive Framer Reframe	DRRFRM	All	Force reframe.
Loopback Control	DLB[1:0]	—	Enable loopback modes.
Loopback control Codes	DXLLB[2:1]	T1	Transmit LLB turn-on (framed 001) and turn-off (framed 0001) codes.
		CEPT	Transmit LLB turn-on (Sa6 = 1000) and turn-off (Sa6 = 1010) codes.

Note: If simultaneous remote alarm and squelch patterns affect the same bit, remote alarm takes precedence.

Concentration Highway Interface (CHI)

T7230A uses a dual, high-speed, serial interface known as the CHI on the system side. This interface is a very flexible, high-speed bus. Configured via the highway control registers (PR13—PR31), this interface can be set up in a number of different configurations.

The following is a list of the CHI features:

1. AT&T standard interface for communication devices.
2. Two pairs of transmit and receive paths to carry data in 8-bit time slots.
3. Programmable definition of highways through offset and clock-edge options (independent for transmit and receive directions).
4. Programmable activation of each receive time slot.
5. Programmable 3-state of each transmit time slot.
6. An 8 kHz framing signal to synchronize each direction of data flow.
7. A device generated, receive line clock derived, 8 kHz frame synchronization signal.
8. Compatible with *Mitel*[1] and *AMD*[2] PCM highways.
9. Compatible with the GCI specification.

The concentration highway interface consists of the following signals:

1. CLKXR = User-supplied clock signal.
2. FS = CHI frame synchronization (FS) signal (8 kHz). All system receive and transmit time slots are referenced from the FS signal.
3. OFS = T7230A generated CHI frame synchronization (OFS) signal (8 kHz); this output is enabled by programming the CHIMM to 1.
4. DRA, DRB = Receive CHI data from the system.
5. DXA, DXB = Transmit CHI data to the system.
6. $\overline{\text{TSCA}}$, $\overline{\text{TSCB}}$ = Time-slot control signals (can be used to enable optional external buffers to drive the DXA or DXB output lines).

Rate adaptation is required for all DS1 formats between the 1.544 Mbits/s line rate and 2.048 Mbits/s (or 4.096 Mbits/s) CHI rate. This is achieved by means of stuffing eight idle time slots[3] into the existing 24 time slots of the T1 frame. Idle time slots are transmitted every fourth time slot (starting in the first, second, third, or fourth time slot) or grouped together at the end of the CHI frame (default setting). The positioning of the idle time slots is the same for transmit and receive directions. Idle time slots contain a programmable code. Idle or unused time slots can be disabled (the DX interface is forced to a high-impedance state for the interval of the unused time slot).

Supported also is an associated signaling mode in which the CHI carries data and its associated signaling information within a 16-bit time slot.

1. *Mitel* is a registered trademark of Mitel Corporation.
2. *AMD* is a registered trademark of Advanced Micro Devices, Inc.
3. These stuffed time slots are ignored on the received CHI and are forced to a high-impedance state in the transmit CHI.

Concentration Highway Interface (CHI) (continued)

CHI Parameters

The eight parameters that define the receive and transmit CHI timing relative to the frame strobe (FS) are given in Table 32.

Table 32. Summary of the Concentration Highway Interface Parameters for the T7230A

Name	Description
FE	**Frame Edge.** FE = 0 (1); FS is sampled on the falling (rising) edge of CLKXR. FE is used in both the receive and transmit directions. In CHIMM (CHI master mode), pin 50 (OFS) outputs a transmit frame strobe to provide synchronization for the DXA and DXB. When FE = 1 (or 0), OFS is centered around rising (or falling) edge of CLKXR. In this mode, FS is used for receive data on CHI and OFS is used for transmit data on CHI. (OFS must be physically connected to FS if OFS is the source of the frame sync signal for the DRA, DRB interface.) The timing for OFS in CHIMM = 1 mode is identical to the timing for FS in CHIMM = 0 mode.
Clock Select Mode (CMS)	**Clock Select Mode.** When CMS = 0, the concentration highway clock (CLKXR) and data (DRA, DRB, DXA, or DXB) have the same rate. When CMS = 1, the concentration highway clock (CLKXR) is twice the rate of CHI data.
XCE	**Transmitter Clock Edge.** XCE = 0 (1), DX is clocked on the falling (rising) edge of CLKXR.
RCE	**Receiver Clock Edge.** RCE = 0 (1), DR is latched on the falling (rising) edge of CLKXR.
XOFF2—XOFF0	**Transmitter Bit Offset.** Three-bit binary offset, relative to FS, for the first bit of the transmit time slot. For CMS = 1, the offset is twice the number of CLKXR clock periods by which transmission of the first bit is delayed. For CMS = 0, the offset is the number of CLKXR cycles by which the first bit is delayed.
ROFF2—ROFF0	**Receiver Bit Offset.** Three-bit binary offset, relative to the FS, for the first bit of the receive time slot. For CMS = 1, the offset is twice the number of CLKXR clock periods by which the first bit is delayed. For CMS = 0, the offset is the number of CLKXR cycles by which the first bit is delayed.
XBYOFF5—XBYOFF0	**Transmitter Byte Offset.** Six-bit binary byte-offset from the framing strobe (FS) to the beginning of the next frame on the transmit highway. Note that in the ASM mode, a frame consists of 64 bytes; whereas in other modes, a frame contains 32 bytes. In the 2.048 Mbits/s mode, the allowable offsets are 0—31 bytes. In both the 4.096 Mbits/s modes, the allowable offsets are 0—63 bytes.
RBYOFF5—RBYOFF0	**Receiver Byte Offset.** Six-bit binary byte-offset from FS to the beginning of the receive CHI frame. Note that in the ASM mode, a frame consists of 64 bytes; whereas in other modes, a frame contains 32 bytes. In the 2.048 Mbits/s mode, the allowable offsets are 0—31 bytes. In both the 4.096 Mbits/s modes, the allowable offsets are 0—63 bytes.

Concentration Highway Interface (CHI) (continued)

CHI Offset Programming

To facilitate bit offset programming, two additional parameters are introduced: CEX is defined as the clock edge with which bit 7 of time slot 1 is transmitted; CER is defined as the clock edge on which bit 0 of time slot 0 is latched. CEX and CER are counted relative to the edge on which the FS signal is sampled. Values of CEX and CER depend upon the values of the eight parameters described above.

The following three tables give values of CEX and CER for various values of CMS, FE, XCE, and RCE, XOFF[2:0], and ROFF[2:0]. The byte (time slot) offsets are assumed to be zero in the following examples.

Table 33. Programming Values for XOFF[2:0] and ROFF[2:0] when CMS = 0

FE	RCE/ XCE	ROFF[2:0] or XOFF[2:0]								
		000	001	010	011	100	101	110	111	
0	0	4	6	8	10	12	14	16	18	CER or CEX
0	1	3	5	6	9	11	13	15	17	
1	0	3	5	6	9	11	13	15	17	
1	1	4	6	8	10	12	14	16	18	

Table 34. Programming Values for XOFF[2:0] when CMS = 1

FE	XCE	XOFF[2:0]								
		000	001	010	011	100	101	110	111	—
0	0	4	8	12	16	20	24	28	32	—
0	1	3	7	11	15	19	23	27	31	CEX
1	0	3	7	11	15	19	23	27	31	—
1	1	4	8	12	16	20	24	28	32	—

Table 35. Programming Values for ROFF[2:0] when CMS = 1

FE	RCE	ROFF[2:0]								
		000	001	010	011	100	101	110	111	—
0	0	6	10	14	18	22	26	30	34	—
0	1	7	11	15	19	23	27	31	35	CER
1	0	7	11	15	19	23	27	31	35	—
1	1	6	10	14	18	22	26	30	34	—

Concentration Highway Interface (CHI) (continued)

CHI Offset Programming (continued)

Figure 16 shows an example of the relative timing of CHI 2.048 Mbits/s data with the following parameters:

1. CMS = 0, FE = 0.
2. XCE = 1, XOFF[2:0] = 000, XBYOFF[5:0] = 000000, XLBIT = 1,
3. RCE = 0 , ROFF[2:0] = 000, RBYOFF[5:0] = 000000, RLBIT = 1.

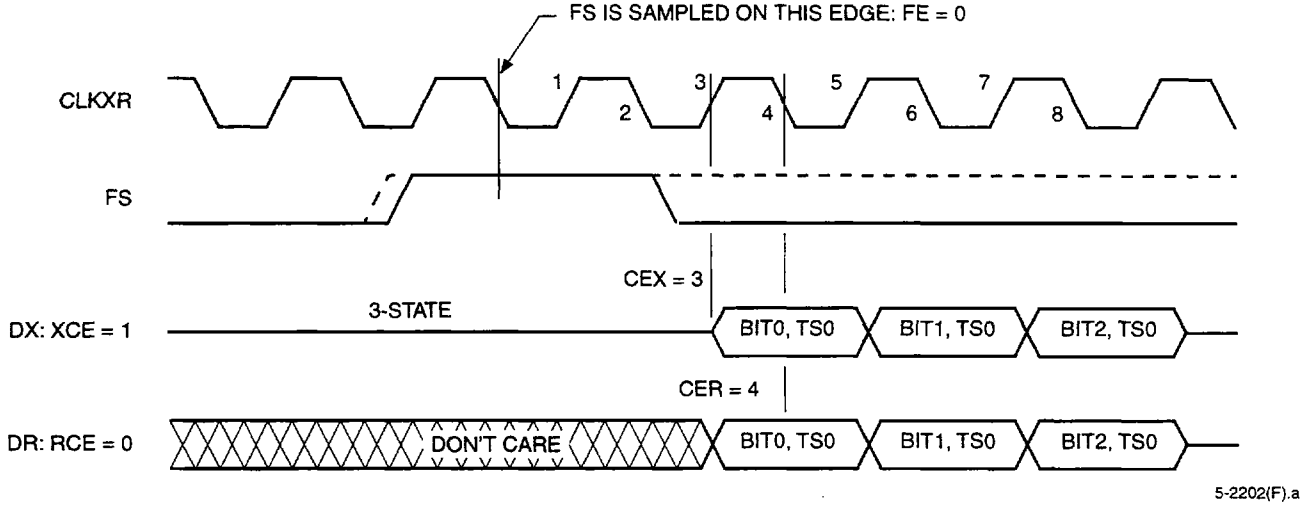


Figure 16. CHI DX and DR to CLKXR Relationship with CMS = 0 (CEX = 3 and CER = 4, Respectively)

Figure 17 shows an example of the relative timing of CHI 2.048 Mbits/s data with the following parameters:

1. CMS =1, FE = 0.
2. XCE = 1, XOFF[2:0] = 000, XBYOFF[5:0] = 000000, XLBIT = 1,
3. RCE = 0 , ROFF[2:0] = 000, RBYOFF[5:0] = 000000, RLBIT = 1.

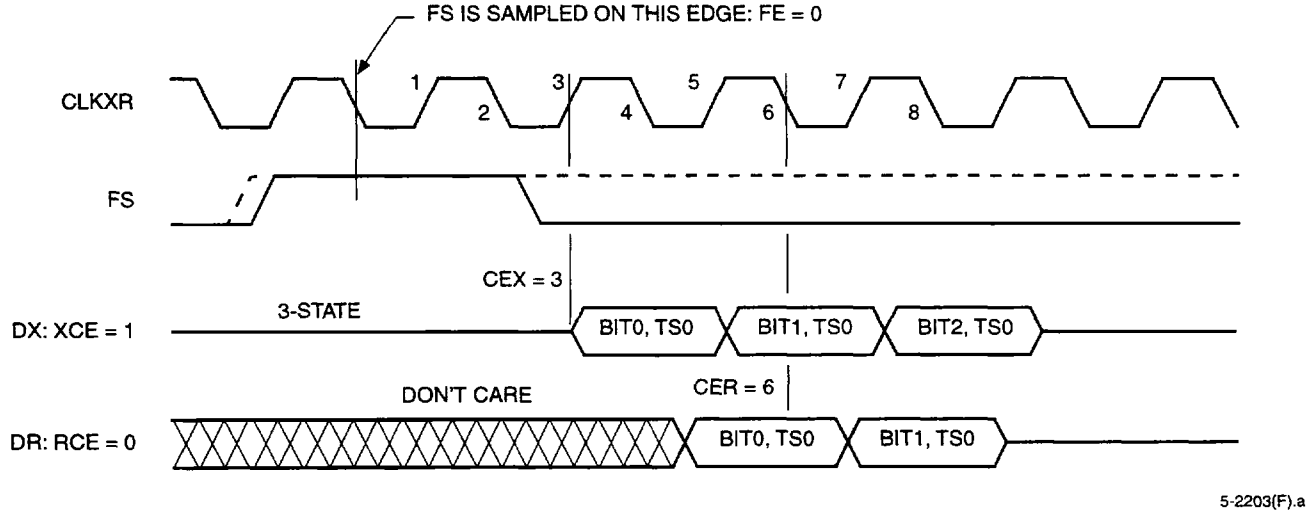


Figure 17. CHI DX and DR to CLKXR Relationship with CMS = 1 (CEX = 3 and CER = 6, Respectively)

Phase-Lock Loop Circuit

The block diagram of the T7230A phase detector circuitry is shown in Figure 18. The T7230A uses elastic store buffers (two frames) to accommodate the transfer of data from the system interface clock rate of 2.048 Mbits/s to the line interface clock rate of either 1.544 Mbits/s or 2.048 Mbits/s.The transmit line side of the T7230A does not have any mechanism to monitor data overruns or underruns (slips) in its elastic store buffer. This interface relies on the requirement that the PLLCK clock signal (variable) is phase-locked to the CLKXR clock signal (reference). When this requirement is not met, uncontrolled slips may occur in the transmit elastic store buffer that would result in corrupted data and no indication will be given. Typically, a variable clock oscillator (VCXO) is used to drive the PLLCK signal. The T7230A provides a phase error signal (EPLL) that can be used to control the VCXO. The EPLL signal is generated by monitoring the divided-down PLLCK (DPLLCK) and CLKXR (DCLKXR) signals and using the DCLKXR signal as a reference to determine the phase difference between DLKCXR and DPLLCK. While DCLKXR and DPLLCK are phase-locked, the EPLL signal is in a high-impedance state. If the T7230A determines that the VCXO needs adjusting, EPLL is driven to either 5 V or 0 V. An RC circuit (typically, R = 1 kΩ and C = 0.1 μF) is used to filter the EPPL signal for the VCXO.

The receive line elastic store buffer contains circuitry that monitors the read and write pointers for potential data overruns and underruns (slips) conditions. Whenever this slip circuitry determines that a slip may occur in the receive elastic store buffer, it will adjust the read pointer such that a controlled slip is performed. The controlled slip is implemented by dropping or repeating a complete frame at the frame boundaries. The occurrence of controlled slips in the receive elastic store is indicated in the status registers.

The T7230A can be programmed to use the receive line signal as the reference and the CLKXR signal as the variable signal. This requires RLCK and PLLCK be tied to the RLCK signal and the PLLREF bit in the parameter register to be programmed to 1. In this mode, the T7230A acts as a master timing source and is capable of generating the system frame synchronization signal through the OFS output pin.

Phase-Lock Loop Circuit (continued)

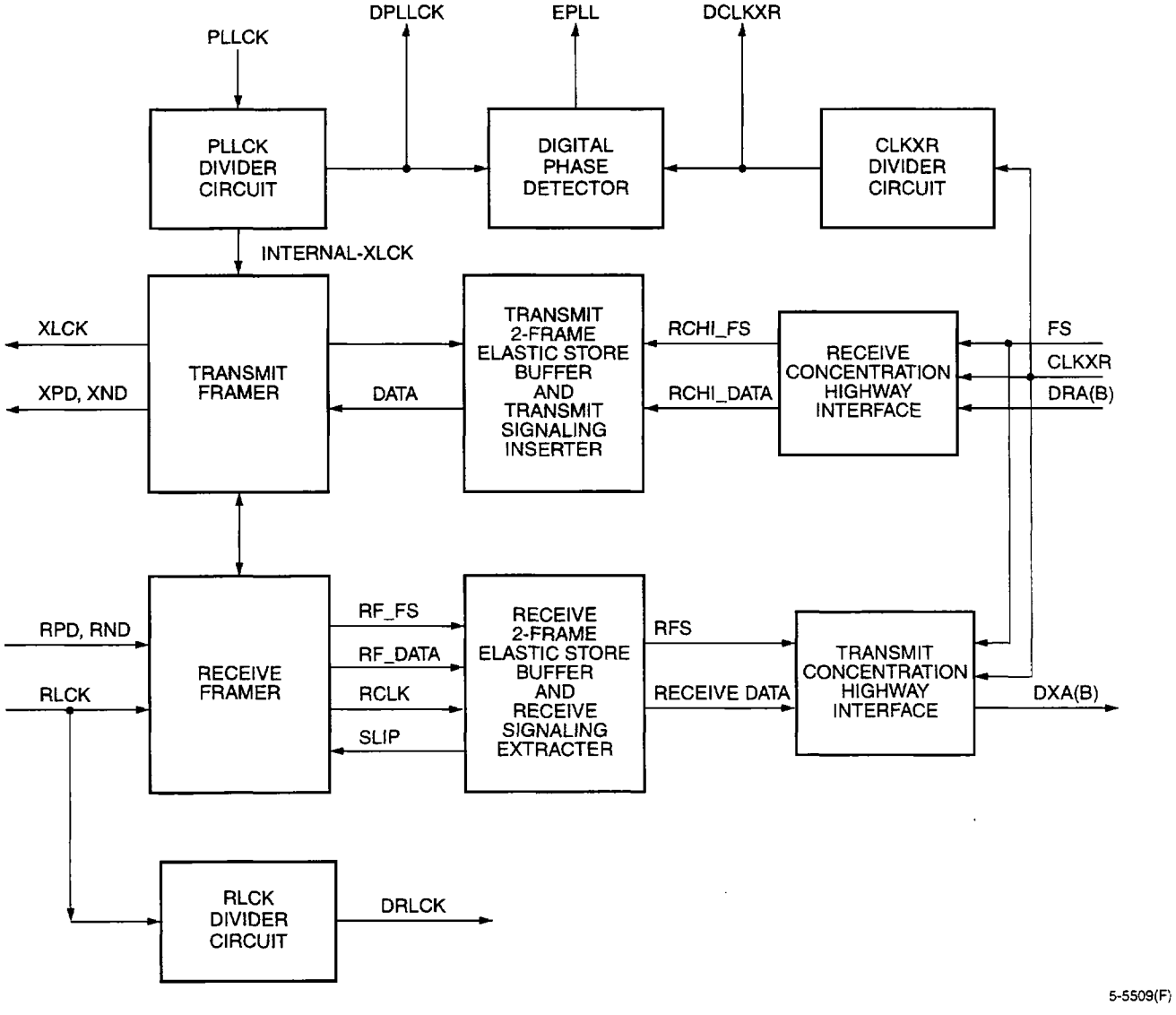


Figure 18. T7230A Phase Detector Circuitry

Microprocessor Interface

T7230A is equipped with an asynchronous microprocessor interface that allows register access through a 7-bit wide address bus that is demultiplexed from a 8-bit wide data bus.

The minimum read and write register access time for the T7230A is specified at 200 ns.

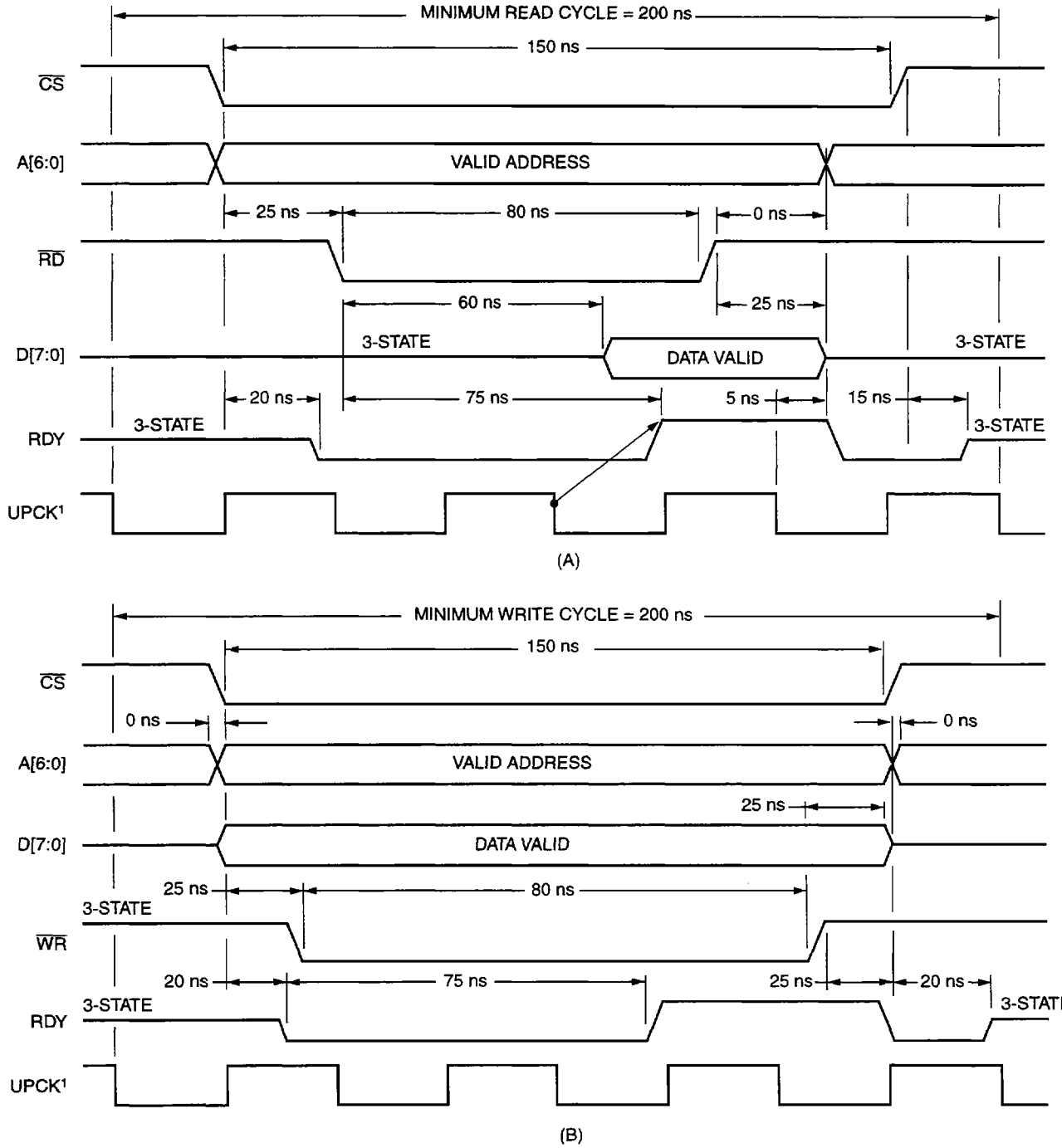
The *Intel* interface mode consists of an chip select ($\overline{CS}$), separate read ($\overline{RD}$) and write ($\overline{WR}$) pins, and a ready pin[1] (RDY). Supplying the appropriate signal to the MPCK input allows the use of the *Intel*-RDY signal to signify the completion of the read or write access. System applications that do not use the *Intel*-RDY output signal should strap the MPCK input to ground (0 V).

The *Motorola* interface mode consists of an address strobe ($\overline{AS}$) pin, a data strobe ($\overline{DS}$) pin, a read/write (R/$\overline{W}$) pin, and data transfer acknowledge[2] ($\overline{DTACK}$) pin. The *Motorola* $\overline{DTACK}$ signal is an asynchronous signal that is a function the $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ signals.

The read-cycle and write-cycle timing for these two modes is illustrated in Figure 19 and Figure 20, respectively.

1. If the setup and hold timing requirements of the $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ signals are met, then the ready signal may be ignored.
2. The $\overline{DTACK}$ signal is asynchronous to the MPCK signal.

Microprocessor Interface (continued)



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1. UPCK is needed only when RDY is desired. Otherwise, UPCK must be strapped to Vss.

Note. The UPCK signal is used to drive the RDY output.

Figure 19. *Intel* Interface Mode Read (A) and Write (B) Cycle Timing

Microprocessor Interface (continued)

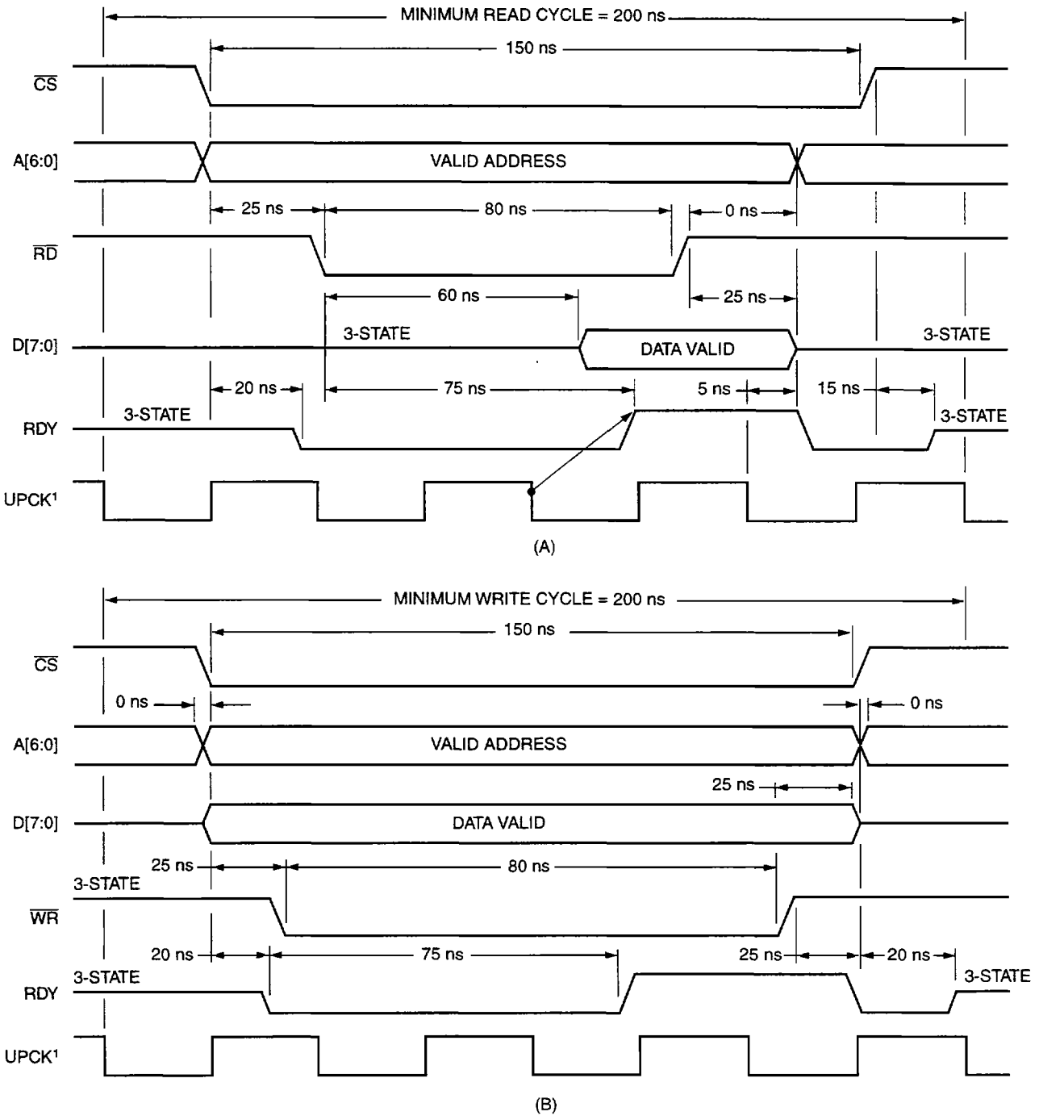


Figure 20. *Motorola* Interface Mode Read (A) and Write (B) Cycle Timing

Register Structure

T7230A registers are structured into six groups:

1. Clear-on-read interrupt generating status registers (SR0—SR5).
2. Cleared-on-read count registers (SR6—SR20).
3. CEPT spare bit registers (SR21—SR22).
4. Parameter registers (PR0—PR31).
5. Receive signaling registers (RSR0—RSR31).
6. Transmit signaling registers (TSR0—TSR31).

Each block of registers is grouped as shown in Table 36.

Table 36. T7230A Status and Control Blocks Address Range

T7230A Register Block	Decimal Address Range
Interrupt Status Registers (COR)	0—5
Status Counters (COR)	6—20
Received CEPT Time Slot 0 and Time Slot 16 Control Bits	21—22
Reserved	23—31
Receive Signaling Registers	32—63
Parameter (Configuration) Registers	64—95
Transmit Signaling Registers	96—127

All status registers are clocked with the framer unit receive line clock.

Status registers SR0, SR3, SR4, and SR5 and all counting registers are cleared on read (COR).

When reading the clear-on-read status registers, only those bits in the 1 state at the time of the read are cleared.

Status registers SR1 and SR2 generate interrupts at the onset of the condition. The condition monitored in these bits are latched and are cleared on read if the condition no longer exists. If the condition is still present at the time of the read, then the bit is cleared by the T7230A when the given condition is no longer observed by the T7230A.

On all 16-bit counter registers both bytes are cleared only after reading both bytes, regardless of the order in which they are read. Once a read is initiated on one of the bytes, the updating of that counter is disabled and remains disabled until both bytes are read. All events during this interval are lost.

The count registers stop at the all ones state. This state may be programmed to generate an interrupt when it is reached.

Register Structure (continued)

Status/Counter Registers

Interrupt Status Register (SR0)

The interrupt pin (INT) goes active when a bit in this register and its associated interrupt enable bit is set.

Table 37. Interrupt Status Register (SR0)

Bits	Description
0	**Facility Alarm Condition Indication (FACI).** A 1 indicates a facility alarm occurred (go read SR1).
1	**Remote Alarm Condition (RAC).** A 1 indicates a remote alarm occurred (go read SR2).
2	**Facility Alarm Event (FAE).** A 1 indicates a facility alarm occurred (go read SR3 and SR4).
3	**PAC Diagnostic Event (PACDE).** A 1 indicates a PAC system event occurred (go read SR5).
4	**Transmit Signaling Superframe Event (TSSFE).** A 1 indicates the transmission of a MOS (or CCS for CEPT) superframe block has been transmitted and the transmit signaling data buffers are ready for new data.
5	**Receive Signaling Superframe Event (RSSFE).** A 1 indicates a MOS (or CCS for CEPT) superframe block has been received and the receive signaling data buffers must be read.
6	**Excessive CRC Error (ECE).** A 1 indicates the receive framer detected an excessive CRC error condition. The ESF threshold is 32 out of 33 errored CRC checksum blocks. The CEPT threshold is 915 out of 1000 errored CRC checksum blocks.
7	**This Bit Is Reserved and Set to 0.**

Register Structure (continued)

Status/Counter Registers (continued)

Facility Alarm Condition Register (SR1)

The bits in the facility alarm condition register (SR1) indicate alarm state of the receive framer section. Interrupts from this register are generated once at the beginning of the alarm condition. If the alarm condition is still present at the time of the read, the bit will remain in the 1 state for the duration of the alarm condition. If the alarm condition is no longer present at the time of the read, then the bit is cleared on read.

Table 38. Facility Alarm Condition (SR1)

Bits	Description
0	**Loss of Frame Alignment (LFA).** A 1 indicates the receive framer is in a loss of frame alignment and is currently searching for a new alignment.
1	**Loss of Signaling Superframe Alignment (LSFA).** A 1 indicates the receive framer is in a loss of signaling multiframe alignment in the DS1 framing formats. A search for a new signaling superframe alignment starts once frame alignment is established. This bit is 0 in the CEPT mode.
2	**Alarm Indication Signal (AIS).** A 1 indicates the receive framer is currently receiving an AIS pattern from its remote line end.
3	**Loss of Frame Alignment Since Last Read (LFALR).** A 1 indicates that the LFA state indicated in bit 0 of this register is the same LFA state from the previous read. The transition from the 0 state to the 1 state in this bit will **not** generate an interrupt.
4	**Loss of Time Slot 0 CRC-4 Multiframe Alignment (LTS0MFA).** A 1 indicates the receive framer is in a loss of time slot 0 CRC-4 multiframe alignment in the CEPT mode. A search for a new CRC-4 multiframe alignment starts once primary basic frame alignment is found. This bit is 0 when receive CRC-4 checking is disabled. This bit is 0 in the DS1 mode.
5	**Loss of Time Slot 16 Signaling Multiframe Alignment (LTS16MFA).** A 1 indicates the receive framer is in a loss of time slot 16 signaling multiframe alignment in the CEPT mode. A search for a new time slot 16 signaling multiframe alignment starts once frame alignment is established. This bit is 0 when the T7230A is programmed for transparent mode (TSIG = 1). This bit is 0 in the DS1 mode.
6	**Unavailable State (UASTATE).** A 1 indicates the receive framer has detected at least ten consecutive severely errored seconds without seeing ten consecutive seconds not errored. Upon detecting the ten consecutive nonseverely errored seconds, the receive framer will clear this bit.
7	**Time Slot 16 Alarm Indication Signal (AIS).** A 1 indicates the receive framer is currently receiving an AIS pattern in time slot 16 from its remote line end. This unframed AIS is detected only in CEPT mode when signaling is enabled.

Register Structure (continued)

Status/Counter Registers (continued)

Remote End Alarm Register (SR2)

A bit set to 1 indicates the receive framer is receiving or has recently received the given alarm. Interrupts from this register are generated once at the onset of the alarm condition. If the alarm is still present at the time of the read, the bit will remain in the 1 state for the duration of the alarm condition. If the alarm condition is no longer present at the time of the read, the bit is cleared on read.

Table 39. Remote End Alarm Condition (SR2)

Bits	Description
0	**Remote Framer Alarm (RFA).** A 1 indicates the receive framer detected a remote frame (yellow) alarm.
1	**RSa6 = 8.** A 1 indicates that the receive framer detected a Sa6 pattern = 1000 (CEPT only).
2	**RSa6 = A.** A 1 indicates that the receive framer detected a Sa6 pattern = 1010 (CEPT only).
3	**Remote Multiframe Alarm (RMFA).** A 1 indicates the receive framer detected a time slot 16 remote frame alarm. This bit is 0 in the CEPT mode.
4	**Remote Japanese Yellow Alarm (RJYA).** A 1 indicates the receive framer detected the Japanese format remote frame alarm. **RSa6 = C.** A 1 indicates that the receive framer detected a Sa6 pattern = 1100 (CEPT only).
5	**RSa6 = E.** A 1 indicates that the receive framer detected a Sa6 pattern = 1110 (CEPT only).
6	**RSa6 = F.** A 1 indicates that the receive framer detected a Sa6 pattern = 1111 (CEPT only).
7	**RSa6 = X.** A 1 indicates that the receive framer detected a Sa6 pattern = anything else (CEPT only).

Register Structure (continued)

Status/Counter Registers (continued)

Facility Errored Event Register (SR3)

A bit set to 1 indicates the receive framer has recently received the given errored event.

Table 40. Facility Errored Event (SR3)

Bits	Description
0	**Line Format Violation (LFV).** A 1 indicates the receive framer detected a line format violation.
1	**Frame-Bit Error (FBE).** A 1 indicates the receive framer detected a frame-bit or frame alignment pattern error.
2	**Change of Frame Alignment (CFA).** A 1 indicates the receive framer established a new alignment that differs from the previous alignment.
3	**Receive Elastic Store Slip: Buffer Overflow (SLIP_O).** A 1 indicates the receive elastic store performed a control slip due to an elastic buffer overflow condition.
4	**Receive Elastic Store Slip: Buffer Underflow (SLIP_U).** A 1 indicates the receive elastic store performed a control slip due to an elastic buffer underflow condition.
5	**CEPT Frame Shift (CFSHT).** A 1 indicates a 1-bit frame shift event on the received framer as required by the Dutch PTT.
6	**Line Loopback On Code Detect (LLBON).** A 1 indicates the receive framer detected the line loopback enable code. This code is defined in the AT&T Technical Reference 62411 as a framed 001 pattern where the frame bit is inserted into the pattern. This bit is 0 in the CEPT mode.
7	**Line Loopback Off Code Detect (LLBOFF).** A 1 indicates the receive framer detected the line loopback disable code. This code is defined in the AT&T Technical Reference 62411 as a framed 00001 pattern where the frame bit is inserted into the pattern. This bit is 0 in the CEPT mode.

Register Structure (continued)

Status/Counter Registers (continued)

Facility Event Register 1 (SR4)

Table 41. Facility Event Register 1 (SR4)

Bits	Description
0	**Errored Second (ES).** A 1 indicates the receive framer detected an errored event within a one second interval.
1	**Bursty Errored Second (BES).** A 1 indicates the receive framer detected a bursty error condition within a one second interval.
2	**Severely Errored Second (SES).** A 1 indicates the receive framer detected a severely errored condition within a one second interval.
3	**CRC Monitor Reset (CRCRST).** A 1 indicates the CRC multiframe alignment in the receive framer has been established. In ESF mode, this event coincides with the establishment of the frame alignment. In CEPT mode, this event will always follow the establishment of the primary basic frame.
4	**Received E bit = 0 (REB0).** A 1 indicates the receive frame detected a E bit = 0 in either frame 13 or 15 of the time slot 0 CRC-4 submultiframe I. This bit is 0 in the DS1 modes.
5	**Received E bit = 0 (REB1).** A 1 indicates the receive frame detected a E bit = 0 in either frame 13 or 15 of the time slot 0 CRC-4 submultiframe II. This bit is 0 in the DS1 modes.
6	**Out of Unavailable State (OUAS).** A 1 indicates the receive framer detected ten consecutive seconds that were not severely errored while in the unavailable state.
7	**Change of Signaling Superframe Alignment (CSFA).** A 1 indicates the receive framer has established the signaling superframe alignment. In the SF modes (D4 and *SLC*-96) and CEPT modes, this alignment is established only after frame alignment is determined. In the ESF mode, this event coincides with the establishment of the frame alignment.

Register Structure (continued)

Status/Counter Registers (continued)

Facility Event Register 2 (SR5)

Table 42. Facility Event Register 2 (SR5)

Bits	Description
0	**Loss of Transmit Superframe Alignment (LTSFA).** A 1 indicates superframe alignment pattern in the facility data link input XFD as defined for *SLC*-96 is errored. Only valid for *SLC*-96 mode. This bit is 0 in all other modes.
1	**Status Counter Overflow (SCO).** A 1 indicates one of the status counters has reached the all ones state.
2	**Loss of Biframe Alignment (LBFA).** A 1 indicates biframe alignment pattern (alternating 1-0 in bit 2 of time slot 0 of each frame) in the receive system data is errored. This alignment pattern is required when transmitting the Si or Sa bits transparently. Transmitted line data on the XPD and XND output will be corrupted while in this state. Only valid in CEPT mode, this bit is forced to 0 while in the double-NOT-FAS mode. This bit is 0 in all other modes or when programmed for double NOTFAS mode.
3	**Biframe Alignment Established (BFA).** A 1 indicates the transmit framer has established a biframe alignment for the transmission of transparent Si and/or Sa bits from the system data. Only valid in CEPT mode. This bit is 0 in all other modes
4	**This Bit Is Reserved and Set to 0.**
5	**Auxiliary Pattern (AUXP).** A 1 indicates that the receive framer has detected a unframed AUXP pattern. If the receive framer is no longer receiving an unframed AUXP, then this bit is cleared on read. The receive the detection of a valid AUXP.
6	**Receive Continuous E Bit = 0 (RCEBIT).** A 1 indicates that the receive framer has detected receive continuous E bit = 0 for at least five seconds.
7	**Receive CRC-4 100 (400) ms Timer Expirer.**

Register Structure (continued)

Status/Counter Registers (continued)

CRC-4 Error Counter Register (SR6—SR7)

CRC errors are not counted during loss of CRC multiframe alignment.

Table 43. CRC Error Counter Register (SR6—SR7)

Byte	Bits	Description
MSByte	7—0	**CRC Error Counter (CEC15—CEC8).**
LSByte	7—0	**CRC Error Counter (CEC7—CEC0.**

Errored Event Counter Register (SR8—SR9) — 16-Bit Counter

Table 44. Errored Event Counter Register (SR8—SR9)

Byte	Bits	Description
MSByte	7—0	**Errored Event Counter (EEC15—EEC8).**
LSByte	7—0	**Errored Event Counter (EEC7—EEC0).**

Errored Seconds Counter Register (SR10—SR11)

Table 45. Errored Seconds Counter Register (SR10—SR11)

Byte	Bits	Description
MSByte	7—0	**Errored Seconds Counter (ESC15—ESC8).**
LSByte	7—0	**Errored Seconds Counter (ESC7—ESC0).**

Bursty Errored Seconds Counter Register (SR12—SR13)

Table 46. Bursty Errored Seconds Counter Register (SR12—SR13)

Byte	Bits	Description
MSByte	7—0	**Bursty Errored Seconds Counter (BESC15—BESC8).**
LSByte	7—0	**Bursty Errored Seconds Counter (BESC7—BESC0).**

Severely Errored Seconds Counter Register (SR14—SR15) — 16-Bit Counter

Table 47. Severely Errored Seconds Counter Register (SR14—SR15)

Byte	Bits	Description
MSB	7—0	**Severely Errored Seconds Counter (SESC15—SESC8).**
LSB	7—0	**Severely Errored Seconds Counter (SESC7—SESC0).**

Register Structure (continued)

Status/Counter Registers (continued)

Unavailable Seconds Counter Register (SR16—SR17) — 16-Bit Counter

Table 48. Unavailable Seconds Counter Register (SR16—SR17)

Byte	Bits	Description
MSB	7—0	**Unavailable Seconds Counter Bits (UASC15—UASC8).**
LSB	7—0	**Unavailable Seconds Counter Bits (UASC7—UASC0).**

Bipolar Violation Counter Register (SR18—SR19)

The 16-bit count of received bipolar violations; when enabled nibbles of no 0s are also counted.

Table 49. Double Bipolar Violation Counter Register (SR18—SR19)

Byte	Bits	Description
MSB	7—0	**BPVs Counter (BPV15—BPV8).**
LSB	7—0	**BPVs Counter (BPV7—BPV0).**

Frame Bit Error Counter Register (SR20)

Frame bit errors are not counted during loss of frame alignment.

Table 50. Framing Bit Error Counter Register (SR20)

Byte	Bits	Description
LSB	7—0	**Frame Bit Error Counter (FBE7—FBE0).**

Received Sa Register (SR21)

This register contains the last valid received Sa bits in the NOT FAS frame time slot 0 while the receive framer was in basic frame alignment. This register is updated every NOT FAS frame.

Table 51. Receive Sa-Bit Register (SR21)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	RSa8	RSa7	RSa6	RSa5	RSa4

Received Si and X Register (SR22)

This register contains the last valid received control bits in CEPT time slot 16 signaling multiframe frame 0 while the receive framer was in signaling multiframe alignment. Also, this register contains the last valid received Si bits in the NOT FAS frame time slot 0 while the receive framer was in basic frame alignment.

Table 52. Receive Si-Bit and X-Bit Register (SR22)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RSi-NOT FAS	RSi-FAS	0	RX2	RX1	RX0

Register Structure (continued)

Status/Counter Registers (continued)

Received Signaling Registers: DS1 Format

Table 53. Received Signaling Registers: DS1 Format (RSR0—RSR23)

	Bit 7	Bit 6*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DS1 Received Signaling Registers (0—23)	P	G	F	X	D	C	B	A
Voice Channel with 16-State Signaling	P	0	0	X	D	C	B	A
Voice Channel with 4-State Signaling	P	0	1	X	X	X	B	A
Voice Channel with 2-State Signaling	P	1	1	X	X	X	X	A
Data Channel (no signaling)	P	1	0	X	X	X	X	X

* Bit 6 and Bit 5 of the DS1 receive signaling registers are copied from Bit 6 and Bit 5 of the DS1 transmit signaling registers.

Receive Signaling Registers: CEPT Format

Table 54. Receive Signaling Registers: CEPT Format (RSR0—RSR31)

Receive Signal Registers	Bit 7	Bit 6—5	Bit 4*	Bit 3	Bit 2	Bit 1	Bit 0
RSR0: IRSM Mode Only	X	X	E0	X	X	X	X
RSR1—TSR15	P	X	E[15:1]	D[15:1]	C[15:1]	B[15:1]	A[15:1]
RSR16: IRSM Mode Only	X	X	E16	X	X	X	X
RSR[31:17]	P	X	E[31:17]	D[31:17]	C[31:17]	B[31:17]	A[31:17]

* This bit contains the IRSM information in time slot 0. In PCS0 or PCS1 signaling mode, this bit is indeterminate.

Register Structure (continued)

Parameter/Control Registers

These registers define the mode configuration of each framer unit, are initially set to a default value upon a hardware reset, and are all read/write registers.

Default states of all bits in this register group are also indicated in the parameter/control register map.

Primary Interrupt Group Enable Register (PR0)

The bits in this register enable the event groups that assert the interrupt pin high.

Table 55. Primary Interrupt Group Enable Register (PR0)

Bits	Description
0	**Facility Alarm Interrupt Enable (FAIE).** A 1 enables facility alarm interrupts.
1	**Remote Alarm Interrupt Enable (RAIE).** A 1 enables remote alarm interrupts.
2	**Facility Event Interrupt Enable (FEIE).** A 1 enables facility event interrupts.
3	**System Event Interrupt Enable (SEIE).** A 1 enables system event interrupts.
4	**Transmit Signaling Superframe Event Interrupt Enable (TSSEI).** A 1 enables an interrupt at the start of a transmit line signaling superframe.
5	**Receive Signaling Superframe Event Interrupt Enable (RSSEI).** A 1 enables an interrupt at the start of a receive line signaling superframe.
6	**Excessive CRC Error Interrupt Enable (ECEIE).** A 1 enables interrupts whenever the receive framer detects excessive CRC errors. The threshold is 32 out of 33 errored CRC checksum blocks for ESF and 915 out of 1000 for CEPT.
7	**Master Interrupt Enable (MIE).** A 1 permits enabled interrupt conditions to generate interrupts. A 0 will disable **all** interrupts.

Register Structure (continued)

Parameter/Control Registers (continued)

Framer Mode Option Register (PR1)

Table 56. Framer Mode Option Bits Decoding

Frame Format		Bit 7	Bit 6	Bit 5	Bit 4 FMODE-4	Bit 3 FMODE-3	Bit 2 FMODE-2	Bit 1 FMODE-1	Bit 0 FMODE-0
ESF (2 out of 4 FBEs = LFA)		X	X	X	0	0	0	0	0
D4 (2 out of 4 FBEs = LFA)		X	X	X	0	0	0	0	1
DDS		X	X	X	0	0	0	1	0
DDS with FDL		X	X	X	0	0	0	1	1
SLC-96		X	X	X	0	0	1	0	0
D4 (2 out of 6 FBEs = LFA)		X	X	X	0	0	1	0	1
ESF (2 out of 6 FBEs = LFA)		X	X	X	0	0	1	1	1
Transmit ESF Receive D4 (2 out of 4 FBEs = LFA)		X	X	X	1	0	0	0	0
Transmit D4 Receive ESF (2 out of 4 FBEs = LFA)		X	X	X	1	0	0	0	1
Transmit D4 Receive ESF (2 out of 6 FBEs = LFA)		X	X	X	1	0	1	0	1
Transmit ESF Receive D4 (2 out of 6 FBEs = LFA)		X	X	X	1	0	1	1	1
CEPT with no CRC-4	CCS	X	X	X	0	1	0	0	0
	PCS Mode 0	X	X	X	0	1	0	0	1
	PCS Mode 1	X	X	X	0	1	0	1	0
CEPT with CRC-4	CCS	X	X	X	0	1	1	0	0
	PCS Mode 0	X	X	X	0	1	1	0	1
	PCS Mode 1	X	X	X	0	1	1	1	0
Line Codes		LCOPT2	LCOPT1	LCOPT0	X	X	X	X	X
B8ZS (T/R)		0	0	0	X	X	X	X	X
ZCS (T/R)		0	0	1	X	X	X	X	X
HDB3 (T/R)		0	1	0	X	X	X	X	X
AMI (T/R)		0	1	1	X	X	X	X	X
B8ZS (T), AMI (R)		1	0	0	X	X	X	X	X
ZCS (T), B8ZS (R)		1	0	1	X	X	X	X	X
Single Rail		1	1	0	X	X	X	X	X
AMI (T), B8ZS (R)		1	1	1	X	X	X	X	X

Register Structure (continued)

Parameter/Control Registers (continued)

Automatic Transmission Enable Register (PR2)

Table 57. Automatic Transmission Enable Register (PR2)

Bits	Description
0	**Automatic A Bit on LFA (AALFA).** A 1 transmits A = 1 to the line whenever the receive framer detects LFA.
1	**Automatic A Bit on LMFA (AALMFA).** A 1 transmits A = 1 to the line whenever the receive framer detects LMFA.
2	**Automatic Receive Channel Squelch (ARCHSQ).** A 1 enables the automatic transmission of AIS to the system interface (DXA, DXB) when in the LFA state. CEPT only.
3	**Automatic Receive Signaling Squelch (ARSGSQ).** A 1 enables squelching of time slot 16 signaling data with the alarm indication signal (all ones) during loss of time slot 16 signaling multiframe alignment state.
4	**Automatic Line Loopback Enable (ALLBE).** A 1 enables the framer section to execute the line loopback on or off commands without system intervention.
5	**Enable ITU G.826 Mode.** A 1 enables the G.826 performance monitoring mode.
6	**Enable CRC-4 100 ms Timer.** A 1 enables the CRC-4 multiframe alignment algorithm with 100 ms timer in CEPT.
7	**Enable CRC-4 400 ms Timer.** A 1 enables the CRC-4 multiframe interworking alignment algorithm and 400 ms timer in CEPT.

On-Demand Transmit Register 1 (PR3)

Table 58. On-Demand Register 1 Bits Decoding

Transmit Signal	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit Remote Frame Alarm.	X	X	X	X	X	X	X	1
Transmit Japanese Remote Frame Alarm. CEPT: Transmit NOT FAS time slot in all every time slot 0 of the transmit system framers. (Duplicate NOT FAS time slot 0 data.)	X	X	X	X	X	X	1	X
Transmit Remote Multiframe Alarm (CEPT-only).	X	X	X	X	X	1	X	X
Transmit Facility Data Link AIS.	X	X	X	X	1	X	X	X
Transmit Squelch Code (PR5) in all Transmit Line Interface Time Slots. In the DDS modes, transmit the unconnected code (UC = 00011000) in transmit line slots 1 through 23.	X	X	X	1	X	X	X	X
Transmit Framed AIS to Line Interface.	0	0	1	0	X	X	X	X
Transmit Low-Density Signal to Line Interface: Framed 0001 Pattern.	0	1	0	0	X	X	X	X
Transmit Squelch Code Register in Line Time Slot 1: PR5.	0	1	1	0	X	X	X	X
Transmit High-Density Signal to Line Interface: Framed AIS.	1	0	0	0	X	X	X	X
Transmit Unframed AIS to Line Interface.	1	0	1	0	X	X	X	X
Transmit Pseudorandom Signal to Line Interface ($2^{15} - 1$).	1	1	0	0	X	X	X	X
Transmit Quasi-random Signal to Line Interface (ANSI T1.403).	1	1	1	0	X	X	X	X

Register Structure (continued)

Parameter/Control Registers (continued)

On-Demand Transmit Register 2 (PR4)

Table 59. On-Demand Register 2 Bits Decoding

Transmit Signal	Bit 7	Bit 6	Bit 5 DLB1	Bit 4 DLB0	Bit 3	Bit 2	Bit 1	Bit 0
Transmit System Channel Squelch: DDS mode transmits the MOS code (00011010). All other modes transmit the AIS (all ones) pattern.	X	X	X	X	X	X	X	1
Transmit System Signaling Squelch: CEPT only: AIS is written into time slot 16 of the transmit system data.	X	X	X	X	X	X	1	X
Receive Framer Reframe: Force the LFA state in the receive framer and initiate a search of frame alignment. Subsequent reframe commands must have this bit in the 0 state first.	X	X	X	X	X	1	X	X
Receive Signaling Inhibit: Inhibit updating of the receive signaling buffer.	X	X	X	X	1	X	X	X
Line Loopback	X	X	0	1	X	X	X	X
Payload Loopback with Pass-Through F Bits: Received channelized-payload data, CRC checksum bits and F bits are looped backed to the line. The system's facility data link bit stream is inserted into the looped data and then transmitted to the line. Inserting a new facility data link into its F-bit position in ESF mode does not change the CRC-6 checksum (all F-bit positions are set to 1 when calculating the CRC-6 checksum). **This mode is NOT recommended for CEPT framing format.** The receive framer processes and monitors the incoming line data autonomously to this loopback mode and transmits the formatted data to the system in the normal format via the CHI.	X	X	1	0	X	X	X	X
Payload Loopback with Regenerated F Bits: As defined in the Lucent Technologies TR 54016, *Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format*, September 1989 edition, the received channelized-payload data is looped back to the line. The framing bits are generated within the transmit framer sections at the point of the PLB. The regenerated framing information includes the F-bit pattern, the CRC checksum bit, and the system's facility data link bit stream. This loopback mode can be used with the CEPT framing mode. The entire time slot 0 data (FAS and NOT FAS) is regenerated by the transmit framer. The receive framer processes and monitors the incoming line data autonomously to this loopback mode and transmits the formatted data to the system in the normal format via the CHI.	X	X	1	1	X	X	X	X
Transmit Line Loopback On Code: 001 (with Valid F-bit Information).	X	1	X	X	X	X	X	X
Transmit Line Loopback Off Code: 00001 (with valid F-bit Information).	1	X	X	X	X	X	X	X

Register Structure (continued)

Parameter/Control Registers (continued)

Framer Squelch Code Register (PR5)

These 8 bits are transmitted in each time slot when the transmit channel squelch command is enabled.

Table 60. Framer System Squelch Code Register (PR5)

Bits	Description
0—7	System Squelch Code 0—7 (SQ0—SQ7) CEPT: XSA Mask **(XSAE4—XSAE8) Default = 1.**

Transmit Sa Source Register (PR6)

These bits contain the transmit Sa bits and define the source of the Sa bits.

Table 61. Sa4—Sa8 Source Register (PR6)

Bits	Description
0—4	**Transmit Sa4—Sa8 Bit (XSA4—XSA8).**
5	**System Frame Sync Mask (SYSFSM).** A 1 masks the system frame synchronization signal in the transmit framer section. **Note:** The transmit framer must see at least one valid system synchronization pulse to initialize its counts; afterwards, this bit may be set. It it suggested for those applications that have jitter on the transmit clock signal relative to the system clock signal to enable this bit so that the jitter is isolated from the transmit framer.
6	**Sa-Bit Source (SAS).** A 1 enables the transmission of Sa[8:4] bits from the bits 0 to 4 of this register. If 0, then the Sa[8:4] bits are transmitted from the system interface transparently through the framer unit; the system data must maintain a biframe alignment pattern of alternating 1, 0 in bit 2 of all time slot 0s on the receive CHI. Bit 2 must be 1 in those frames containing the Sa bit information; bit 2 must be 0 in those frames not containing Sa bit information. When the biframe alignment is not correct, the transmit framer will transmit corrupt data.
7	**Transmit Sa4 Source (Sa4S).** A 1 enables the transmit facility data link input (XFD) to source the transmit Sa4 bit. All other sources are ignored.

Register Structure (continued)

Parameter/Control Registers (continued)

Si-Bit/X-Bit/E-Bit Source Register (PR7)

These bits define the source of the E, X, and Si bits transmitted to the line.

Table 62. Si-Bit/X-Bit/E-Bit Source Register (PR7)

Bits	Description
0—2	**Transmit Time Slot 16 X0—X2 Bits (XTS16X0—XTS16X2).** The content of these bits are written into CEPT signaling multiframe time slot 0 X bits.
3	**X-Bit Source (XS).** A 1 enables the XTS16X[2:0] bits to be written into CEPT time slot 16 multiframe frame 0. A 0 transmits the X bits transparently.
4	**Transmit Bit 1 in FAS (XSiF).** The content of this bit can be transmitted to the line in bit 1 of the FAS. In CRC-4 mode, this bit is used for E-bit data in frame 13, only valid if ATECE = 0.
5	**Transmit Bit 1 in NOT FAS (XSiNF).** The content of this bit can be transmitted to the line in bit 1 of the NOT FAS. In CRC-4 mode, this bit is used for E-bit data in frame 15, only valid if ATECE = 0.
6	**Si-Bit Source (SIS).** A 0 forces XSiF and XSiNF to the line in FAS and NOT FAS, respectively. A 1, in non-CRC-4 mode, transmits system data to the line transparently.
7	**Automatic Transmit E Bit = 0 for Received CRC-4 Errored Events (ATECE).** A 1 transmits E = 0 to the line whenever the receive framer detects a received CRC-4 errored checksum.

Framer Exercise Register (PR8)

Table 63. Framer Exercise Register (PR8)

Bits		Description
FEX0—FEX5		Framer Exercise Bits 0—5 (FEX0—FEX5). See Table 66.
FEX6	FEX7	Second Pulse Interval.
0	0	1 Second Pulse.
0	1	500 ms Pulse.
1	0	100 ms Pulse.
1	1	Manufacturer's Test.

Register Structure (continued)

Parameter/Control Registers (continued)

Table 64. Framer Exercises, PR8, Bits 5—0

Exercise Type	FEX5	FEX4	FEX3	FEX2	FEX1	FEX0	Exercise	Framing Format
—	0	0	0	0	0	0	No exercise	
System Status	0	0	0	0	0	1	Loss of transmit clock stuck at 0	All
	0	0	0	0	1	0	Loss of transmit clock stuck at 1	All
	0	0	0	1	0	1	Loss of receive clock stuck at 0	All
	0	0	0	1	1	0	Loss of receive clock stuck at 1	All
Facility Status	0	0	1	0	0	0	Line format violation	All
							CRC checksum error	ESF or CEPT
							Receive remote frame alarm	D4 or ESF
	0	0	1	0	0	1	Alarm indication signal detection	All
							Loss of frame alignment	CEPT
							Receive remote frame alarm	Japanese D4
	0	0	1	0	1	0	Time slot 0 1-bit shift	CEPT
							Transmit corrupt CRC	ESF & CEPT
	0	0	1	0	1	1	Frame-bit error & loss of frame alignment	All
							Loss of time slot 16 multiframe alignment	CEPT
							Remote frame alarm	D4 & DDS
							CRC bit errors	ESF & CEPT
	0	0	1	1	0	0	Frame-bit errors	All
	0	0	1	1	0	1	Frame-bit errors and loss of frame alignment	All*
							Loss of time slot 16 multiframe alignment	PCS0 & PSC1†
	0	0	1	1	1	0	Frame-bit error and loss of frame alignment	All*
							Change of frame alignment	ESF, DDS, & CEPT (ADPTTE = 0)
							Loss of time slot 16 multiframe alignment	PCS0 & PCS1†
	0	0	1	1	1	1	Excessive CRC checksum errors	ESF & CEPT

* This affects the transmitted system data if ACHSQ when asserted and the transmitted line A bit when AXRFA is asserted.

† This affects the transmitted system time slot 16 data when AXSGSQ is asserted and affects the transmitted line time slot 16 multiframe alarm when AXRMFA is asserted.

Register Structure (continued)

Parameter/Control Registers (continued)

Table 64. Framer Exercises, PR8 Bits 5—0 (continued)

Exercise Type	FEX5	FEX4	FEX3	FEX2	FEX1	FEX0	Exercise	Framing Format
Performance Status	0	1	0	0	0	0	Errored second	All
	0	1	0	0	0	1	Bursty errored second	
	0	1	0	0	1	0	Severely errored second	
	0	1	0	0	1	1	Severely errored second count	
	0	1	0	1	0	0	Unavailable state	
	0	1	0	1	0	1	Factory test	
	0	1	0	1	1	0	Increment status counters SR6—SR14	
	0	1	0	1	1	1	Increment status counters SR6—SR14	
Status Counters	1	0	0	0	0	1	CRC error counter	All
	1	0	0	0	1	0	Errored event counter	
	1	0	0	0	1	1	Errored second counter	
	1	0	0	1	0	0	Severely errored second counter	
	1	0	0	1	0	1	Unavailable second counter	
	1	0	0	1	1	0	Line format violation counter	
	1	0	0	1	1	1	Frame bit error counter	
Manufacturer's	1	1	0	0	0	0	Factory test	—
	1	1	1	1	1	0	Enables access to the line XSA-bit enable register located in PR5. The bit assignments are PR5_Bits[0:4] for XSa Bits[4:8], respectively. While PR8 is programmed in this state, PR5 access is directed to the XSA-Bit Enable register (the default state for the XSA enable is 1, transmit from PR6, bits 0 through 4, when SAS = 1). When PR6, bit 6 = 1, setting the XSA-bit enable bits to 0 allows for transparent transmission of CHI Sa data. When PR8 is programmed to any other state, PR5 accesses Framer Squelch register.	CEPT Only
	1	1	1	1	1	1	Transmit data transparently (CHI-FS is used for the transmit framer FS; ignore receive framing data.)	CEPT Only
	All other combinations						Reserved	—

Register Structure (continued)

Parameter/Control Registers (continued)

System Interface Control Register (PR9)

Table 65. Facility Alarm Interrupt Enable Register (PR9)

Bits	Description
0—2	**Stuffed Time Slots (STS0—STS2).** **In DS1 modes only: 012** 000: SDDDSDDDSDDDSDDDSDDDSDDDSDDDSDDD 001: DSDDDSDDDSDDDSDDDSDDDSDDDSDDDSDD 010: DDSDDDSDDDSDDDSDDDSDDDSDDDSDDDSD 011: DDDSDDDSDDDSDDDSDDDSDDDSDDDSDDDS 1XX: DDDDDDDDDDDDDDDDDDDDDDDSSSSSSSS (Default mode) **In CEPT mode only: 012** 000: Sa4 = FDL 001: Sa5 = FDL 010: Sa6 = FDL 011: Sa7 = FDL 100: Sa8 = FDL
1	**Phase-Lock Loop Reference (PLLREF).** A 0 enables the use of the clock signal CLKXR as the reference signal and PLLCK as the variable signal internal phase-lock loop circuit. The EPLL signal is connected to the VCXO circuit that produces the PLLCK signal. A 1 enables the use of the clock signal PLLCK as the reference signal and CLKXR as the variable signal internal phase-lock loop circuit. The EPLL signal is connected to the VCXO circuit that produces the CLKXR signal. This mode can be used in applications where the receive line clock is the reference signal; the receive clock signal must be connected to the RLCK input (as normal) and the PLLCK input. The T7230A is the "master" clock source of the system in this mode. In the master mode, it is recommended that the T7230A also generate the system frame synchronization signal.
4	**Concentration Highway Master Mode (CHIMM).** A 0 enables the system's frame synchronization signal (FS) to drive both the receive and transmit paths of the T7230's concentration highway interface. A 1 enables the T7230's transmit concentration interface to generate a system frame synchronization signal derived from the receive line interface. The T7230's system frame synchronization signal is generated on the OFS output pin (pin #50). Applications using the receive line clock as the reference clock signal of the system are recommended to enable this mode and use the OFS signal generated by the T7230.
5	**Superframe Select (SFSEL).** A 0 enables the signaling superframe pulse referenced from the CHI data. The superframe signal will be active-high during time slot 0 of the CHI at the beginning of the superframe. A 1 enables the signaling superframe pulse referenced from the frame sections. The superframe signal will be active-high during bit 0 of time slot 0 of the framer data at the beginning of the superframe.
6—7	**Framer Factory Test Modes (FFT0—FFT1).** These bits must always be 0.

Register Structure (continued)

Parameter/Control Registers (continued)

Signaling Mode Register (PR10)

Table 66. Signaling Mode Register (PR10)

Bits	Description
0	**Transparent Signaling (TSIG).** A 0 enables signaling information to be inserted into and extracted from the data stream. The signaling source is either the signaling registers or the system data (in the associated signaling mode). In DS1 modes, the choice of data or voice channels assignment for each channel is a function of the programming of the F and G bits in the transmit signaling registers. A 1 (the default mode) enables data to pass through the device transparently. All channels are treated as data channels.
1	**Stomp Mode (STOMP).** A 1 enables the receive signaling circuit to replace (in those time slots programmed for signaling) all signaling bits (in the receive line bit stream) with a 1, after extracting the valid signaling information. A 0 allows the received signaling bits to pass through the receive signaling circuit unmodified.
2	**Associated Signaling Mode (ASM).** A 1 enables the associate signaling mode that configures the CHI to carry both data and its associated signaling information for a particular channel. Enabling this mode must be in conjunction with the programming of the CHI data rate to 4.048 Mbits/s. Each channel consists of 16 bits where 8 bits are data and the remaining 8 bits are signaling information
3	**Channel Signaling Suppression or Nine-State Signaling (CCS_9ST).** DS1 *SLC*-96: A 1 enables the nine-state signaling mode. CEPT: A 1 enables the received signaling circuit substitute of the signaling combination of ABCD = 0000 to ABCD = 1111.
4	**Message-Oriented Signaling or Common Channel Signaling (MOS_CCS).** DS1: A 1 enables the channel 24 message-oriented signaling mode. CEPT: A 1 enables the time slot 16 common channel signaling mode.
5	**IRSM/TSRFGE Mode (IRSM).** A 1 enables the CEPT IRSM mode in time slot 0. DS1 formats and ASM = 1: A 1 enables the transmit signaling register F and G bits to define the robbed-bit signaling format while the ABCD bit information is extracted from the CHI interface. The F and G bits are copied to the receive signaling block and are used to extract the signaling information from the receive line.
6	**Framer Data (FRMD).** A 0 enables the divided down signal of PLLCK and CLKXR onto the DPLLCK and DCLKXR output pins, respectively. A 1 forces receive line data and receive line frame synchronization signals onto the DPLLCK and DCLKXR output pins, respectively. Enabling this mode assumes an application that does not require the divided down PLLCK and CLKXR signals.
7	**Framer Factory Test (FFT2).** This bit must always be 0.

Register Structure (continued)

Parameter/Control Registers (continued)

System Clock Control Register (PR11)

Table 67. System Clock Control Register (PR11)

Transmit Signal	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High-Frequency_Low-Frequency PLLCK Clock Mode (HFLF = 0). Enables the low-frequency PLLCK mode for the divide-down circuit in the internal phase-lock loop section (DS1 PLLCK = 1.544 MHz; CEPT PLLCK = 2.048 MHz). The divide-down circuit will produce an 8 kHz signal on DPLLCK.	X	X	X	X	X	X	X	0
High-Frequency_Low-Frequency PLLCK Clock Mode (HFLF = 1). A 1 enables the high-frequency PLLCK mode for the divide-down circuit in the internal phase-lock-loop section (DS1: PLLCK = 6.176 (4 x 1.544) MHz; CEPT: 8.192 (4 x 2.048) MHz). The divide-down circuit will produce a 32 kHz signal on DPLLCK.	X	X	X	X	X	X	X	1
Concentration Highway Clock Mode (CMS = 0). CLKXR frequency and CHI data (DRA, DRB, DXA, and DXB) rates are equal.	X	X	X	X	X	X	0	X
Concentration Highway Clock Mode (CMS = 1). CLKXR frequency is 2X the CHI data (DRA, DRB, DXA, and DXB) rate.	X	X	X	X	X	X	1	X
Concentration Highway Data Rate Select (CDRS = 0). CHI data (DRA, DRB, DXA, and DXB) rate is 2.048 Mbits/s.	X	X	X	X	X	0	X	X
Concentration Highway Data Rate Select (CDRS = 1). CHI data (DRA, DRB, DXA, and DXB) rate is 4.096 Mbits/s.	X	X	X	X	X	1	X	X
Software Reset (SWRST = 0). T7230A operates as programmed.	X	X	X	X	0	X	X	X
Software Reset (SWRST = 1). T7230A is placed into reset state where all parameter registers (excluding this bit) are forced into the default state. SWRST must be set to the 0 state to deassert this state.	X	X	X	X	1	X	X	X
Software Restart (SWRSTRT = 0). T7230A operates as programmed.	X	X	X	0	X	X	X	X
Software Restart (SWRSTRT = 1). T7230's internal counters are placed into reset state. The state of the parameter registers remain as programmed. SWRSTRT must be set to the 0 state to deassert this state.	X	X	X	1	X	X	X	X
Open Collector Enable (OCE = 0). CHI outputs DXA and DXB generate a positive pulse (5 V) to represent a binary 1.	X	X	0	X	X	X	X	X
Open Collector Enable (OCE = 1). CHI outputs DXA and DXB are placed in a high-impedance state to represent a binary 1.	X	X	1	X	X	X	X	X
Full System Loopback (FSLB = 0). T7230A transmits and receives data as programmed.	X	0	X	X	X	X	X	X
Full System Loopback (FSLB = 1). T7230A loops back to the system DRA and/or DRB data to DXA and/or DXB. Data transverses the entire transmit path and receive path of the T7230.	X	1	X	X	X	X	X	X
Framer Factory Test (FFT3). This bit must always be 0.	0	X	X	X	X	X	X	X

Register Structure (continued)

Parameter/Control Registers (continued)

Framer Idle Code Register (PR12)

These 8 bits are transmitted in each time slot when the transmit channel squelch command is enabled.

Table 68. Framer Line Idle Code Register (PR12)

Bits	Description
0—7	Line Idle Code 0—7 (IC0—IC7) (Default = 01111111).

CHI Common Control Register (PR13)

These bits define the common attributes of the CHI for both DX and DR.

Table 69. CHI Common Control Register (PR13)

Bits	Description
0—2	**CHI DX Bit Offset (XOFF0—XOFF2).** These 3 bits define the bit offset from FS for each transmit time slot. CMS = 0, the offset is the number of CLKXR clock periods by which the first bit is delayed from FS. CMS = 1, the offset is twice (2X) the number of CLKXR clock periods by which the first bit is delayed from FS.
3	**Highway Enable (HWYEN).** A 1 in this bit position enables transmission to the concentration highway. This allows the T7230A to be fully configured before transmission to the highway. A 0 forces the idle code as defined in PR12, to be transmitted to the line in all payload time slots and the DX pin is forced to a high-impedance state for all CHI transmitted time slots.
4—6	**CHI DR Bit Offset (ROFF0—ROFF2).** These 3 bits define the bit offset from FS for each received time slot. CMS = 0, the offset is the number of CLKXR clock periods by which the first bit is delayed from FS. CMS = 1, the offset is twice (2X) the number of CLKXR clock periods by which the first bit is delayed from FS.
7	**Frame Clock Edge (FE).** A 0 (1) enables the falling (rising) edge of CLKXR to latch in the frame synchronization signal, FS.

CHI Transmit Control Register (PR14)

Table 70. CHI Transmit Control Register (PR14)

Bits	Description
0—5	**Transmit Byte Offset (XBYOFF0—XBYOFF5).** These 6 bits define the byte offset from FS to the beginning of the next transmit CHI frame on DX.
6	**Transmitter Clock Edge (XCE).** A 1 (0) enables the rising (falling) edge of CLKXR to clock out data on DX.
7	**Transmit Least Significant Bit First (XLBIT).** A 0 forces the most significant bit of each time slot (bit 0) as the most significant bit of the time slot. A 1 forces the least significant bit of each time (bit 7) as the most significant bit of the time slot.

Register Structure (continued)

Parameter/Control Registers (continued)

CHI Receive Control Register (PR15)

Table 71. CHI Receive Control Register (PR15)

Bits	Description
0—5	**Receiver Byte Offset (RBYOFF0—RBYOFF5).** These 6 bits define the byte offset from FS to the beginning of the next receive CHI on DR.
6	**Receiver Clock Edge (RCE).** A 1 (0) enables the rising (falling) edge of CLKXR to latch data on DR.
7	**Receive Least Significant Bit First (RLBIT).** A 0 forces bit 0 of the time slot as the most significant bit of the time slot. A 1 forces bit 7 of the time slot as the most significant bit of the time slot.

CHI Transmit Time-Slot Enable Registers (PR16—PR19)

These four registers define which transmit CHI time slots are enabled. A 1 enables the DX time slot. A 0 forces the CHI transmit highway time slot to be 3-stated.

Table 72. CHI Transmit Time-Slot Enable Registers (PR16—PR19)

PR	Bits	Description
16	7—0	**Transmit Time-Slot Enable Bits 31—24 (TTSE31—TTSE24).**
17	7—0	**Transmit Time-Slot Enable Bits 23—16 (TTSE23—TTSE16).**
18	7—0	**Transmit Time-Slot Enable Bits 15—8 (TTSE15—TTSE8).**
19	7—0	**Transmit Time-Slot Enable Bits 7—0 (TTSE7—TTSE0).**

Receive Time-Slot Enable Registers (PR20—PR23)

These four registers define which receive CHI time slots are enabled. A 1 enables the CHI-DR time slots. A 0 disables the CHI-DR time slot and transmits the programmable idle code to the line in the corresponding time slot. When RTSEx = 0 and RHSx = 0, then 01111111 is transmitted to the line interface. When RTSEx = 0 and RHSx = 1, then the programmable idle code in PR12 is transmitted to the line interface.

Table 73. Receive Time-Slot Enable Registers (PR20—PR23)

PR	Bits	Description
20	7—0	**Receive Time-Slot Enable Bits 31—24 (RTSE31—RTSE24).**
21	7—0	**Receive Time-Slot Enable Bits 23—16 (RTSE23—RTSE16).**
22	7—0	**Receive Time-Slot Enable Bits 15—8 (RTSE15—RTSE8).**
23	7—0	**Receive Time-Slot Enable Bits 7—0 (RTSE7—RTSE0).**

Register Structure (continued)

Parameter/Control Registers (continued)

CHI Transmit Highway Select Registers (PR24—PR27)

These four registers define which transmit CHI highway DXA or DXB contains valid data for the active time slot. A 0 enables DXA; a 1 enables the DXB.

Table 74. CHI Transmit Highway Select Registers (PR24—PR27)

PR	Bits	Description
24	7—0	Transmit Highway Select Bits 31—24 (THS31—THS24).
25	7—0	Transmit Highway Select Bits 23—16 (THS23—THS16).
26	7—0	Transmit Highway Select Bits 15—8 (THS15—THS8).
27	7—0	Transmit Highway Select Bits 7—0 (THS7—THS0).

CHI Receive Highway Select Registers (PR28—PR31)

These four registers define which receive CHI highway DRA or DRB contains valid data for the active time slot. A 0 enables DRA; a 1 enables the DRB.

Table 75. CHI Receive Highway Select Registers (PR28—PR31)

PR	Bits	Description
28	7—0	Receive Highway Select Bits 31—24 (RHS31—RHS24).
29	7—0	Receive Highway Select Bits 23—16 (RHS23—RHS16).
30	7—0	Receive Highway Select Bits 15—8 (RHS15—RHS8).
31	7—0	Receive Highway Select Bits 7—0 (RHS7—RHS0).

Transmit Signaling Registers: DS1 Format

Table 76. Transmit Signaling Registers: DS1 Format (TSR0—TSR23)

—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DS1 Transmit Signaling Registers (0—23)	P	G	F	X	D	C	B	A
ESF: Format Voice Channel with 16-State Signaling; *SLC*-96: 9-State Signaling	P	0	0	X	D	C	B	A
Voice Channel with 4-State Signaling	P	0	1	X	X	X	B	A
Voice Channel with 2-State Signaling	P	1	1	X	X	X	X	A
Data Channel (No Signaling)	P	1	0	X	X	X	X	X

Register Structure (continued)

Parameter/Control Registers (continued)

Transmit Signaling Registers: CEPT Format

Table 77. Transmit Signaling Registers: CEPT Format (TSR0—TSR31)

Transmit Signal Registers	Bit 7	Bit 6—5	Bit 4*	Bit 3	Bit 2	Bit 1	Bit 0
TSR0: IRSM Mode Only	X	X	E0	X	X	X	X
TSR1—TSR15	P	X	E[15:1]	D[15:1]	C[15:1]	B[15:1]	A[15:1]
TSR16: IRSM Mode Only	X	X	E16	X	X	X	X
TSR[31:17]	P	X	E[31:17]	D[31:17]	C[31:17]	B[31:17]	A[31:17]

* This bit contains the IRSM information in time slot 0. In PCS0 or PCS1 signaling mode, this bit is ignored.

Register Maps

Tables 78, 79, 80, and 81 show the bit maps of the status registers, the receive signaling registers, the parameter registers, and the transmit signaling registers, respectively.

Status Registers

Table 78. Status Register Map

SR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address		Type*
									DEC	HEX	
SR0	0	ECE	RSSFE	TSSFE	PACDE	FAE	RAC	FACI	0	00	COR
SR1	0	UASTATE	LTS16MFA	LTS0MFA	LFALR	AIS	LSSFA	LFA	1	01	R
SR2	RSA6_X	RSA6_F	RSA6_E	RJYA /RSA6_C	RMFA	RSA6_A	RSA6_8	RFA	2	02	R
SR3	LLBOFF	LLBON	CFSHT	SLIP_U	SLIP_O	CFA	FBE	LFV	3	03	COR
SR4	CSFA	OUAS	REB_1	REB_0	CRCRST	SES	BES	ES	4	04	COR
SR5	RCEB	RCRCXR	0	0	BFA	LBFA	SCO	LTSFA	5	05	COR
SR6	CEC15	CEC14	CEC13	CEC12	CEC11	CEC10	CEC9	CEC8	6	06	COR
SR7	CEC7	CEC6	CEC5	CEC4	CEC3	CEC2	CEC1	CEC0	7	07	COR
SR8	EEC15	EEC14	EEC13	EEC12	EEC11	EEC10	EEC9	EEC8	8	08	COR
SR9	EEC7	EEC6	EEC5	EEC4	EEC3	EEC2	EEC1	EEC0	9	09	COR
SR10	ESC15	ESC14	ESC13	ESC12	ESC11	ESC10	ESC9	ESC8	10	0A	COR
SR11	ESC7	ESC6	ESC5	ESC4	ESC3	ESC2	ESC1	ESC0	11	0B	COR
SR12	BESC15	BESC14	BESC13	BESC12	BESC11	BESC10	BESC9	BESC8	12	0C	COR
SR13	BESC7	BESC6	BESC5	BESC4	BESC3	BESC2	BESC1	BESC0	13	0D	COR
SR14	SESC15	SESC14	SESC13	SESC12	SESC11	SESC10	SESC9	SESC8	14	0E	COR
SR15	SESC7	SESC6	SESC5	SESC4	SESC3	SESC2	SESC1	SESC0	15	0F	COR
SR16	UASC15	UASC14	UASC13	UASC12	UASC11	UASC10	UASC9	UASC8	16	10	COR
SR17	UASC7	UASC6	UASC5	UASC4	UASC3	UASC2	UASC1	UASC0	17	11	COR
SR18	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8	18	12	COR
SR19	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	ETUC0	19	13	COR
SR20	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	ENT0	20	14	COR
SR21	0	0	0	RSA8	RSA7	RSA6	RSA5	RSA4	21	15	R
SR22	0	0	RSi_NF	RSi_FAS	0	RX2	RX1	RX0	22	16	R
SR23	0	0	0	0	0	0	0	0	23	17	R
SR24	0	0	0	0	0	0	0	0	24	18	R
SR25	0	0	0	0	0	0	0	0	25	19	R
SR26	0	0	0	0	0	0	0	0	26	1A	R
SR27	0	0	0	0	0	0	0	0	27	1B	R
SR28	0	0	0	0	0	0	0	0	28	1C	R
SR29	0	0	0	0	0	0	0	0	29	1D	R
SR30	0	0	0	0	0	0	0	0	30	1E	R
SR31	0	0	0	0	0	0	0	0	31	1F	R

* COR = clear-on-read register; R = read-only register.

Register Maps (continued)

Received Signaling Registers

Table 79. Receive Signaling Registers MAP

RSR	Bit 7	Bit 6[1]	Bit 5[1]	Bit 4[2]	Bit 3	Bit 2	Bit 1	Bit 0	Address		Type[3]
									DEC	HEX	
RSR0[4]	P	G_0	F_0	E_0	D_0	C_0	B_0	A_0	32	20	R
RSR1	P	G_1	F_1	E_1	D_1	C_1	B_1	A_1	33	21	R
RSR2	P	G_2	F_2	E_2	D_2	C_2	B_2	A_2	34	22	R
RSR3	P	G_3	F_3	E_3	D_3	C_3	B_3	A_3	35	23	R
RSR4	P	G_4	F_4	E_4	D_4	C_4	B_4	A_4	36	24	R
RSR5	P	G_5	F_5	E_5	D_5	C_5	B_5	A_5	37	25	R
RSR6	P	G_6	F_6	E_6	D_6	C_6	B_6	A_6	38	26	R
RSR7	P	G_7	F_7	E_7	D_7	C_7	B_7	A_7	39	27	R
RSR8	P	G_8	F_8	E_8	D_8	C_8	B_8	A_8	40	28	R
RSR9	P	G_9	F_8	E_8	D_8	C_8	B_8	A_8	41	29	R
RSR10	P	G_10	F_10	E_10	D_10	C_10	B_10	A_10	42	2A	R
RSR11	P	G_11	F_11	E_11	D_11	C_11	B_11	A_11	43	2B	R
RSR12	P	G_12	F_12	E_12	D_12	C_12	B_12	A_12	44	2C	R
RSR13	P	G_13	F_13	E_13	D_13	C_13	B_13	A_13	45	2D	R
RSR14	P	G_14	F_14	E_14	D_14	C_14	B_14	A_14	46	2E	R
RSR15	P	G_15	F_15	E_15	D_15	C_15	B_15	A_15	47	2F	R
RSR16[4]	P	G_16	F_16	E_16	D_16	C_16	B_16	A_16	48	30	R
RSR17	P	G_17	F_17	E_17	D_17	C_17	B_17	A_17	49	31	R
RSR18	P	G_18	F_18	E_18	D_18	C_18	B_18	A_18	50	32	R
RSR19	P	G_19	F_19	E_19	D_19	C_19	B_19	A_19	51	33	R
RSR20	P	G_20	F_20	E_20	D_20	C_20	B_20	A_20	52	34	R
RSR21	P	G_21	F_21	E_21	D_21	C_21	B_21	A_21	53	35	R
RSR22	P	G_22	F_22	E_22	D_22	C_22	B_22	A_22	54	36	R
RSR23	P	G_23	F_23	E_23	D_23	C_23	B_23	A_23	55	37	R
RSR24[5]	P	X[6]	X	E_24	D_24	C_24	B_24	A_24	56	38	R
RSR25[5]	P	X	X	E_25	D_25	C_25	B_25	A_25	57	39	R
RSR26[5]	P	X	X	E_26	D_26	C_26	B_26	A_26	58	3A	R
RSR27[5]	P	X	X	E_27	D_27	C_27	B_27	A_27	59	3B	R
RSR28[5]	P	X	X	E_28	D_28	C_28	B_28	A_28	60	3C	R
RSR29[5]	P	X	X	E_29	D_29	C_29	B_29	A_29	61	3D	R
RSR30[5]	P	X	X	E_30	D_30	C_30	B_30	A_30	62	3E	R
RSR31[5]	P	X	X	E_31	D_31	C_31	B_31	A_31	63	3F	R

1. In the DS1 robbed-bit signaling modes, these bits are copied from the corresponding transmit signaling registers. In the CEPT signaling modes, these bits are in the 0 state and should be ignored.
2. In the CEPT IRSM signaling modes, these bits are in the 0 state and should be ignored.
3. R = read-only register.
4. In the CEPT signaling modes, the A-, B-, C-, and D-bit information of these registers contains unknown data.
5. In the DS1 signaling modes, these registers contain unknown data.
6. Signifies unknown data.

Register Maps (continued)

Parameter Registers

Table 80. Parameter Registers MAP

PR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address		Type*
									DEC	HEX	
PR0	MIE	ECEIE	RSSEI	TSSEI	SEIE	FEIE	RAIE	FAIE	64	40	R/W
PR1	LCOPT2	LCOPT1	LCOPT0	FMODE4	FMODE3	FMODE2	FMODE1	FMODE0	65	41	R/W
PR2	E400CI	E100TR	EG826	ALLBE	ARSGSQ	ARCHSQ	AALMFA	AALFA	66	42	R/W
PR3	XPAT3	XPAT2	XPAT1	XPAT0	XFDLAIS	XRMFA	XJRFA DNF_SA	XRFA	67	43	R/W
PR4	XLLBONC	XLLBOFFC	DLB1	DLB0	RSI	RFRFRM	XSSSQ	XSCSQ	68	44	R/W
PR5	SQ7	SQ6	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	69	45	R/W
PR6	SA4S	SAS	SYSFSM	XSA8	XSA7	XSA6	XSA5	XSA4	70	46	R/W
PR7	ATECE	SIS	XSINF	XSIF	XS	XX2	XX1	XX0	71	47	R/W
PR8	FEX7	FEX6	FEX5	FEX4	FEX3	FEX2	FEX1	FEX0	72	48	R/W
PR9	FFT1	FFT0	SFSEL	CHIMM	PLLREF	STS2_ SaFDL2	STS1_ SaFDL1	STS0_ SaFDL0	73	49	R/W
PR10	FFT2	FRDM	IRSM_ TSRFBE	MOS_CCS	CSS_9ST	ASM	STOMP	TSIG	74	4A	R/W
PR11	FFT3	FSLB	OCE	SWRSTART	SWRESET	CDRS	CMS	HF_LF	75	4B	R/W
PR12	IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0	76	4C	R/W
PR13	FE	ROFF2	ROFF1	ROFF0	HWYEN	XOFF2	XOFF1	XOFF0	77	4D	R/W
PR14	XLBIT	XCE	XBYOFF5	XBYOFF4	XBYOFF3	XBYOFF2	XBYOFF1	XBYOFF0	78	4E	R/W
PR15	RLBIT	RCE	RBYOFF5	RBYOFF4	RBYOFF3	RBYOFF2	RBYOFF1	RBYOFF0	79	4F	R/W
PR16	TTSE31	TTSE30	TTSE29	TTSE28	TTSE27	TTSE26	TTSE25	TTSE24	80	50	R/W
PR17	TTSE23	TTSE22	TTSE21	TTSE20	TTSE19	TTSE18	TTSE17	TTSE16	81	51	R/W
PR18	TTSE15	TTSE14	TTSE13	TTSE12	TTSE11	TTSE10	TTSE9	TTSE8	82	52	R/W
PR19	TTSE7	TTSE6	TTSE5	TTSE4	TTSE3	TTSE2	TTSE1	TTSE0	83	53	R/W
PR20	RTSE31	RTSE30	RTSE29	RTSE28	RTSE27	RTSE26	RTSE25	RTSE24	84	54	R/W
PR21	RTSE23	RTSE22	RTSE21	RTSE20	RTSE19	RTSE18	RTSE17	RTSE16	85	55	R/W
PR22	RTSE15	RTSE14	RTSE13	RTSE12	RTSE11	RTSE10	RTSE9	RTSE8	86	56	R/W
PR23	RTSE7	RTSE6	RTSE5	RTSE4	RTSE3	RTSE2	RTSE1	RTSE0	87	57	R/W
PR24	THS31	THS30	THS29	THS28	THS27	THS26	THS25	THS24	88	58	R/W
PR25	THS23	THS22	THS21	THS20	THS19	THS18	THS17	THS16	89	59	R/W
PR26	THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8	90	5A	R/W
PR27	THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0	91	5B	R/W
PR28	RHS31	RHS30	RHS29	RHS28	RHS27	RHS26	RHS25	RHS24	92	5C	R/W
PR29	RHS23	RHS22	RHS21	RHS20	RHS19	RHS18	RHS17	RHS16	93	5D	R/W
PR30	RHS15	RHS14	RHS13	RHS12	RHS11	RHS10	RHS9	RHS8	94	5E	R/W
PR31	RHS7	RHS6	RHS5	RHS4	RHS3	RHS2	RHS1	RHS0	95	5F	R/W

* R/W = read/write register.

Register Maps (continued)

Transmit Signaling Registers

Table 81. Transmit Signaling Registers MAP

TSR	Bit 7	Bit 6[1]	Bit 5[1]	Bit 4[2]	Bit 3	Bit 2	Bit 1	Bit 0	Address		Type[3,4]
									DEC	HEX	
TSR0[5]	P	G_0	F_0	E_0	D_0	C_0	B_0	A_0	96	60	R/W
TSR1	P	G_1	F_1	E_1	D_1	C_1	B_1	A_1	97	61	R/W
TSR2	P	G_2	F_2	E_2	D_2	C_2	B_2	A_2	98	62	R/W
TSR3	P	G_3	F_3	E_3	D_3	C_3	B_3	A_3	99	63	R/W
TSR4	P	G_4	F_4	E_4	D_4	C_4	B_4	A_4	100	64	R/W
TSR5	P	G_5	F_5	E_5	D_5	C_5	B_5	A_5	101	65	R/W
TSR6	P	G_6	F_6	E_6	D_6	C_6	B_6	A_6	102	66	R/W
TSR7	P	G_7	F_7	E_7	D_7	C_7	B_7	A_7	103	67	R/W
TSR8	P	G_8	F_8	E_8	D_8	C_8	B_8	A_8	104	68	R/W
TSR9	P	G_9	F_8	E_8	D_8	C_8	B_8	A_8	105	69	R/W
TSR10	P	G_10	F_10	E_10	D_10	C_10	B_10	A_10	106	6A	R/W
TSR11	P	G_11	F_11	E_11	D_11	C_11	B_11	A_11	107	6B	R/W
TSR12	P	G_12	F_12	E_12	D_12	C_12	B_12	A_12	108	6C	R/W
TSR13	P	G_13	F_13	E_13	D_13	C_13	B_13	A_13	109	6D	R/W
TSR14	P	G_14	F_14	E_14	D_14	C_14	B_14	A_14	110	6E	R/W
TSR15	P	G_15	F_15	E_15	D_15	C_15	B_15	A_15	111	6F	R/W
TSR16[5]	P	G_16	F_16	E_16	D_16	C_16	B_16	A_16	112	70	R/W
TSR17	P	G_17	F_17	E_17	D_17	C_17	B_17	A_17	113	71	R/W
TSR18	P	G_18	F_18	E_18	D_18	C_18	B_18	A_18	114	72	R/W
TSR19	P	G_19	F_19	E_19	D_19	C_19	B_19	A_19	115	73	R/W
TSR20	P	G_20	F_20	E_20	D_20	C_20	B_20	A_20	116	74	R/W
TSR21	P	G_21	F_21	E_21	D_21	C_21	B_21	A_21	117	75	R/W
TSR22	P	G_22	F_22	E_22	D_22	C_22	B_22	A_22	118	76	R/W
TSR23	P	G_23	F_23	E_23	D_23	C_23	B_23	A_23	119	77	R/W
TSR24[6]	P	X[7]	X	E_24	D_24	C_24	B_24	A_24	120	78	R/W
TSR25[6]	P	X	X	E_25	D_25	C_25	B_25	A_25	121	79	R/W
TSR26[6]	P	X	X	E_26	D_26	C_26	B_26	A_26	122	7A	R/W
TSR27[6]	P	X	X	E_27	D_27	C_27	B_27	A_27	123	7B	R/W
TSR28[6]	P	X	X	E_28	D_28	C_28	B_28	A_28	124	7C	R/W
TSR29[6]	P	X	X	E_29	D_29	C_29	B_29	A_29	125	7D	R/W
TSR30[6]	P	X	X	E_30	D_30	C_30	B_30	A_30	126	7E	R/W
TSR31[6]	P	X	X	E_31	D_31	C_31	B_31	A_31	127	7F	R/W

1. In the DS1 robbed-bit signaling modes, these bits define the corresponding receive channel signaling mode and are copied into the received signaling registers. In the CEPT signaling modes, these bits are ignored.
2. In the CEPT IRSM signaling mode, E-bit information is valid. In all other CEPT modes, these bits contain unknown data.
3. R/W = read/write register.
4. In the associated signaling mode, these registers are read only.
5. In the CEPT signaling modes, the A-, B-, C-, and D-bit information of these registers contains unknown data.
6. In the DS1 signaling modes, these registers contain unknown data.
7. Signifies known data.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
VDD Supply Voltage Range	VDD	–0.5	6.5	V
Power Dissipation	PD	0.5	0.75	W
Storage Temperature Range	Tstg	–55	150	°C
Ambient Operating Temperature Range	TA	–40	85	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 82. ESD Threshold Voltage

Device	Voltage
T7230A	>1000 V

Electrical Characteristics

T_A = –40 °C to +85 °C, V_{DD} = 5.0 V ± 5%, V_{SS} = 0.0 V.

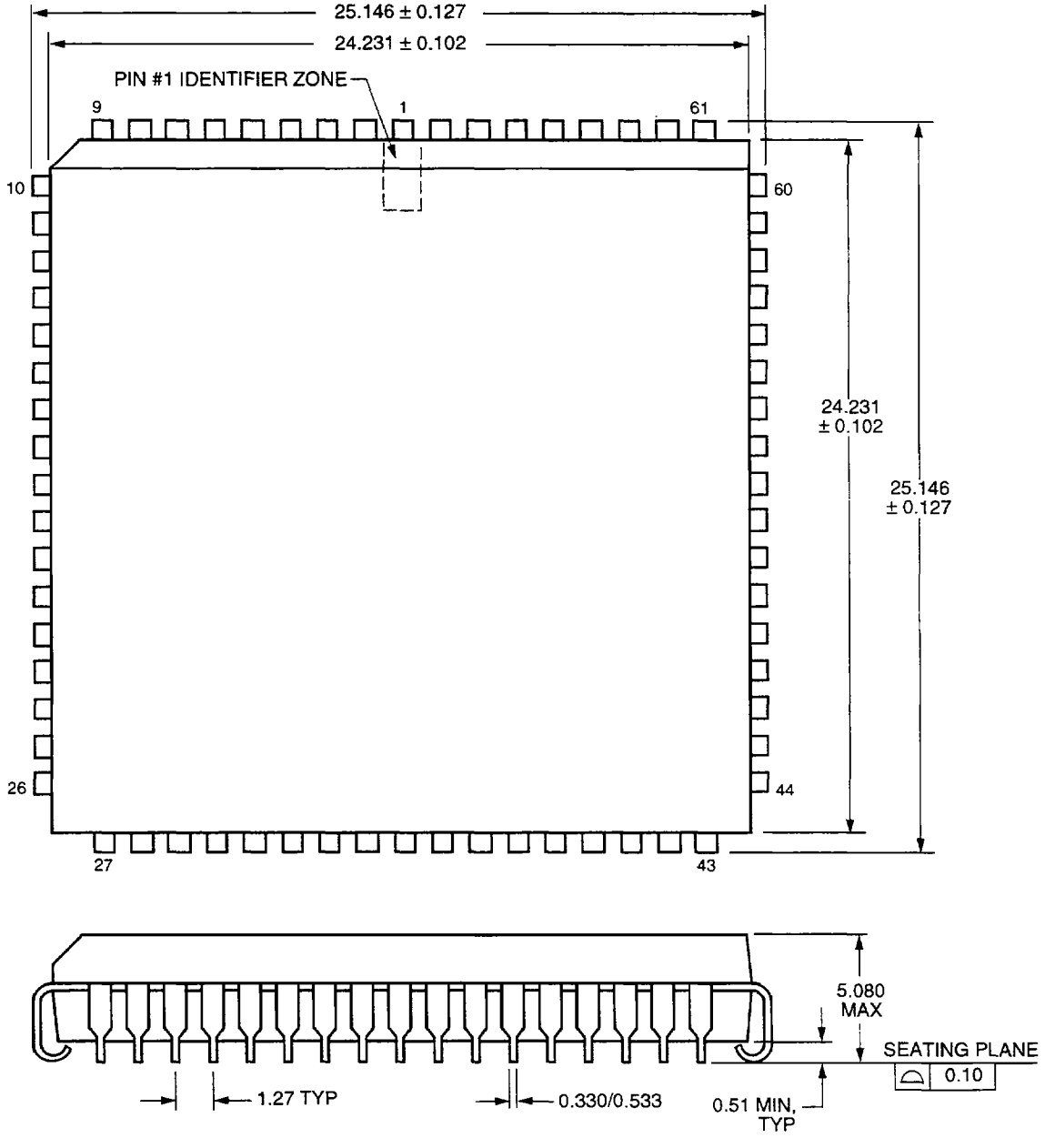
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Current:					
Non-pull-up Pins	I_{IN}	–0.25 V ≤ V_{IN} ≤ V_{DD} + 0.25 V	–10	10	mA
Pull-up Pins	I_{INU}	V_{IN} = 0 V	–120	20	mA
Non-pull-up Pins (I/O)	I_{IN}	–0.25 V ≤ V_{IN} ≤ V_{DD} + 0.25 V	–70	70	mA
Output 3-state Current	I_{OZ}	–0.25 V ≤ V_O ≤ V_{DD} + 0.25 V	–60	60	mA
Input Voltage:					
High	V_{IH}	—	2.1	—	V
Low	V_{IL}	—	—	0.8	V
Output Voltage:					
Low	V_{OL}	–4.5 mA on all pins except: –11.0 mA (INT, RDY_$\overline{\text{DTACK}}$, DXA, DXB), –13.1 mA (D0—D7)	—	0.4	V
High	V_{OH}	5.8 mA on all pins except: 15.2 mA (INT, RDY_$\overline{\text{DTACK}}$, DXA, DXB), 19.4 mA (D0—D7)	V_{DD} – 0.5	—	V
Power Dissipation	P_D	50 pF on all outputs except 100 pF on DXA, DXB, and D0—D7	—	750	mW

Note: All timing characteristics are specified in the timing figures throughout the document. All timing parameters are minimum timing specifications. There are no maximum times.

Outline Diagrams

68-Pin PLCC

Dimensions are in millimeters.



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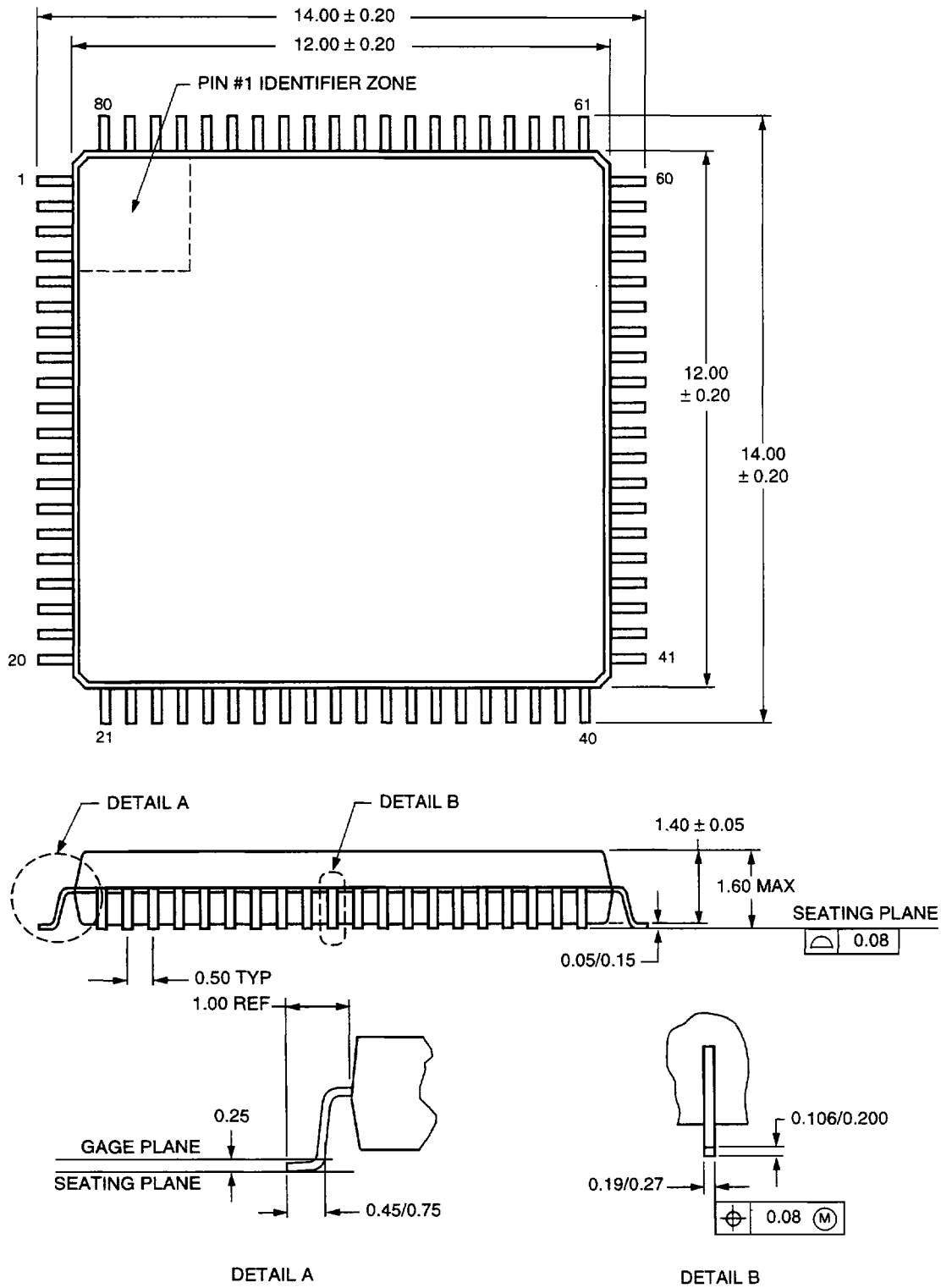
Outline Diagrams (continued)

80-Pin TQFP

Dimensions are in millimeters.



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Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T7230A - - ML	68-Pin PLCC	–40 °C to +85 °C	107394652
T7230A - - TL	80-Pin TQFP	–40 °C to +85 °C	107841454

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Notes

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