

# DATA SHEET

**74LV03**

Quad 2-input NAND gate

Product data  
Supersedes data of 1998 Apr 20

2003 Mar 03

# Quad 2-input NAND gate

# 74LV03

## FEATURES

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for Low Voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce) < 0.8 V @  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot) > 2 V @  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Level shifter capability
- Output capability: standard (open drain)
- $I_{CC}$  category: SSI

## DESCRIPTION

The 74LV03 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2-input NAND function.

The 74LV03 has open-drain N-transistor outputs, which are not clamped by a diode connected to  $V_{CC}$ . In the OFF-state, i.e., when one input is LOW, the output may be pulled to any voltage between GND and  $V_{Omax}$ . This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PZL}/t_{PLZ}$	Propagation delay nA, nB to nY	$C_L = 15$ pF $V_{CC} = 3.3$ V	8	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	Notes 1, 2	4	pF

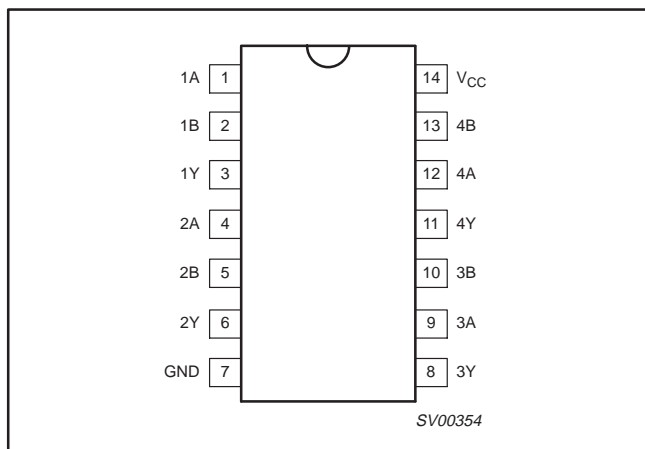
### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W)  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 N = the number of outputs switching;  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = GND$  to  $V_{CC}$
- The given value of  $C_{PD}$  is obtained with :  $C_L = 0$  pF and  $R_L = \infty$

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
14-Pin Plastic SO	-40 °C to +125 °C	74LV03D	SOT108-1

## PIN CONFIGURATION



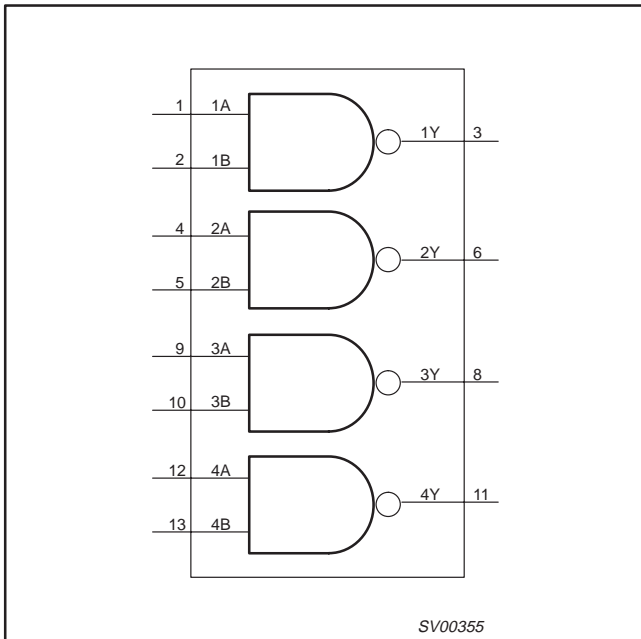
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0 V)
14	$V_{CC}$	Positive supply voltage

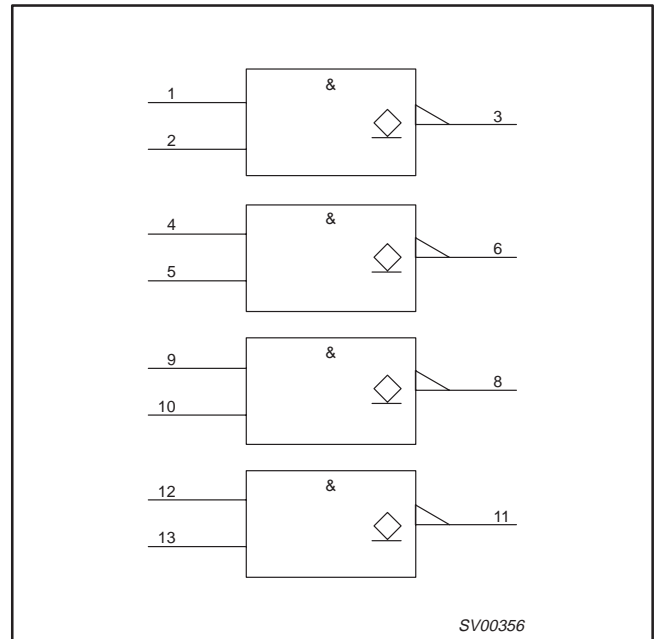
# Quad 2-input NAND gate

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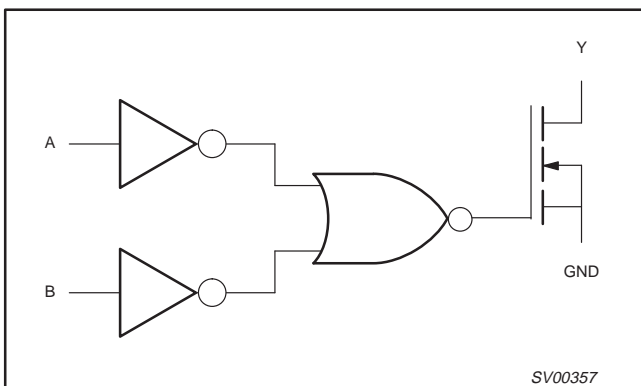
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

**NOTES:**  
 H = HIGH voltage level  
 L = LOW voltage level  
 Z = High impedance OFF-state

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0 \text{ V to } 2.0 \text{ V}$	–	–	500	ns/V
		$V_{CC} = 2.0 \text{ V to } 2.7 \text{ V}$	–	–	200	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	–	–	100	
		$V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$	–	–	50	

## NOTES:

- 1 The LV is guaranteed to function down to  $V_{CC} = 1.0 \text{ V}$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 5.5 \text{ V}$ .

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5 \text{ or } V_I > V_{CC} + 0.5 \text{ V}$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5 \text{ or } V_O > V_{CC} + 0.5 \text{ V}$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with –standard outputs		50	mA
$T_{stg}$	Storage temperature range		–65 to +150	°C
$P_{TOT}$	Power dissipation per package –plastic mini-pack (SO)	for temperature range: –40 °C to +125 °C above +70 °C derate linearly with 8 mW/K	500	mW

## NOTES:

- 1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**DC CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	0.9			0.9		V
		V <sub>CC</sub> = 2.0 V	1.4			1.4		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0			2.0		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7*V <sub>CC</sub>			0.7*V <sub>CC</sub>		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V			0.3		0.3	V
		V <sub>CC</sub> = 2.0 V			0.6		0.6	
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V			0.3*V <sub>CC</sub>		0.3*V <sub>CC</sub>	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100 μA		1.2				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100 μA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100 μA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100 μA	2.8	3.0		2.8		
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100 μA	4.3	4.5		4.3		
V <sub>OH</sub>	HIGH level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 6 mA	2.40	2.82		2.20		V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 12 mA	3.60	4.20		3.50		
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA		0	0.2		0.2	
V <sub>OL</sub>	LOW level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6 mA		0.25	0.40		0.50	V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12 mA		0.35	0.55		0.65	
I <sub>oz</sub>	HIGH level output leakage current	V <sub>CC</sub> = 2.0 V to 3.6 V; V <sub>I</sub> = V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND			5.0		10	μA
I <sub>oz</sub>	HIGH level output leakage current	V <sub>CC</sub> = 2.0 V to 3.6 V; V <sub>I</sub> = V <sub>IL</sub> ; V <sub>O</sub> = 6.0 V <sup>2</sup>			10		20	μA
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	μA
I <sub>CC</sub>	Quiescent supply current; SSI	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V			500		850	μA

**NOTES:**

- All typical values are measured at T<sub>amb</sub> = 25 °C.
- The maximum operating output voltage (V<sub>O(max)</sub>) is 6.0 V.

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## AC CHARACTERISTICS FOR 74LV03

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 1$  k $\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT	
			V <sub>CC</sub> (V)	MIN	TYP <sup>1</sup>	MAX	MIN		MAX
t <sub>PZL</sub> /t <sub>PLZ</sub>	Propagation delay nA, nB, to nY	Figures, 1, 2	1.2	-	50	-	-	ns	
			2.0	-	17	26	-		31
			2.7	-	13	19	-		23
			3.0 to 3.6	-	10 <sup>2</sup>	16	-		19
			4.5 to 5.5	-	- <sup>3</sup>	13	-		16

**NOTE:**

- 1 Unless otherwise stated, all typical values are at T<sub>amb</sub> = 25 °C.
- 2 Typical value measured at V<sub>CC</sub> = 3.3 V.
- 3 Typical value measured at V<sub>CC</sub> = 5.0 V.

## AC WAVEFORMS

V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V ≤ 3.6 V  
 V<sub>M</sub> = 0.5 V \* V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V and ≥ 4.5 V  
 V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.  
 V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V and ≤ 3.6 V  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 \* V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V and ≥ 4.5 V

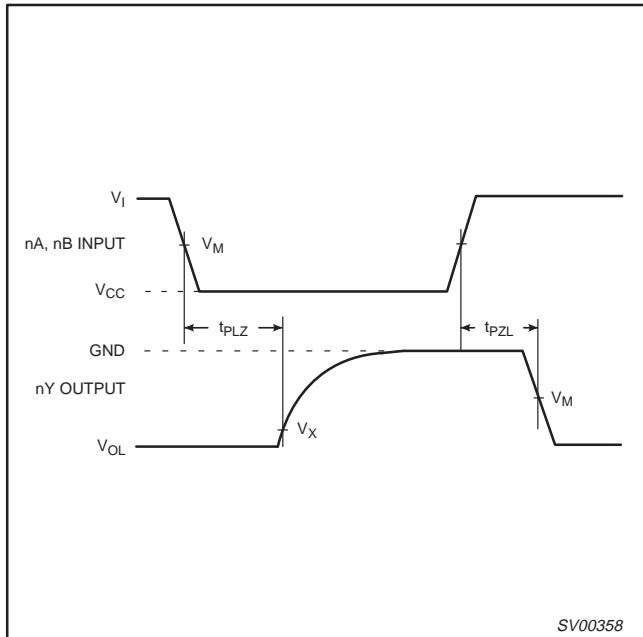


Figure 1. Input (nA, nB) to output (nY) propagation delays.

## TEST CIRCUIT

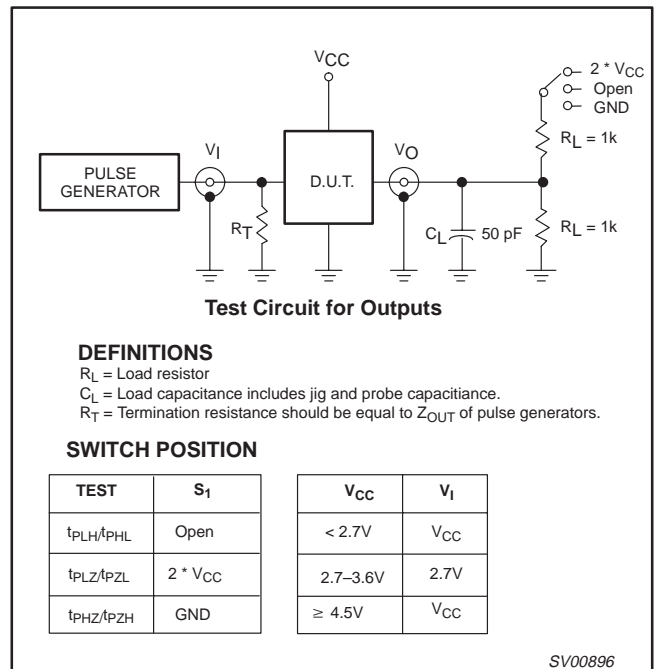


Figure 2. Load circuitry for switching times

## Quad 2-input NAND gate

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## REVISION HISTORY

Rev	Date	Description
_3	20030303	<b>Product data (9397 750 11191). ECN 853-1963 29494 of 07 February 2003. Supersedes data of 1998 Apr 20 (9397 750 04403).</b> Modifications: <ul style="list-style-type: none"> <li>• Delete DIL, SSOP and TSSOP package ordering and package outlines (discontinued options).</li> <li>• Correct power dissipation formula.</li> </ul>
_2	19980420	<b>Product specification (9397 750 04403). ECN 853-1963 19257 of 20 April 1998. Supersedes data of 1997 Mar 28.</b>

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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# 74LV03; Quad 2-input NAND gate

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
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## Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for Low Voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V @  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  Cel
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V @  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  Cel
- Level shifter capability
- Output capability: standard (open drain)
- $I_{CC}$  category: SSI








## ❑ Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74LV03	Quad 2-input NAND gate	3/3/2003	Product specification	7	58	 <a href="#">Download</a>


## ❑ Parametrics

<u>Type number</u>	<u>Package</u>	<u>Description</u>	<u>Propagation Delay(ns)</u>	<u>Voltage</u>	<u>No. of Pins</u>	<u>Power Dissipation Considerations</u>	<u>Logic Switching Levels</u>	<u>Output Drive Capability</u>
74LV03D	<a href="#">SOT108-1</a> (SO14)	Quad 2-Input NAND Gate with Level Shift Capability	15	Low	14	Low Power or Battery Applications	TTL	Low

## ❑ Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u>  <a href="#">IC packing info</a>	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
74LV03D	74LV03D	9351 758 20112	Standard Marking * Tube	<a href="#">SOT108-1</a> (SO14)	Full production	 <a href="#">Order this</a> 
	74LV03D-T	9351 758 20118	Standard Marking * Reel Pack, SMD, 13"	<a href="#">SOT108-1</a> (SO14)	Full production	 <a href="#">Order this</a> 

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