HARRIS SEMICONDUCTOR

# CD74HCT258

## High Speed CMOS Logic Quad 2-Input Multiplexer with Three-State Inverting Outputs

November 1997

### Features

- Buffered Inputs
- Typical Propagation Delay = 7ns at $V_{CC}$ =5V, $C_L$ = 15pF, $T_A$ = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$

### Description

The Harris CD74HCT258 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select Input (S). The Output Enable input ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are in the high impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 258. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

### Ordering Information

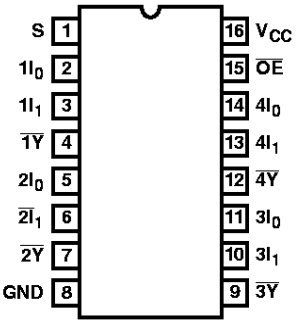
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD74HCT258E | -55 to 125 | 16 Ld PDIP | E16.3 |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout

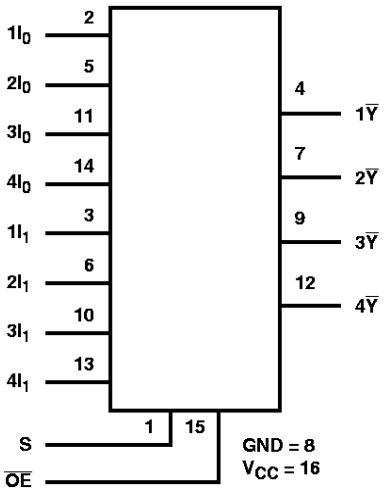
CD74HCT258
(PDIP)
TOP VIEW






File Number 1775.1

## Functional Diagram




**TRUTH TABLE**

| OUTPUT ENABLE | SELECT INPUT | DATA INPUTS | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance, OFF State

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Drain Current, per Output, $I_O$
For -0.5V < $V_O$ < $V_{CC}$ + 0.5V. . . . . ±35mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±70mA

## Operating Conditions

Temperature Range, $T_A$ . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Thermal Resistance (Typical, Note 3) $\theta_{JA}$ (°C/W)
PDIP Package . . . . . 100
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4) | $\Delta I_{CC}$ | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | - | 5.5 | - | - | ±0.5 | - | ±5 | - | ±10 | µA |

NOTE:

4. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| Data | 0.5 |
| S | 1.5 |
| $\overline{OE}$ | 1.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

### Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| Propagation Delay In to $\overline{Y}$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 27 | 34 | 41 | ns |
| | | $C_L$ = 15pF | 5 | 11 | - | - | - | ns |
| Propagation Delay S to $\overline{Y}$ | $t_{PZL}$, $t_{PZH}$ | $C_L$ = 50pF | 4.5 | - | 34 | 43 | 51 | ns |
| | | $C_L$ = 15pF | 5 | 14 | - | - | - | ns |
| Propagation Delay $\overline{OE}$ to $\overline{Y}$ | $t_{PZL}$, $t_{PZH}$ | $C_L$ = 50pF | 4.5 | - | 28 | 35 | 42 | ns |
| | | $C_L$ = 15pF | 5 | 11 | - | - | - | ns |
| Propagation Delay $\overline{OE}$ to $\overline{Y}$ | $t_{PLZ}$, $t_{PHZ}$ | $C_L$ = 50pF | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 12 | 15 | 18 | ns |
| Input Capacitance | $C_I$ | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | $C_O$ | - | - | - | 20 | 20 | 20 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | $C_{PD}$ | - | 5 | 49 | - | - | - | pF |

NOTES:

5. $C_{PD}$ is used to determine the dynamic power consumption, per multiplexer.
6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## *Test Circuits and Waveforms*

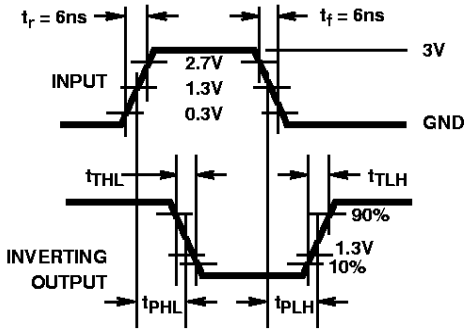



FIGURE 1. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

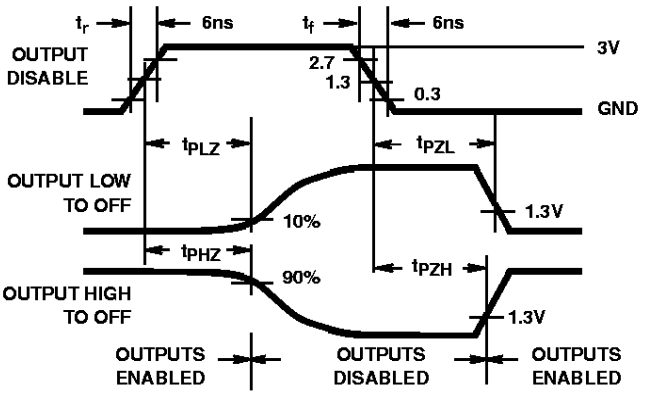
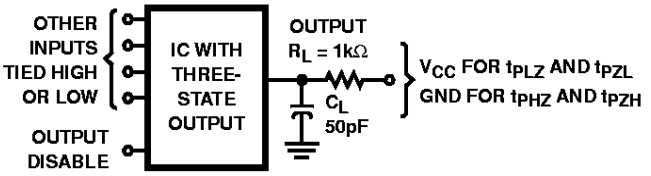



FIGURE 2. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

## Test Circuits and Waveforms (Continued)




NOTE: Open drain waveforms $t_{PLZ}$ and $t_{PZL}$ are the same as those for three-state shown on the left. The test circuit is Output $R_L$ = 1kΩ to $V_{CC}$, $C_L$ = 50pF.

**FIGURE 3. HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT**

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.



## Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

**NORTH AMERICA**
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

**EUROPE**
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

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