



# FDMC7664

## N-Channel PowerTrench<sup>®</sup> MOSFET

30 V, 18.8 A, 4.2 mΩ

### Features

- Max  $r_{DS(on)}$  = 4.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 18.8$  A
- Max  $r_{DS(on)}$  = 5.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 16.1$  A
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

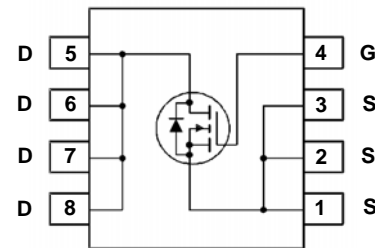
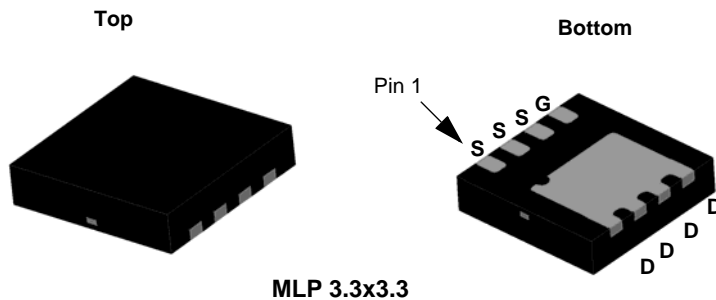


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Applications

- DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		30	V
$V_{GS}$	Gate to Source Voltage		±20	V
$I_D$	Drain Current	-Continuous $T_C = 25$ °C	24	A
		-Continuous $T_A = 25$ °C (Note 1a)	18.8	
		-Pulsed	60	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	188	mJ
$P_D$	Power Dissipation	$T_C = 25$ °C	45	W
		$T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7664	FDMC7664	MLP 3.3x3.3	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 18.8\text{ A}$		3.6	4.2	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 16.1\text{ A}$		4.5	5.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 18.8\text{ A}$ $T_J = 125\text{ }^\circ\text{C}$		4.4	5.4	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 18.8\text{ A}$		115		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$		3655	4865	pF
$C_{oss}$	Output Capacitance			1100	1465	pF
$C_{rss}$	Reverse Transfer Capacitance			115	170	pF
$R_g$	Gate Resistance			0.8	2.2	$\Omega$

### Switching Characteristics

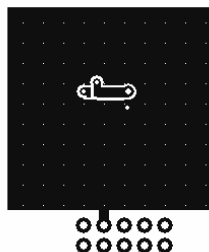
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 18.8\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		15	27	ns	
$t_r$	Rise Time			7	14	ns	
$t_{d(off)}$	Turn-Off Delay Time			37	59	ns	
$t_f$	Fall Time			6	12	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		55	76	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 15\text{ V}$ $I_D = 18.8\text{ A}$		25	34	nC
$Q_{gs}$	Gate to Source Charge				12		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				6		nC

### Drain-Source Diode Characteristics

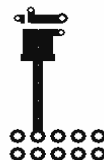
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 18.8\text{ A}$ (Note 2)		0.83	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.71	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 18.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		41	65	ns
$Q_{rr}$	Reverse Recovery Charge			20	35	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3.  $E_{AS}$  of 188 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 19.4\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

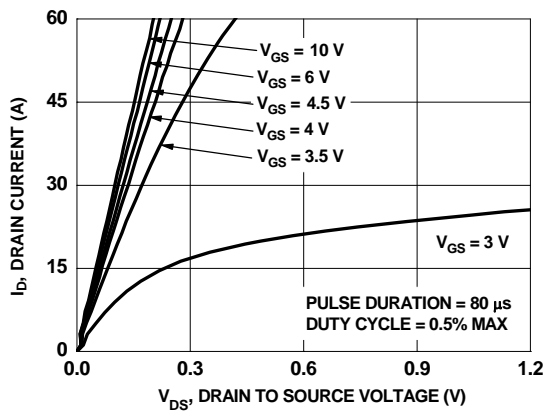


Figure 1. On Region Characteristics

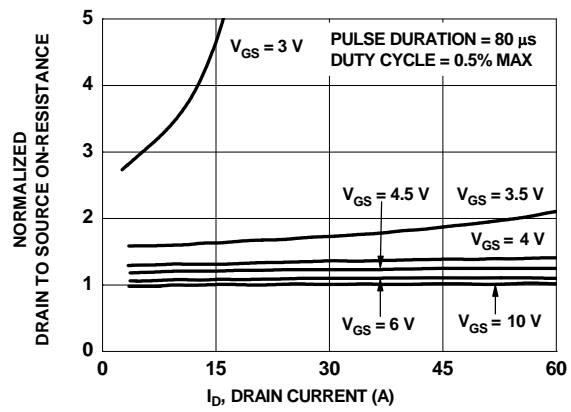


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

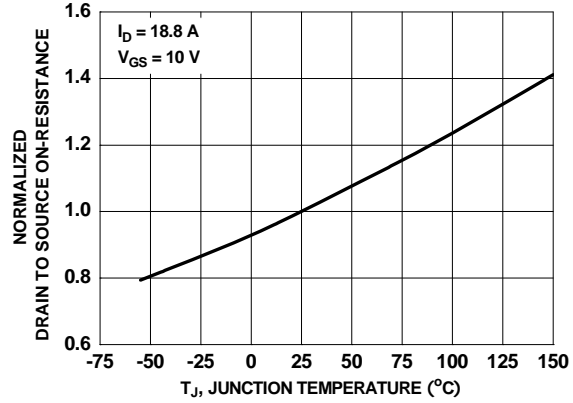


Figure 3. Normalized On Resistance vs. Junction Temperature

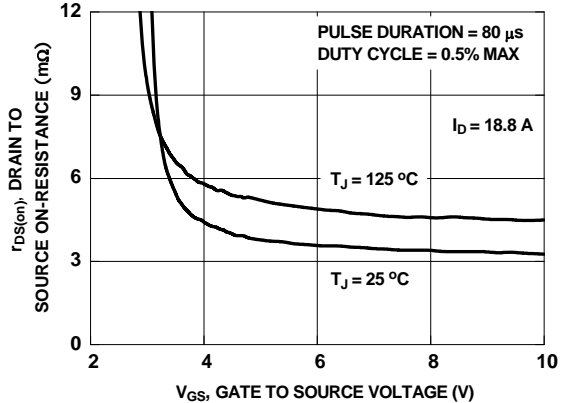


Figure 4. On-Resistance vs. Gate to Source Voltage

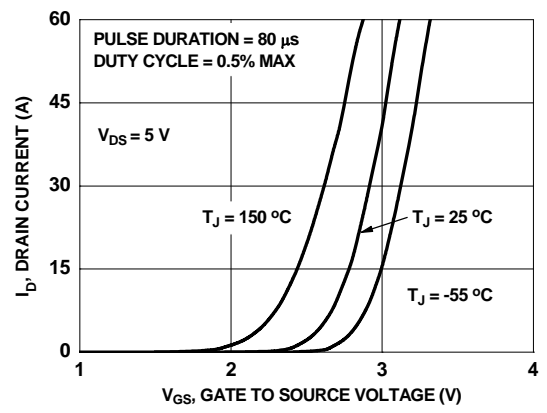


Figure 5. Transfer Characteristics

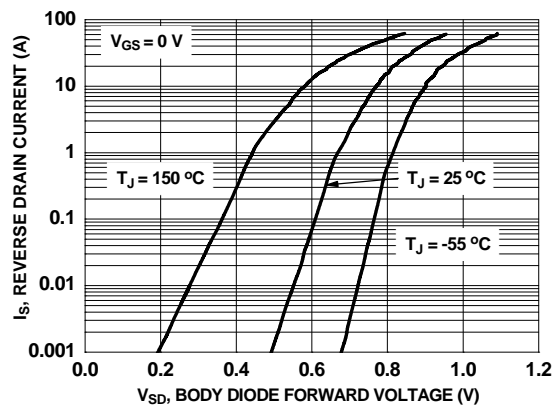
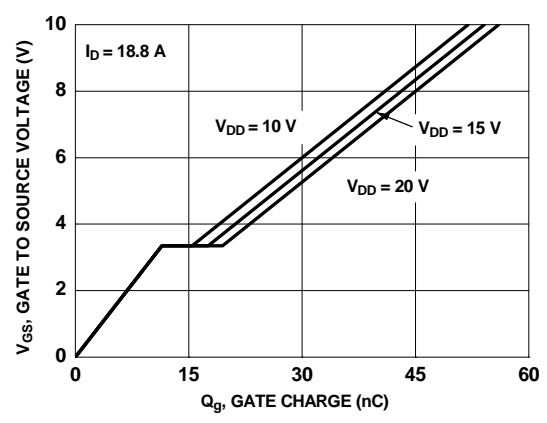
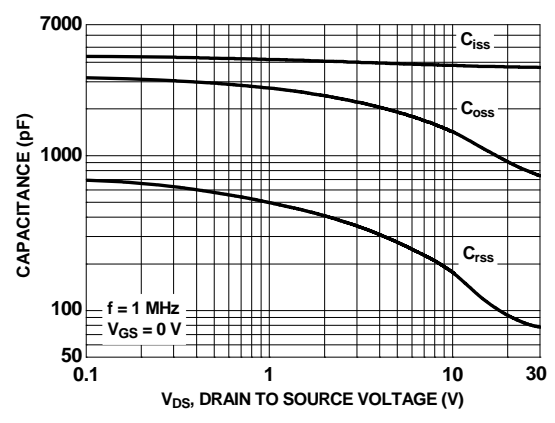


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

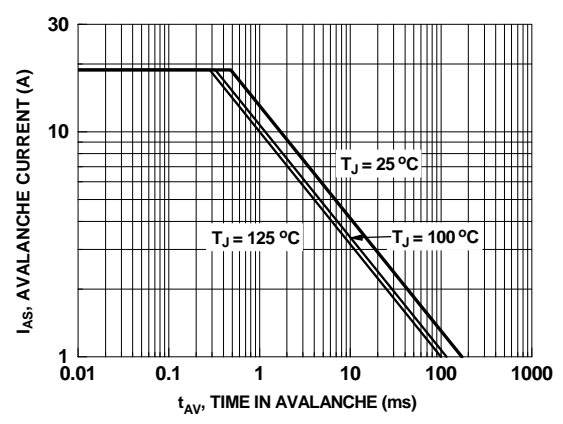
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



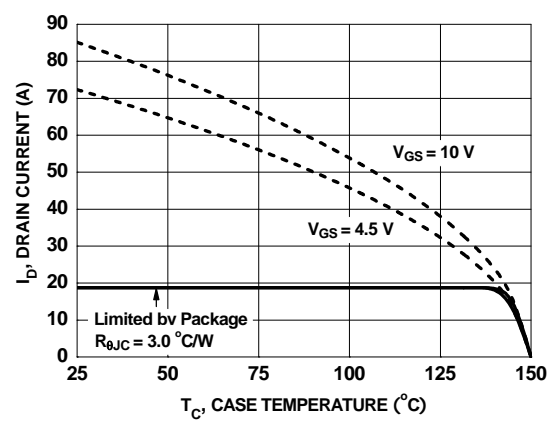
**Figure 7. Gate Charge Characteristics**



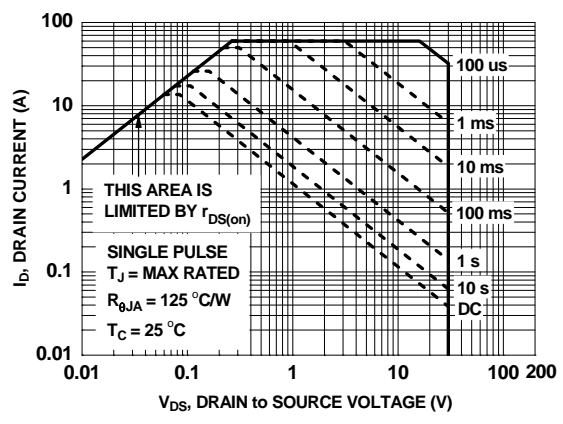
**Figure 8. Capacitance vs. Drain to Source Voltage**



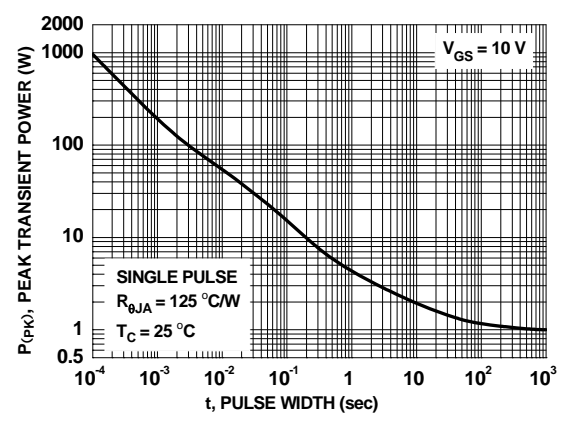
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

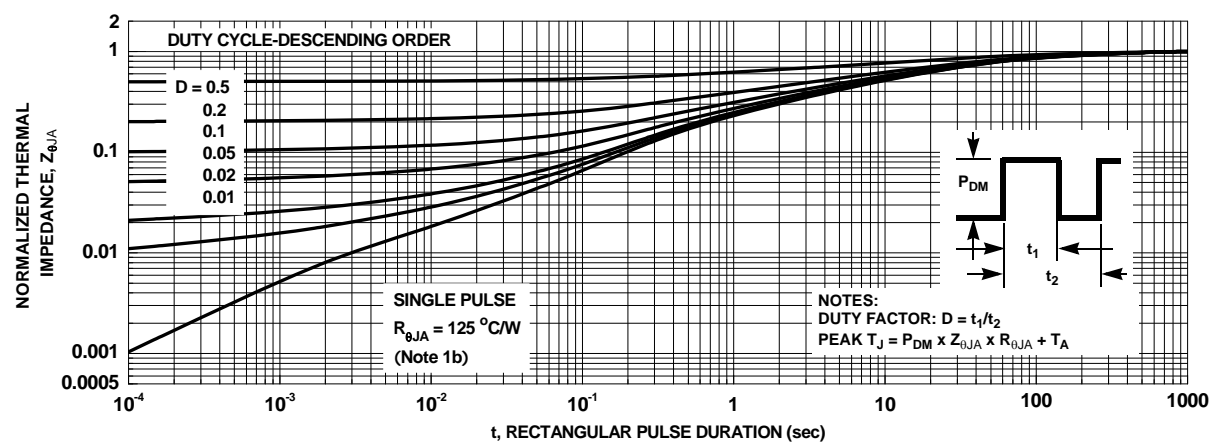


**Figure 11. Forward Bias Safe Operating Area**



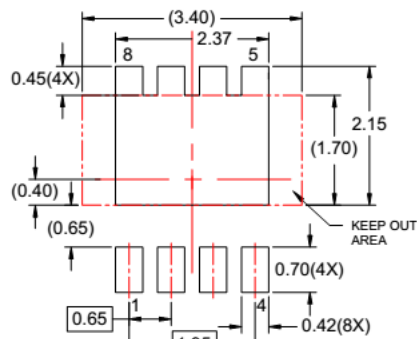
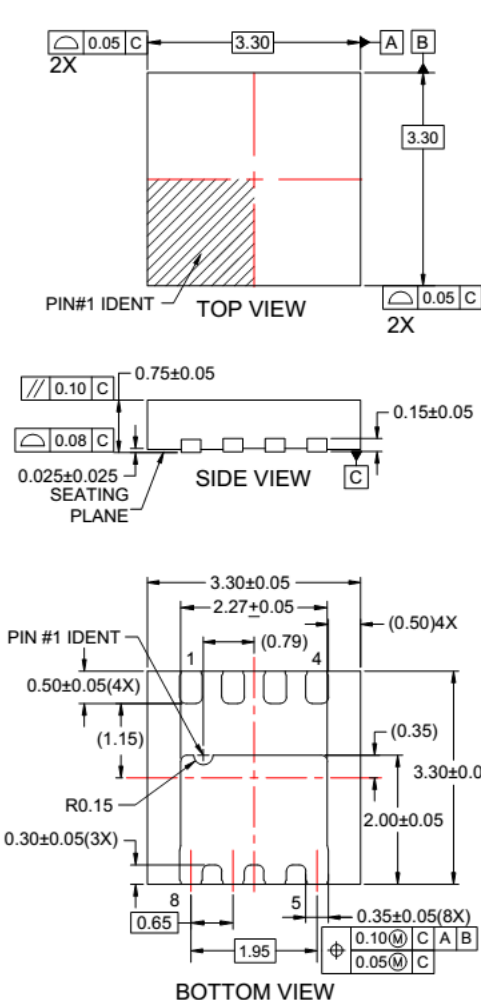
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.







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