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LP3947
USB/AC Adaptor, Single Cell Li-Ion Battery Charger IC

General Description

The LP3947 is a complete charge management system that safely charges and maintains a Li-Ion battery from either USB power source or AC adaptor. In USB mode, the LP3947 supports charging in low power or high power mode. Alternatively, the LP3947 can take charge from AC adaptor. In both USB and AC adaptor modes, charge current, battery regulation voltage, and End of Charge (EOC) point can be selected via I^2C interface. The LP3947 can also operate on default values that are pre-programmed in the factory. The battery temperature is monitored continuously at the Ts pin to safeguard against hazardous charging conditions. The charger also has under-voltage and over-voltage protection as well as an internal 5.6 hr timer to protect the battery. The pass transistor and charge current sensing resistor are all integrated inside the LP3947.

The LP3947 operates in four modes: pre-qualification, constant current, constant voltage and maintenance modes. There are two open drain outputs for status indication. An internal amplifier readily converts the charge current into a voltage. Also, the charger can operate in an LDO mode providing a maximum of 1.2 Amp to the load.

Features

- Supports USB Charging Scheme
- Integrated Pass Transistor
- Near-Depleted Battery Preconditioning
- Monitors Battery Temperature
- Built-In 5.6 hour timer
- Under Voltage and Over Voltage Lockout
- Charge Status Indicators
- Charge Current Monitor Analog Output
- LDO Mode Operation can source 1 Amp
- Continuous Over Current/Temperature Protection

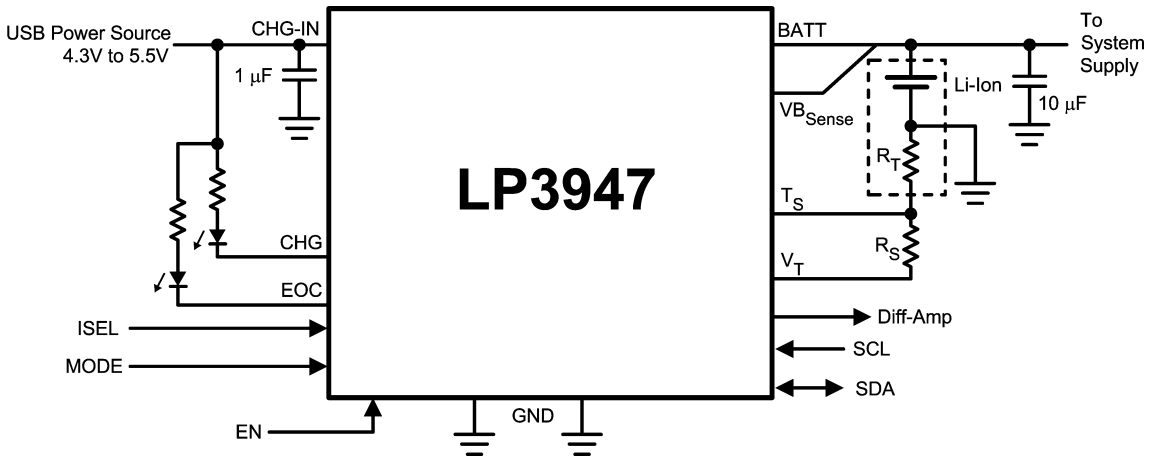
Key Specifications

- 1% Charger Voltage Accuracy Over $0^\circ C \le T_J \le 85^\circ C$
- 4.3V to 6.0V Input Voltage Range
- 100 mA to 750 mA charge current range, in charger mode
- 100mA to 500mA charge current range, in USB mode
- LLP Package Power Dissipation: 2.7W at $T_A = 25^\circ C$

Applications

- Cellular Phones
- PDAs
- Digital Cameras
- USB Powered Devices
- Programmable Current Sources

Typical Application Circuit



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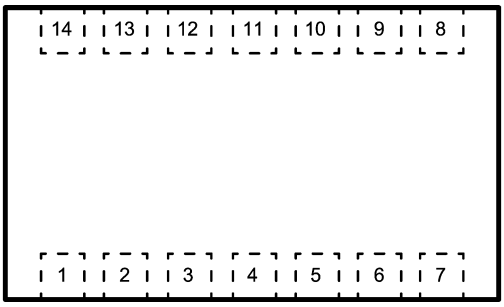
More Application Circuit can be found in the Application Note section.

Connection Diagrams and Package Mark Information



(Top View)
See NS Package Number SDA14B

Pin Descriptions

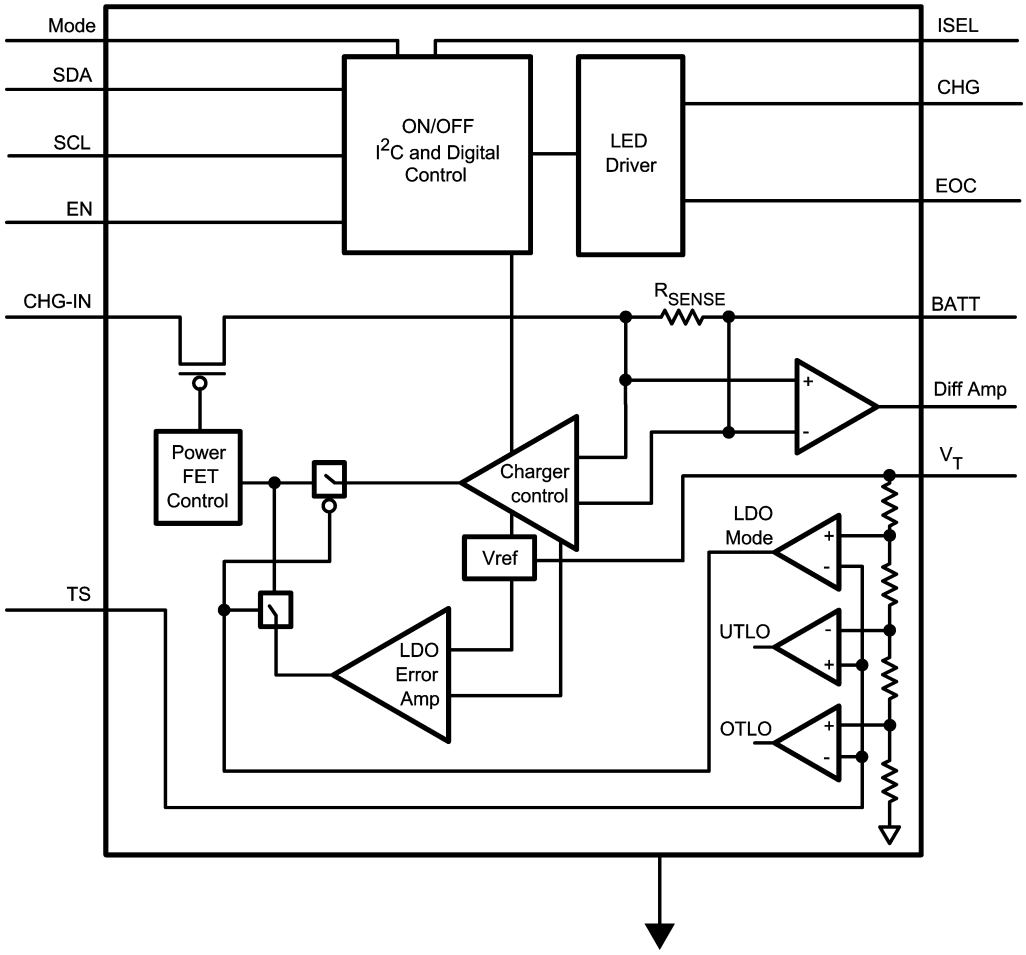
Pin #	Name	Description
1	EN	Charger Enable Input. Internally pulled high to CHG-IN pin. A HIGH enables the charger and a LOW disables the charger.
2	SCL	I^2C serial Interface Clock input.
3	SDA	I^2C serial Interface Data input/out.
4	BATT	Battery supply input terminal. Must have 10 µF ceramic capacitor to GND
5	V_T	Regulated 2.78V output used for biasing the battery temperature monitoring thermistor.
6	VB_{SENSE}	Battery Voltage Sense connected to the positive terminal of the battery.
7	MODE	Select pin between AC adaptor and USB port. A LOW sets the LP3947 in USB port and a HIGH sets it in the AC adaptor.
8	Diff-Amp	Charge current monitoring differential amplifier output. Voltage output representation of the charge current.
9	Ts	Multi function pin. Battery temperature monitoring input and LDO/Charger mode. Pulling this pin to V_T, or removing the thermistor by physically disconnecting the battery, sets the device in LDO mode.
10	EOC	Active Low Open Drain Output. Active when USB port or AC adaptor is connected and battery is fully charged. For more information, refer to “LED Charge Status Indicators” section.
11	GND	Ground
12	CHG	Active Low Open Drain Output. Active when USB port or AC adaptor is connected and battery is being charged. For more information, refer to “LED Charge Status Indicators” section.
13	ISEL	Control pin to switch between low power (100 mA) mode and high power (500 mA) mode in USB mode. This pin is pulled high internally as default to set the USB in 100 mA mode. This pin has to be externally pulled low to go into 500 mA mode.
14	CHG-IN	Charger input from a regulated, current limited power source. Must have a 1 µF ceramic capacitor to GND

Ordering Information

LP3947 Supplied as 1000 Units, Tape and Reel	LP3947 Supplied as 4500 Units Tape and Reel	Default Options*	Package Marking
LP3947ISD-09	LP3947ISDX-09	I_{CHG} = 500 mA V_{BATT} = 4.1V EOC = 0.1C	L00061B
LP3947ISD-51	LP3947ISDX-51	I_{CHG} = 500 mA V_{BATT} = 4.2V EOC = 0.1C	L00062B

*Other default options are available. Please contact National Semiconductor sales office/distributors for availability and specifications.

LP3947 Functional Block Diagram



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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

CHG-IN	−0.3V to +6.5V
All pins except GND and CHG-IN (Note 3)	−0.3V to +6V
Junction Temperature	150˚C
Storage Temperature	−40˚C to +150˚C
Power Dissipation (Note 4)	1.89W
ESD (Note 5)	
Human Body Model	2 kV
Machine Model	200V

Operating Ratings (Notes 1, 2)

CHG-IN	0.3V to 6.5V
EN, ISEL, MODE, SCL, SDA, V_T (Note 3)	0V to 6V
Junction Temperature	−40˚C to +125˚C
Operating Temperature	−40˚C to +85˚C
Thermal Resistance θ_{JA}	37˚C/W
Maximum Power Dissipation (Note 6)	1.21W

Electrical Characteristics

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V, C_{CHG-IN} = 1 µF, C_{BATT} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{CC} SUPPLY						
V_{CHG-IN}	Input Voltage Range			**4.5**	**6**	V
V_{USB}				**4.3**	**6**	
I_{CC}	Quiescent Current	$V_{CHG-IN} \leq 4V$	2		**20**	µA
		EOC = Low, adaptor connected, V_{BATT} = 4.1V	50		**150**	
$V_{OK-TSHD}$	Adaptor OK Trip Point (CHG-IN)	$V_{CHG-IN} - V_{BATT}$ (Rising)	60			mV
		$V_{CHG-IN} - V_{BATT}$ (Falling)	50			mV
$V_{UVLO-TSHD}$	Under Voltage Lock-Out Trip Point	V_{CHG-IN} (Rising)	3.95	**3.6**	**4.3**	V
		V_{CHG-IN} (Falling)	3.75	**3.4**	**4.1**	V
$V_{OVLO-TSHD}$	Over Voltage Lock-Out Trip Point	V_{CHG-IN} (Rising)	5.9			V
		V_{CHG-IN} (Falling)	5.7			
	Thermal Shutdown Temperature	(Note 8)	160			˚C
	Thermal Shutdown Hysteresis		20			
BATTERY CHARGER						
I_{CHG}	Fast Charge Current Range	ISEL = High, In USB Mode	100			mA
		ISEL = Low, In USB Mode	500			
		In AC Adaptor Mode		**100**	**750**	
	Fast Charge Current Accuracy	I_{CHARGE} = 100 mA or 150 mA		**−20**	**+20**	mA
		$I_{CHARGE} \geq$ 200 mA		**−10**	**+10**	%
$I_{PRE-CHG}$	Pre-Charge Current	V_{BATT} = 2V		**45**	**70**	mA
I_{EOC}	End of Charge Current Accuracy	100 mA to 450 mA, 0.1C EOC Only (Note 10)		**−10**	**+10**	mA
		500 mA to 750 mA, All EOC Points		**−20**	**+20**	%
V_{BATT}	Battery Regulation Voltage (For 4.1V Cell)	T_J = 0˚C to +85˚C	4.1	**4.059**	**4.141**	V
		T_J = −40˚C to +85˚C	4.1	**4.038**	**4.162**	
	Battery Regulation Voltage (For 4.2V Cell)	T_J = 0˚C to +85˚C	4.1	**4.158**	**4.242**	
		T_J = −40˚C to +85˚C	4.2	**4.137**	**4.263**	
V_{CHG-Q}	Full Charge Qualification Threshold	V_{BATT} Rising, Transition from Pre-Charge to Full Current	3.0			V

Electrical Characteristics (Continued)

Unless otherwise noted, V_{CHG-IN} = 5V, V_{BATT} = 4V, C_{CHG-IN} = 1 µF, C_{BATT} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +85˚C. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
BATTERY CHARGER						
$V_{BAT-RST}$	Restart Threshold Voltage (For 4.1V Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qualification State	3.9	**3.77**	**4.02**	V
	Restart Threshold Voltage (For 4.2V Cell)	V_{BATT} Falling, Transition from EOC, to Pre-Qualification State	4.00	**3.86**	**4.12**	
R_{SENSE}	Internal Current Sense Resistance	(Note 8)	120			mΩ
	Internal Current Sense Resistor Load Current				**1.2**	A
$ICHG_{MON}$	Diff-Amp Output	I_{CHG} = 50 mA	0.583			V
		I_{CHG} = 100 mA	0.663			
		I_{CHG} = 750 mA	1.790			
t_{OUT}	Charger Time Out	T_J = 0˚C to 85˚C	5.625	**4.78**	**6.42**	Hrs
		T_J = −40˚C to +85˚C	5.625	**4.5**	**6.75**	
V_{OL}	Low Level Output Voltage	EOC, CHG Pins each at 9 mA	100			mV
TEMPERATURE SENSE COMPARATORS						
V_{UTLO}	Low Voltage Threshold	Voltage at Ts Pin, Rising	2.427			V
		Voltage at Ts Pin, Falling	2.369			
V_{OTLO}	High Voltage Threshold	Voltage at Ts Pin, Rising	1.470			V
		Voltage at Ts Pin, Falling	1.390			
V_{LDO}	LDO Mode Voltage Threshold	Voltage at Ts Pin, % of V_T	97			%
V_T	Voltage Output		2.787			V
LDO MODE (Ts = HIGH)						
V_{OUT}	Output Voltage Regulation	I_{LOAD} = 50 mA	4.10			V
		I_{LOAD} = 750 mA	4.06			
LOGIC LEVELS						
V_{IL}	Low Level Input Voltage	EN, ISEL, MODE			**0.4**	V
V_{IH}	High Level Input Voltage	EN, ISEL, MODE		**2.0**		V
I_{IL}	Input Current	EN, ISEL = LOW		**−10**	**+10**	µA
		MODE = LOW		**−5**	**+5**	µA
I_{IH}	Input Current	EN, ISEL, MODE = HIGH		**−5**	**+5**	µA

Electrical Characteristics, I²C Interface

Unless otherwise noted, V_{CHG-IN} = V_{DD} = 5V, V_{BATT} = 4V. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40˚C to +125˚C. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IL}	Low Level Input Voltage	SDA & SCL (Note 8)		**0.4**	**0.3 V_{DD}**	V
V_{IH}	High Level Input Voltage	SDA & SCL (Note 8)		**0.7 V_{DD}**	**V_{DD} +0.5**	V
V_{OL}	Low Level Output Voltage	SDA & SCL (Note 8)		**0**	**0.2 V_{DD}**	V
V_{HYS}	Schmitt Trigger Input Hysteresis	SDA & SCL (Note 8)		**0.1 V_{DD}**		V
F_{CLK}	Clock Frequency	(Note 8)			**400**	kHz
t_{HOLD}	Hold Time Repeated START Condition	(Note 8)		**0.6**		µs
t_{CLK-LP}	CLK Low Period	(Note 8)		**1.3**		µs
t_{CLK-HP}	CLK High Period	(Note 8)		**0.6**		µs

Electrical Characteristics, I²C Interface (Continued)

Unless otherwise noted, $V_{CHG-IN} = V_{DD} = 5V$, $V_{BATT} = 4V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J = -40^\circ C$ to $+125^\circ C$. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
t_{SU}	Set-Up Time Repeated START Condition	(Note 8)		**0.6**		µs
$t_{DATA-HOLD}$	Data Hold Time	(Note 8)		**300**		ns
$t_{DATA-SU}$	Data Set-Up Time	(Note 8)		**100**		ns
t_{SU}	Set-Up Time for STOP Condition	(Note 8)		**0.6**		µs
t_{TRANS}	Maximum Pulse Width of Spikes that must be Suppressed by the Input Filter of both DATA & CLK Signals.	(Note 8)	50			ns

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Caution must be taken to avoid raising pins EN and V_T 0.3V higher than V_{CHG-IN} and raising pins ISEL, MODE, SCL and SDA 0.3V higher than V_{BATT}.

Note 4: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula

$$P = (T_J - T_A)\theta_{JA}, \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.89W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150˚C, for T_J, 80˚C for T_A, and 37˚C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 80˚C. Less power can be dissipated safely at ambient temperatures above 80˚C. The Absolute Maximum power dissipation can be increased by 27 mW for each degree below 80˚C, and it must be de-rated by 27 mW for each degree above 80˚C.

Note 5: The human-body model is used. The human-body model is 100 pF discharged through 1.5 kΩ.

Note 6: Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 1.21W rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125˚C, for T_J, 80˚C for T_A, and 37˚C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 80˚C. Less power can be dissipated at ambient temperatures above 80˚C. The maximum power dissipation for operation can be increased by 27 mW for each degree below 80˚C, and it must be de-rated by 27 mW for each degree above 80˚C.

Note 7: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25^\circ C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 8: Guaranteed by design.

Note 9: LP3947 is not intended as a Li-Ion battery protection device, any battery used in this application should have an adequate internal protection.

Note 10: The ±10 mA limits apply to all charge currents from 100 mA to 450 mA, to 0.1C End Of Charge (EOC). The limits increase proportionally with higher EOC points. For example, at 0.2C, the End Of Charge current accuracy becomes ±20 mA.

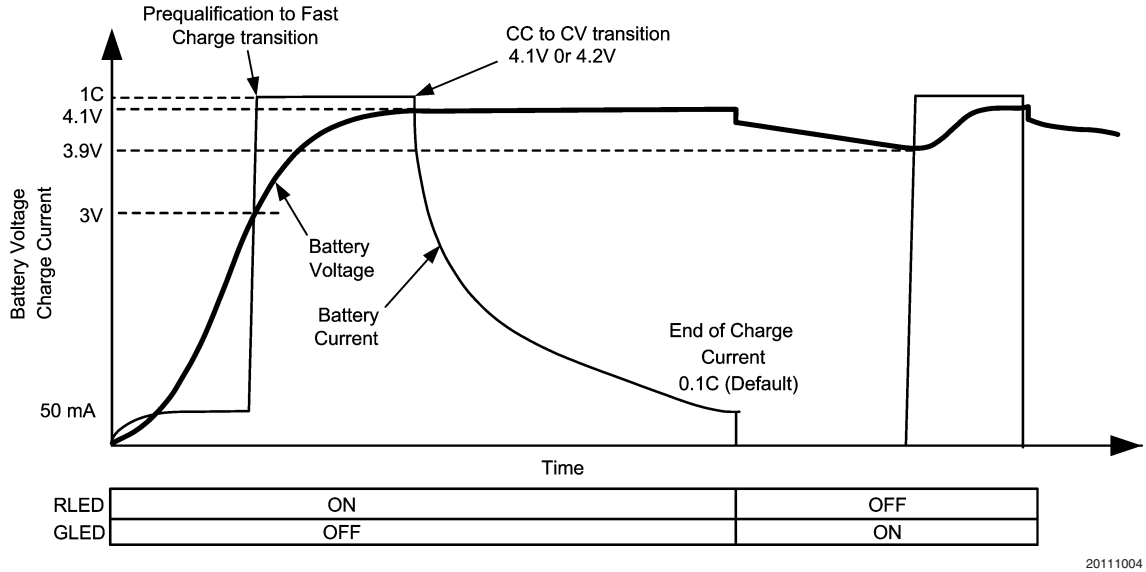


FIGURE 1. Li-Ion Charging Profile

Application Notes

LP3947 CHARGER OPERATION

The LP3947 charge cycle is initiated with AC adaptor or USB power source insertion. If the voltage on the CHG-IN pin meets under-voltage ($V_{UVLO-TSHD}$), over-voltage ($V_{OVLO-TSHD}$) requirements, and the Adaptor OK signal is detected, then pre-qualification cycle begins (see *Figure 1*). In this cycle, a safe current level, less than 70mA, is pumped into the battery while the voltage across the battery terminals is measured. Once this voltage exceeds 3.0V, the controller will initiate constant current fast charge cycle. If the CHG-IN pin is connected to an AC adaptor, the default charge current is 500 mA and I^2C interface can be used to program this parameter. If the CHG-IN pin is connected to the USB port, constant current cycle will start with a default of 100 mA. During this cycle, the 5.6 hr safety timer starts counting.

If the 5.6 hr safety timers times out during constant current cycle, charging is terminated. As the battery is charged during constant current mode, the voltage across pack terminal increases until it reaches 4.2V (or 4.1V). As soon as pack terminal reaches 4.2V (or 4.1V), the controller starts operating in constant voltage mode by applying regulated V_{BATT} voltage across the battery terminals. During this cycle, the charge current, I_{CHG}, continues to decrease with time and when it drops below 0.1C (default value), the EOC signal is activated indicating successful completion of the charge cycle. The EOC current can be programmed to 0.1C, 0.15C, or 0.2C. The default value is 0.1C. After completing the full charge cycle, the controller will start the maintenance cycle where battery pack voltage is monitored continuously. During the maintenance cycle, if the pack voltage drops 200 mV below the termination voltage, charge cycle will be initiated providing that the wall adaptor is plugged in and is alive.

Charging terminates when the battery temperature is out of range. For more explanation, please refer to “Ts Pin” section.

The LP3947 with I^2C interface allows maximum flexibility in selecting the charge current, battery regulation voltage and EOC current. The LP3947 operates in default mode during power up. See the “I^2C Interface” section for more detail.

When charging source comes from the USB port, charging starts with 100 mA (low power mode, ISEL = high). The USB controller can set the ISEL pin low to charge the battery at 500 mA. A simple external circuit selects between an AC adaptor or the USB port. The circuit is designed with priority given to the AC adaptor.

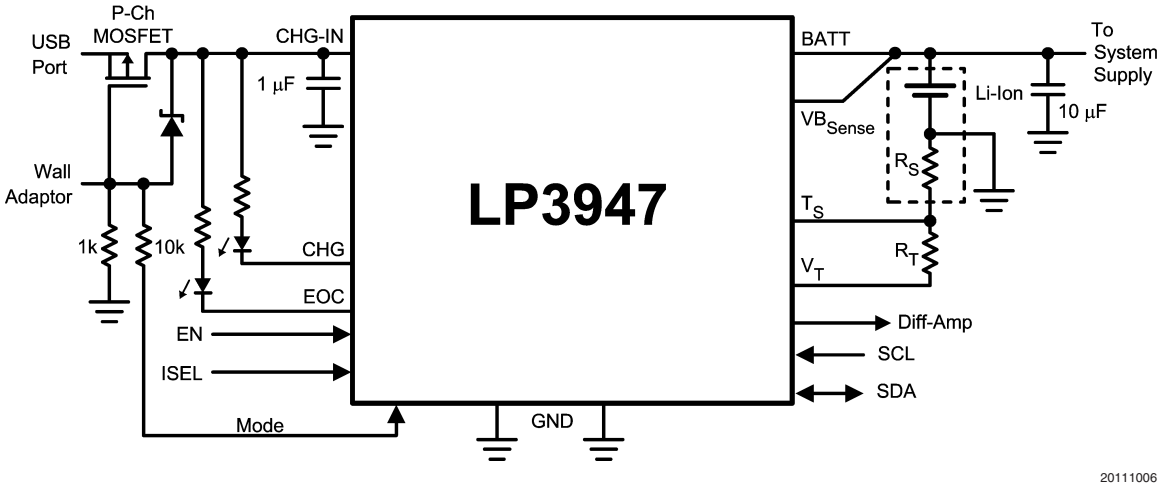


FIGURE 2. LP3947 with External Switch

Application Notes (Continued)

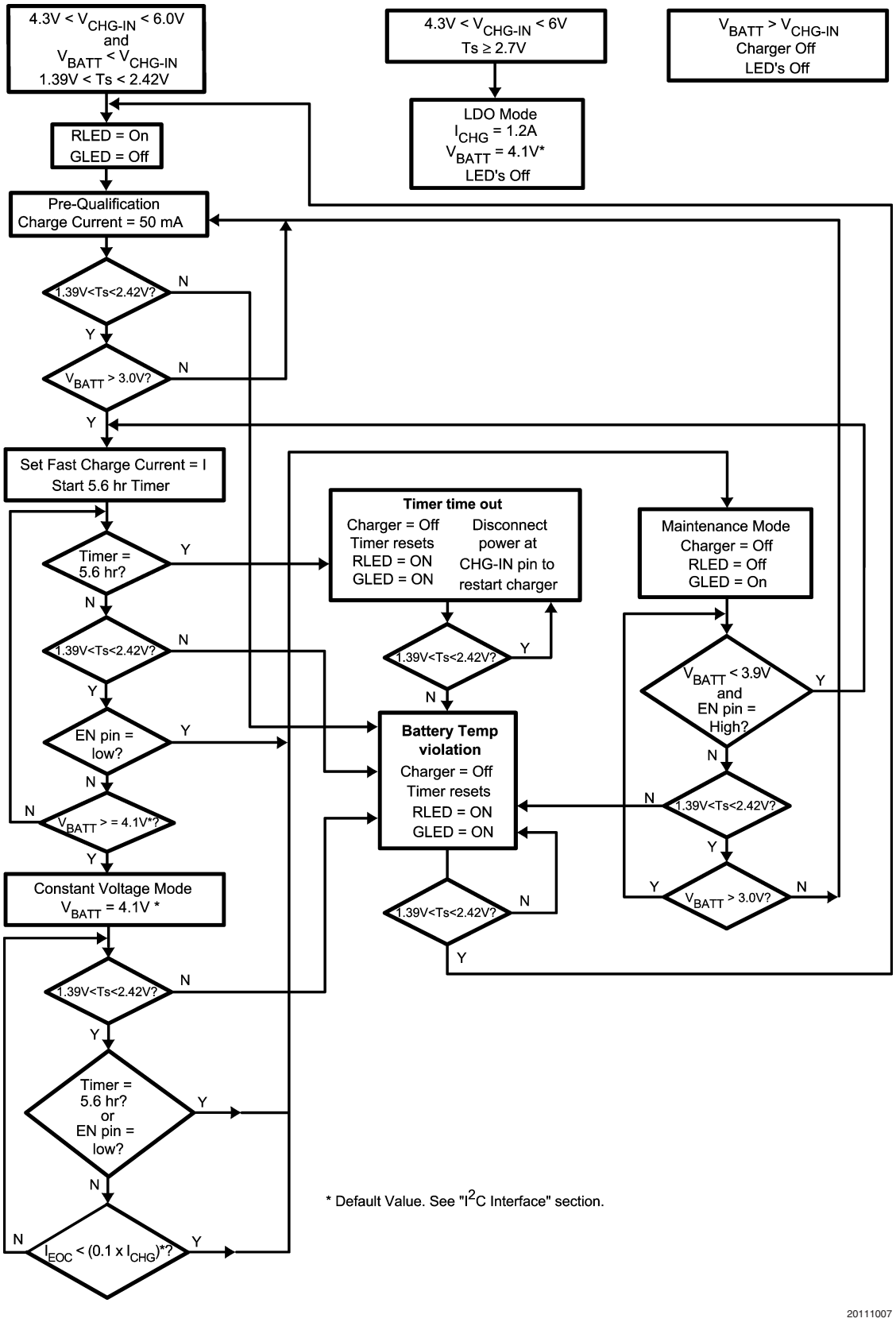


FIGURE 3. LP3947 Charger Flow Chart

Application Notes (Continued)

CHARGE CURRENT SELECTION IN CONSTANT CURRENT MODE

In the AC adaptor mode, the LP3947 is designed to provide a charge current ranging from 100 mA to 750 mA, in steps of 50 mA, to support batteries with different capacity ratings. The default value is 500 mA. No external resistor is required to set the charge current in the LP3947. In the USB mode, the LP3947 will initially charge with 100 mA (ISEL = high). By setting the ISEL pin low, charge current can be programmed to 500 mA. In addition, with ISEL = low, the charge current can be programmed to different values via the I^2C interface.

TABLE 1. Charge Current Selection in AC Adaptor/USB Mode

	MODE Pin	ISEL Pin	Functions
AC Adaptor Mode	HIGH	HIGH	ISEL polarity is irrelevant. Default 500 mA charge current. Can be reprogrammed via I^2C.
	HIGH	LOW	
USB Mode	LOW	HIGH	100 mA charge current
	LOW	LOW	Default 500 mA charge current. Can be reprogrammed via I^2C.

BATTERY VOLTAGE SELECTION

The battery voltage regulation can be set to 4.1V or 4.2V by default. Please refer to the Ordering Information table for more detail.

END OF CHARGE (EOC) CURRENT SELECTION

The EOC thresholds can be programmed to 0.1C, 0.15C or 0.2C in the LP3947. The default value is 0.1C, which provides the highest energy storage, but at the expense of longer charging time. On the other hand, 0.2C takes the least amount of charging time, but yields the least energy storage.

CHARGE CURRENT SENSE DIFFERENTIAL AMPLIFIER

The charge current is monitored across the internal 120 mΩ current sense resistor. The differential amplifier provides the analog representation of the charge current. Charge current can be calculated using the following equation:

$$I_{CHG} = \frac{(V_{DIFF} - 0.497)}{1.655}$$

Where voltage at Diff Amp output (V_{DIFF}) is in volt, and charge current (I_{CHG}) is in amps.

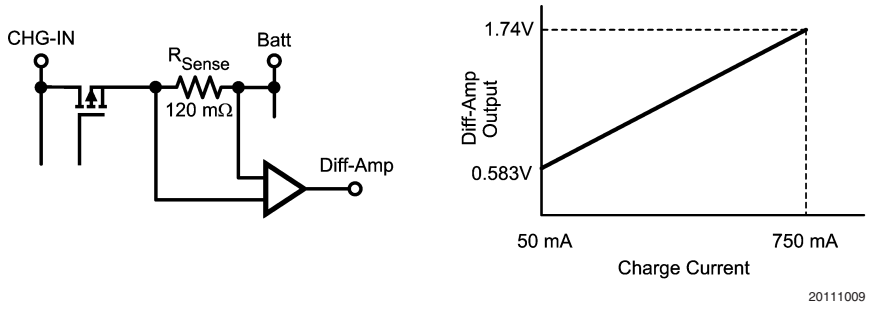


FIGURE 4. Charge Current Monitoring Circuit (Diff-Amp)

Monitoring the Diff Amp output during constant voltage cycle can provide an accurate indication of the battery charge status and time remaining to EOC. This feature is particularly useful during constant voltage mode. The current sense circuit is operational in the LDO mode as well. It can be used to monitor the system current consumption during testing.

LED CHARGE STATUS INDICATORS

The LP3947 is equipped with two open drain outputs to drive a green LED and a red LED. These two LEDs work together in combinations to indicate charge status or fault conditions. *Table 2* shows all the conditions.

Application Notes (Continued)

TABLE 2. LED Indicator Summary

	RED LED (CHG)	GREEN LED (EOC)
Charger Off	OFF	OFF
Charging Li Ion Battery*	ON	OFF
Maintenance Mode	OFF	ON
Charging Li Ion Battery after Passing Maintenance Mode	OFF	ON
EN Pin = LOW	OFF	ON
LDO Mode	OFF	OFF
5.6 Hr Safety Timer Flag/Battery Temperature Violation	ON	ON

* Charging Li Ion battery for the first time after V_{CHG-IN} insertion.

Ts PIN

The LP3947 continuously monitors the battery temperature by measuring the voltage between the Ts pin and ground. Charging stops if the battery temperature is outside the permitted temperature range set by the battery's internal thermistor R_T and the external bias resistor R_S. A 1% precision resistor should be used for R_S. A curve 2 type thermistor is recommended for R_T. The voltage across R_T is proportional to the battery temperature. If the battery temperature is outside of the range during the charge cycle, the LP3947 will suspend charging. As an example, for a temperature range of 0˚C to 50˚C, a 10kΩ for the thermistor and a 4.1kΩ for R_s should be used. When battery temperature returns to the permitted range, charging resumes from the beginning of the flow chart and the 5.6 hr safety timer is reset. Refer to *Figure 3*. LP3947 Charger Flow Chart for more information.

In absence of the thermistor, Ts pin will be pulled high to VT and the LP3947 goes into LDO mode. In this mode, the internal power FET provides up to 1.2 amp of current at the BATT pin. The LDO output is set to 4.1V or 4.2V, depending on the programmed battery regulation voltage. When operating at higher output currents, care must be taken not to exceed the package power dissipation rating. See "Thermal Performance of LLP Package" section for more detail.

Charger Status in Relation to Ts Voltage

Voltage on the Ts Pin	Charger Status
Ts ≥ 2.7V	LDO Mode
2.427v ≤ Ts < 2.7V 0V ≤ Ts ≤ 1.39V	Charger Off
1.39V < Ts < 2.427V	Charger On

LDO MODE

The charger is in the LDO mode when the Ts pin is left floating. This mode of operation is used primarily during system level testing of the handset to eliminate the need for battery insertion. **CAUTION:** battery may be damaged if device is operating in LDO mode with battery connected.

The internal power FET provides up to 1.2 amp of current at BATT pin in this mode. The LDO output is set to 4.1V. When operating at higher output currents, care must be taken not to exceed the package power dissipation rating. See "Thermal Performance of LLP Package" section for more detail.

EN PIN

The Enable pin is used to enable/disable the charger, in both the charger mode and the LDO mode, see *Figures 5, 6*. The enable pin is internally pulled HIGH to the CHG-IN pin. When the charger is disabled, it draws less than 4 µA of current.

Application Notes (Continued)

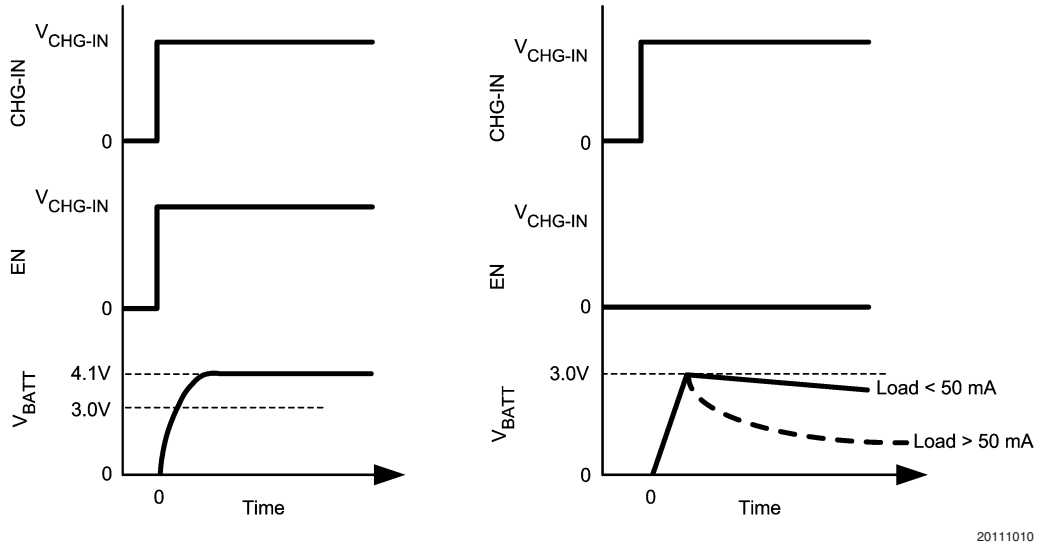


FIGURE 5. Power Up Timing Diagram in Charger Mode (1.39V < Ts < 2.427V)

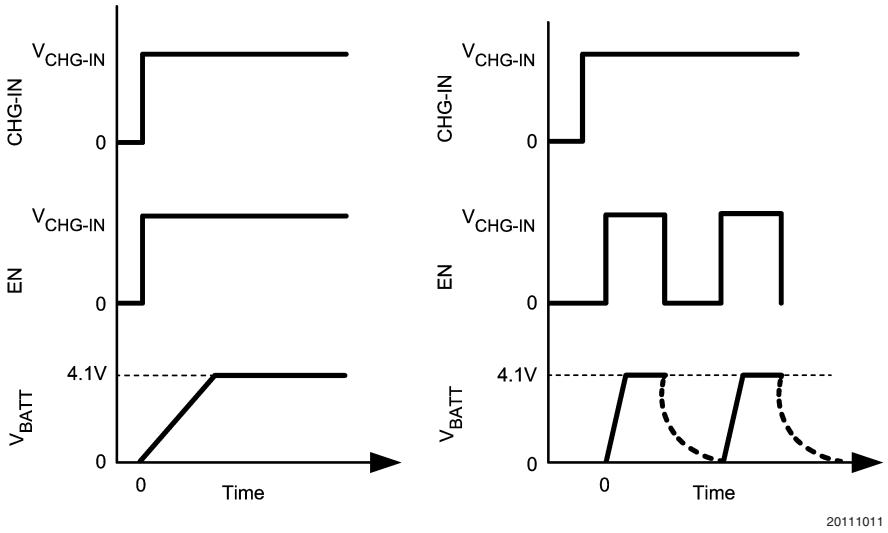


FIGURE 6. Power Up Timing Diagram in LDO Mode (Ts ≥ 2.7V)

MODE PIN

The mode pin toggles the LP3947 between the AC adaptor mode and the USB mode. When CHG-IN is connected to a USB port, this pin must be set low. When CHG-IN is connected to an AC adaptor, this pin must be tied high to either the BATT pin or to the wall adaptor input. Caution: MODE pin should never be tied to CHG-IN pin directly, as it will turn on an internal diode.

5.6 HR SAFETY TIMER IN CHARGER MODE

The LP3947 has a built-in 5.6 hr back up safety timer to prevent over-charging a Li Ion battery. The 5.6 hr timer starts counting when the charger enters the constant current mode. It will turn the charger off when the 5.6 hr timer is up while the charger is still in constant current mode. In this case, both LEDs will turn on, indicating a fault condition.

When the battery temperature is outside the specified temperature range, the 5.6 hr safety timer will reset upon recovery of the battery temperature.

I^2C INTERFACE

I^2C interface is used in the LP3947 to program various parameters as shown in *Table 3*. The LP3947 operates on default settings following power up. Once programmed, the LP3947 retains the register data as long as the battery voltage is above 2.85V.

Application Notes (Continued)

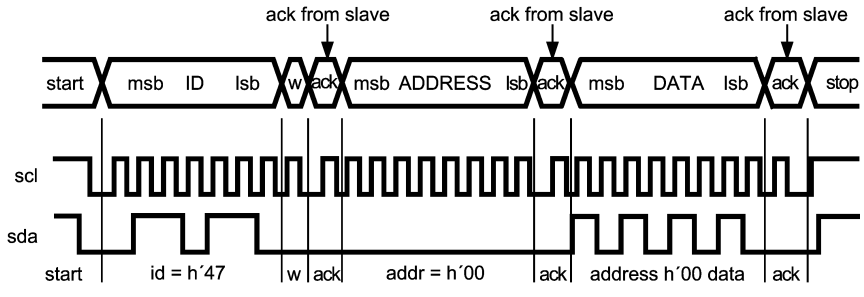
TABLE 3. LP3947 Serial Port Communication address code 7h'47

LP3947 Control and Data Codes									
Addrs	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
8'h00	Charger Register -1				Batt Voltage (0) = 4.1V 1 = 4.2V	AC Adaptor Charge Current Code 3 (1)	AC Adaptor Charge Current Code 2 (0)	AC Adaptor Charge Current Code 1 (0)	AC Adaptor Charge Current Code 0 (0)
8'h01	Charger Register -2				EOC (Green LED) R/O	Charging (Red LED) R/O	EOC SEL-1 (0)	EOC SEL-0 (1)	
8'h02	Charger Register -3					USB Charge Current Code 3 (1)	USB Charge Current Code 2 (0)	USB Charge Current Code 1 (0)	USB Charge Current Code 0 (0)

Numbers in parentheses indicate default setting. "0" bit is set to low state, and "1" bit is set to high state. R/O –Read Only, All other bits are Read and Write.

TABLE 4. Charger Current and EOC Current Programming Code

Data Code	Charger Current Selection Code I_{SET} (mA)	End of Charge Current Selection Code
4h'00	100	
4h'01	150	**0.1C**
4h'02	200	0.15C
4h'03	250	0.2C
4h'04	300	
4h'05	350	
4h'06	400	
4h'07	450	
4h'08	**500**	
4h'09	550	
4h'0A	600	
4h'0B	650	
4h'0C	700	
4h'0D	750	



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w = write (sda = "0")

r = read (sda = "1")

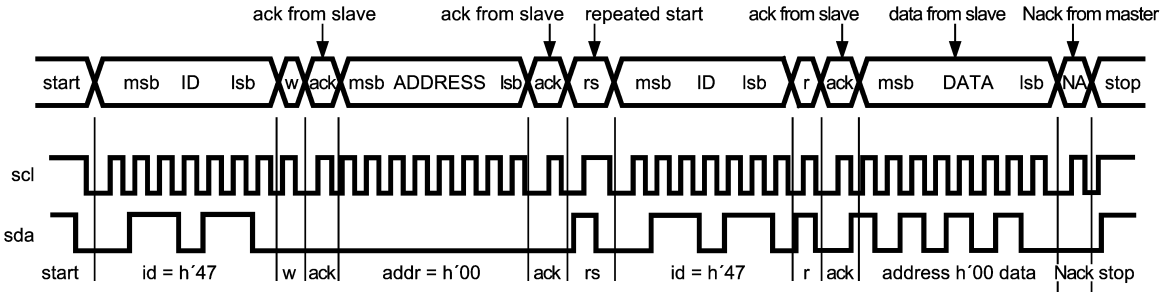
ack = acknowledge (sda pulled low by either master or slave)

Nack = No Acknowledge

rs = repeated start

FIGURE 7. LP3947 (Slave) Register Write

Application Notes (Continued)



w = write (sda = "0")

r = read (sda = "1")

ack = acknowledge (sda pulled low by either master or slave)

Nack = No Acknowledge

rs = repeated start

FIGURE 8. LP3947 (Slave) Register Read

THERMAL PERFORMANCE OF LLP PACKAGE

The LP3947 is a monolithic device with an integrated pass transistor. To enhance the power dissipation performance, the Leadless Lead frame Package, or LLP, is used. The LLP package is designed for improved thermal performance because of the exposed die attach pad at the bottom center of the package. It brings advantage to thermal performance by creating a very direct path for thermal dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the mold compound, the LLP reduces a layer of thermal path.

The thermal advantage of the LLP package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board and thermal vias are planted underneath the thermal land. Based on a LLP thermal measurement, junction to ambient thermal resistance (θ_{JA}) can be improved by as much as two times if a LLP is soldered on the board with thermal land and thermal vias than if not.

An example of how to calculate for LLP thermal performance is shown below:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

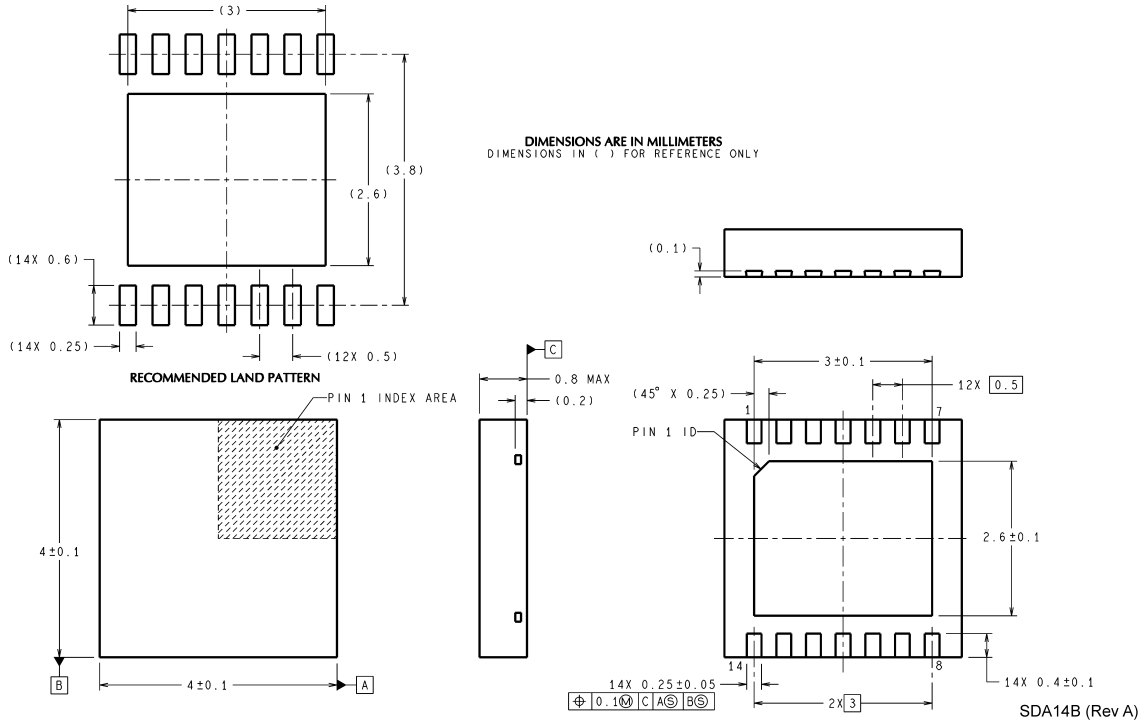
By substituting 37˚C/W for θ_{JA}, 125˚C for T_J and 70˚C for T_A, the maximum power dissipation allowed from the chip is 1.48W. If V_{CHG-IN} is at 5.0V and a 3.0V battery is being charged, then 740 mA of I_{CHG} can safely charge the battery. More power can be dissipated at ambient temperatures below 70˚C. Less power can be dissipated at ambient temperatures above 70˚C. The maximum power dissipation for operation can be increased by 27 mW for each degree below 70˚C, and it must be de-rated by 27 mW for each degree above 70˚C.

LAYOUT CONSIDERATION

The LP3947 has an exposed die attach pad located at the bottom center of the LLP package. It is imperative to create a thermal land on the PCB board when designing a PCB layout for the LLP package. The thermal land helps to conduct heat away from the die, and the land should be the same dimension as the exposed pad on the bottom of the LLP (1:1 ratio). In addition, thermal vias should be added inside the thermal land to conduct more heat away from the surface of the PCB to the ground plane. Typical pitch and outer diameter for these thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1oz although thicker copper may be used to improve thermal performance. The LP3947 bottom pad is connected to ground. Therefore, the thermal land and vias on the PCB board need to be connected to ground.

For more information on board layout techniques, refer to Application Note 1187 "Leadless Leadframe Package (LLP)." The application note also discusses package handling, solder stencil, and assembly.

Physical Dimensions inches (millimeters) unless otherwise noted



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