μPD44164184B

18M-BIT DDR II SRAM
4-WORD BURST OPERATION

Description

The μPD44164184B is a 1,048,576-word by 18-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD44164184B integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and K#) are latched on the positive edge of K and K#. These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.
These products are packaged in 165-pin PLASTIC BGA.

Features

- 1.8 ± 0.1 V power supply

- 165-pin PLASTIC BGA (13 x 15)

- HSTL interface

- PLL circuitry for wide output data valid window and future frequency scaling

- Pipelined double data rate operation

- Common data input/output bus

- Two-tick burst for low DDR transaction size

- Two input clocks (K and K#) for precise DDR timing at clock rising edges only

- Two output clocks (C and C#) for precise flight time

  and clock skew matching-clock and data delivered together to receiving device

- Internally self-timed write control

- Clock-stop capability. Normal operation is restored in 20 μs after clock is resumed.

- User programmable impedance output (35 to 70 Ω)

- Fast clock cycle time : 3.3 ns (300 MHz), 3.5 ns (287 MHz), 4.0 ns (250 MHz), 5.0 ns (200 MHz)

- Simple control logic for easy depth expansion

- JTAG 1149.1 compatible test access port

Ordering Information

Part No.	Organization (word x bit)	Cycle time	Clock frequency	Operating Ambient Temperature	Package
μPD44164184BF5-E33-EQ3-A	1M x 18	3.3ns	300MHz	Ta = 0 to 70°C	165-pin PLASTIC BGA (13 x 15) Lead-free
μPD44164184BF5-E35-EQ3-A		3.5ns	287MHz		
μPD44164184BF5-E40-EQ3-A		4.0ns	250MHz		
μPD44164184BF5-E50-EQ3-A		5.0ns	200MHz		
μPD44164184BF5-E33-EQ3	1M x 18	3.3ns	300MHz	Ta = 0 to 70°C	165-pin PLASTIC BGA (13 x 15) Lead
μPD44164184BF5-E35-EQ3		3.5ns	287MHz		
μPD44164184BF5-E40-EQ3		4.0ns	250MHz		
μPD44164184BF5-E50-EQ3		5.0ns	200MHz		
μPD44164184BF5-E33Y-EQ3-A	1M x 18	3.3ns	300MHz	Ta = −40 to 85°C	165-pin PLASTIC BGA (13 x 15) Lead-free
μPD44164184BF5-E35Y-EQ3-A		3.5ns	287MHz		
μPD44164184BF5-E40Y-EQ3-A		4.0ns	250MHz		
μPD44164184BF5-E50Y-EQ3-A		5.0ns	200MHz		
μPD44164184BF5-E33Y-EQ3	1M x 18	3.3ns	300MHz	Ta = −40 to 85°C	165-pin PLASTIC BGA (13 x 15) Lead
μPD44164184BF5-E35Y-EQ3		3.5ns	287MHz		
μPD44164184BF5-E40Y-EQ3		4.0ns	250MHz		
μPD44164184BF5-E50Y-EQ3		5.0ns	200MHz		

Pin Arrangement

165-pin PLASTIC BGA (13 x 15)

(Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	Vss/72M	A	R, W#	BW1#	K#	NC/144M	LD#	A	Vss/36M	CQ
B	NC	DQ9	NC	A	NC/288M	K	BW0#	A	NC	NC	DQ8
C	NC	NC	NC	Vss	A	A0	A1	Vss	NC	DQ7	NC
D	NC	NC	DQ10	Vss	Vss	Vss	Vss	Vss	NC	NC	NC
E	NC	NC	DQ11	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ6
F	NC	DQ12	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ5
G	NC	NC	DQ13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC
H	DLL#	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	DQ4	NC
K	NC	NC	DQ14	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ3
L	NC	DQ15	NC	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	DQ1	NC
N	NC	NC	DQ16	Vss	A	A	A	Vss	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A0, A1, A	: Address inputs		TMS	: IEEE 1149.1 Test input
DQ0 to DQ17	: Data inputs / outputs		TDI	: IEEE 1149.1 Test input
LD#	: Synchronous load		TCK	: IEEE 1149.1 Clock input
R, W#	: Read Write input		TDO	: IEEE 1149.1 Test output
BW0#, BW1#	: Byte Write data select		V_{REF}	: HSTL input reference input
K, K#	: Input clock		V_{DD}	: Power Supply
C, C#	: Output clock		$V_{DD}Q$	: Power Supply
CQ, CQ#	: Echo clock		V_{SS}	: Ground
ZQ	: Output impedance matching		NC	: No connection
DLL#	: PLL disable		NC/xxM	: Expansion address for xxMb

Remarks 1. ×××# indicates active LOW.
    2. Refer to **Package Dimensions** for the index mark.
    3. 2A, 7A, 10A and 5B are expansion addresses   : 10A for 36Mb
                                                              : 10A and 2A for 72Mb
                                                              : 10A, 2A and 7A for 144Mb
                                                              : 10A, 2A, 7A and 5B for 288Mb

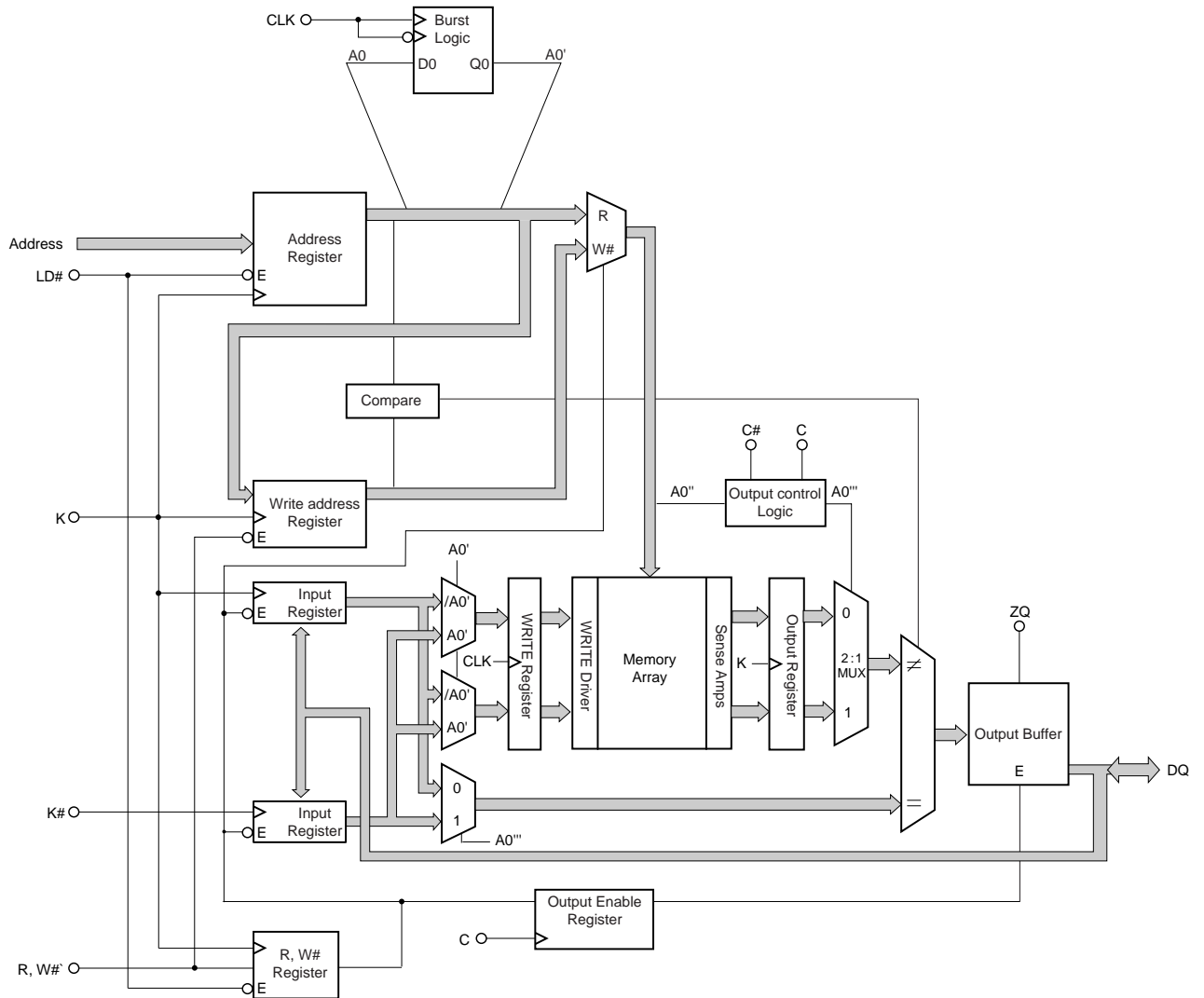   2A and 10A of this product can also be used as NC.

Pin Description

(1/2)

Symbol	Type	Description
A0 A1 A	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of four words (two clock periods of bus activity). A0 and A1 are used as the lowest two address bits for BURST READ and BURST WRITE operations permitting a random burst start address. These inputs are ignored when device is deselected, i.e., NOP (LD# = HIGH), or once BURST operation is in progress.
DQ0 to DQ17	Input/Output	Synchronous Data IOs: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective C and C# data clocks or to K and K# if C and C# are tied to HIGH.
LD#	Input	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of 4 data (two clock periods of bus activity).
R, W#	Input	Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R, W# is HIGH, WRITE when R, W# is LOW) for the loaded address. R, W# must meet the setup and hold times around the rising edge of K. If a synchronous load command (LD# = LOW) is input, inputs of R, W# and LD# on the subsequent rising edge of K are ignored.
BW0#, BW1#.	Input	Synchronous Byte Writes: When LOW these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See **Pin Arrangement** for signal to data relationships. See **Byte Write Operation** for relation between BWx# and Dxx.
K, K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C, C#	Input	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of C# is used as the output timing reference for first output data. The rising edge of C is used as the output reference for second output data. Ideally, C# is 180 degrees out of phase with C. When use of K and K# as the reference instead of C and C#, then fixed C and C# to HIGH. Operation cannot be guaranteed unless C and C# are fixed to HIGH (i.e. toggle of C and C#)

(2/2)

Symbol	Type	Description
CQ, CQ#	Output	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when DQ tristates. If C and C# are stopped (if K and K# are stopped in the single clock mode), CQ and CQ# will also stop.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ, CQ and CQ# output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to ground. The output impedance can be minimized by directly connect ZQ to $V_{DD}Q$. This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 20 μs upon power-up to account for drifts in supply voltage and temperature. After replacement for a resistor, the new output impedance is reset by implementing power-on sequence.
DLL#	Input	PLL Disable: When debugging the system or board, the operation can be performed at a clock frequency slower than TKHKH (MAX.) without the PLL circuit being used, if DLL# = LOW. The AC/DC characteristics cannot be guaranteed. For normal operation, DLL# must be HIGH and it can be connected to $V_{DD}Q$ through a 10 kΩ or less resistor.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 1.8 V I/O level. These balls may be left Not Connected if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 Clock Input: 1.8 V I/O level. This pin must be tied to V_{SS} if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: 1.8 V I/O level. When providing any external voltage to TDO signal, it is recommended to pull up to V_{DD}.
V_{REF}		HSTL Input Reference Voltage: Nominally $V_{DD}Q/2$. Provides a reference voltage for the input buffers.
V_{DD}	Supply	Power Supply: 1.8 V nominal. See **Recommended DC Operating Conditions** and **DC Characteristics** for range.
$V_{DD}Q$	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5 V. 1.8 V is also permissible. See **Recommended DC Operating Conditions** and **DC Characteristics** for range.
V_{SS}	Supply	Power Supply: Ground
NC		No Connect: These signals are not connected internally.

Block Diagram

Power-On Sequence in DDR II SRAM

DDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. The following timing charts show the recommended power-on sequence.

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, $V_{DD}Q$, V_{REF}, then V_{IN}. V_{DD} and $V_{DD}Q$ can be applied simultaneously, as long as $V_{DD}Q$ does not exceed V_{DD} by more than 0.5 V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, $V_{DD}Q$, V_{DD}, V_{SS}. V_{DD} and $V_{DD}Q$ can be removed simultaneously, as long as $V_{DD}Q$ does not exceed V_{DD} by more than 0.5 V during power-down.

**Power-On Sequence**

Apply power and tie DLL# to HIGH.
 - Apply V_{DD} before $V_{DD}Q$.
 - Apply $V_{DD}Q$ before V_{REF} or at the same time as V_{REF}.
Provide stable clock for more than 20 μs to lock the PLL.

PLL Constraints

The PLL uses K clock as its synchronizing input and the input should have low phase jitter which is specified as TKC var. The PLL can cover 120 MHz as the lowest frequency. If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an undesired clock frequency.

Power-On Waveforms
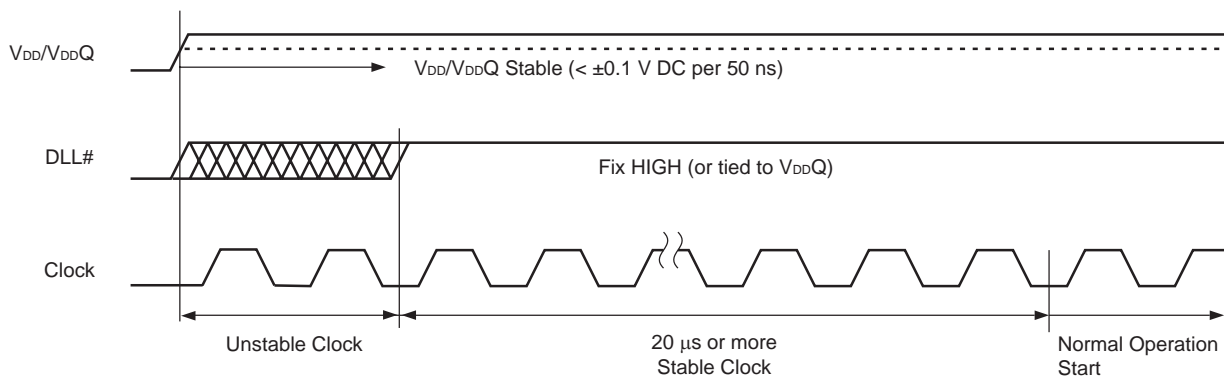
Burst Sequence

Linear Burst Sequence Table

	A1, A0	A1, A0	A1, A0	A1, A0
External Address	0, 0	0, 1	1, 0	1, 1
1st Internal Burst Address	0, 1	1, 0	1, 1	0, 0
2nd Internal Burst Address	1, 0	1, 1	0, 0	0, 1
3rd Internal Burst Address	1, 1	0, 0	0, 1	1, 0

Truth Table

Operation	LD#	R, W#	CLK	DQ				
WRITE cycle Load address, input write data on consecutive K and K# rising edge	L	L	L → H	Data in				
				Input data	D(A1)	D(A2)	D(A3)	D(A4)
				Input clock	K(t+1) ↑	K#(t+1) ↑	K(t+2) ↑↑	K#(t+2) ↑
READ cycle Load address, read data on consecutive C and C# rising edge	L	H	L → H	Data out				
				Output data	Q(A1)	Q(A2)	Q(A3)	Q(A4)
				Output clock	C#(t+1) ↑	C(t+2) ↑	C#(t+2) ↑	C(t+3) ↑
NOP (No operation)	H	×	L → H	High-Z				
Clock stop	×	×	Stopped	Previous state				

Remarks 1. H : HIGH, L : LOW, × : don't care, ↑ : rising edge.

    2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges except if C and C# are HIGH then Data outputs are delivered at K and K# rising edges.

    3. All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.

    4. This device contains circuitry that ensure the outputs to be in high impedance during power-up.

    5. Refer to state diagram and timing diagrams for clarification.

    6. A1 refers to the address input during a WRITE or READ cycle. A2, A3 and A4 refers to the next internal burst address in accordance with the linear burst sequence.

    7. It is recommended that K = K# = C = C# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
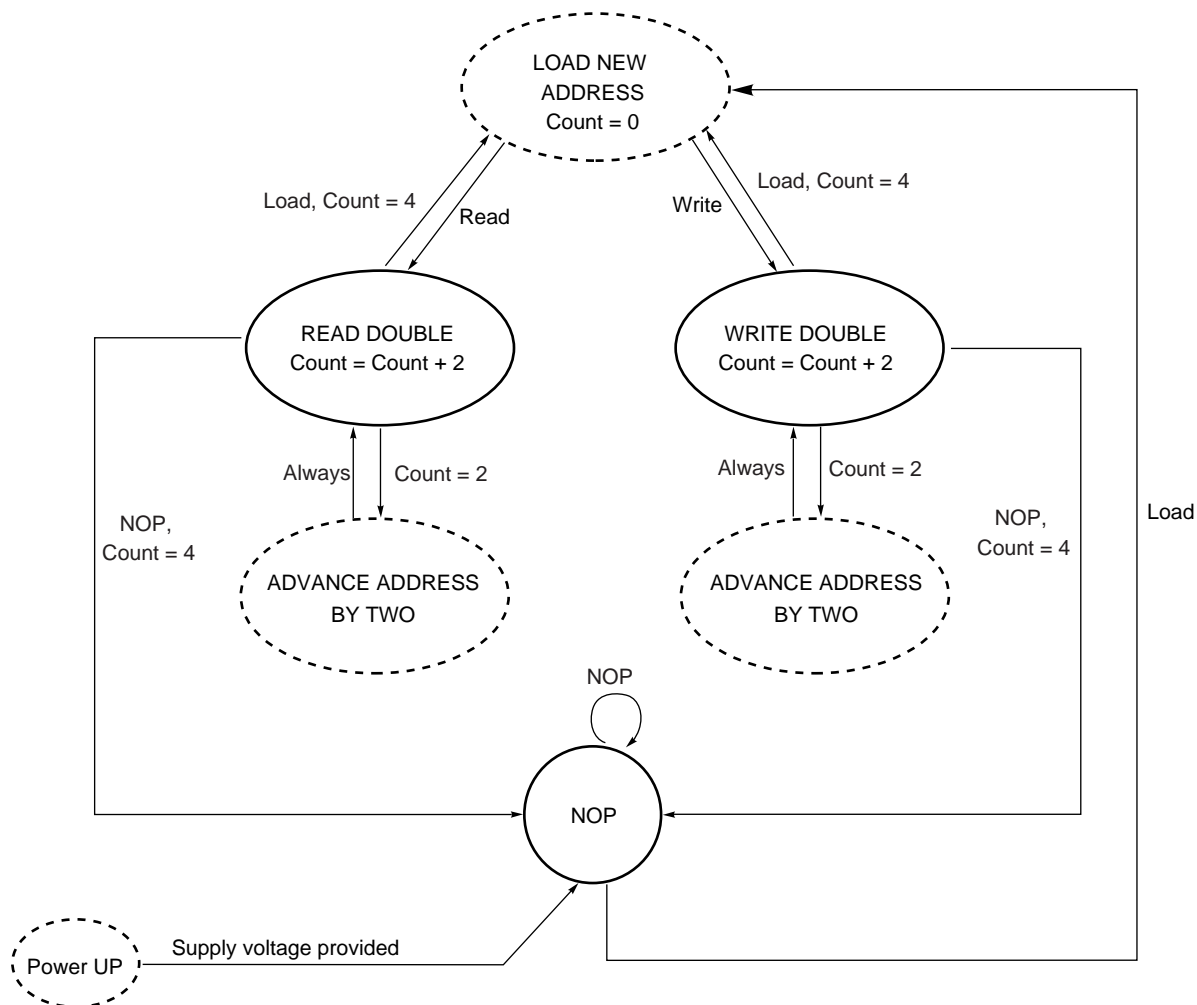
Byte Write Operation

Operation	K	K#	BW0#	BW1#
Write DQ0 to DQ17	L → H	–	0	0
	–	L → H	0	0
Write DQ0 to DQ8	L → H	–	0	1
	–	L → H	0	1
Write DQ9 to DQ17	L → H	–	1	0
	–	L → H	1	0
Write nothing	L → H	–	1	1
	–	L → H	1	1

Remarks 1. H : HIGH, L : LOW, → : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram

LOAD NEW
ADDRESS
Count = 0

Load, Count = 4   Read   Write   Load, Count = 4

READ DOUBLE
Count = Count + 2

WRITE DOUBLE
Count = Count + 2

Always   Count = 2   Always   Count = 2

NOP,
Count = 4   Load

NOP,
Count = 4

ADVANCE ADDRESS
BY TWO

ADVANCE ADDRESS
BY TWO

NOP

NOP

Power UP   Supply voltage provided

Remarks 1. A0 and A1 are internally advanced in accordance with the burst order table.

Bus cycle is terminated after burst count = 4.

2. State transitions: L = (LD# = LOW); L# = (LD# = HIGH); R = (R#, W = HIGH); W = (R#, W = LOW).

3. State machine control timing sequence is controlled by K.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		-0.5 to $+2.5$	V
Output supply voltage	$V_{DD}Q$		-0.5 to V_{DD}	V
Input voltage	V_{IN}		-0.5 to $V_{DD}+0.5$ (2.5 V MAX.)	V
Input / Output voltage	$V_{I/O}$		-0.5 to $V_{DD}Q+0.5$ (2.5 V MAX.)	V
Operating ambient temperature	T_A	(E** series)	0 to 70	°C
		(E**Y series)	-40 to 85	
Storage temperature	T_{stg}		-55 to $+125$	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C, T_A = $-$40 to 85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		1.7	1.8	1.9	V	
Output supply voltage	$V_{DD}Q$		1.4		V_{DD}	V	1
Input HIGH voltage	$V_{IH (DC)}$		V_{REF} +0.1		$V_{DD}Q+0.3$	V	1, 2
Input LOW voltage	$V_{IL (DC)}$		-0.3		V_{REF} -0.1	V	1, 2
Clock input voltage	V_{IN}		-0.3		$V_{DD}Q+0.3$	V	1, 2
Reference voltage	V_{REF}		0.68		0.95	V	

Notes 1. During normal operation, $V_{DD}Q$ must not exceed V_{DD}.
  2. Power-up: VIH $\leq$ $V_{DD}Q$ +0.3 V and V_{DD} $\leq$ 1.7 V and $V_{DD}Q \leq$ 1.4 V for t $\leq$ 200 ms

Recommended AC Operating Conditions (T_A = 0 to 70°C, T_A = $-$40 to 85°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	$V_{IH (AC)}$		V_{REF} +0.2		V	1
Input LOW voltage	$V_{IL (AC)}$			V_{REF} -0.2	V	1

Note 1. Overshoot: $V_{IH (AC)} \leq V_{DD}$ +0.7 V (2.5 V MAX.) for t $\leq$ TKHKH/2
  Undershoot: $V_{IL (AC)} \geq -0.5$ V for t $\leq$ TKHKH/2
  Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).

DC Characteristics 1 (T$_A$ = 0 to 70°C, V$_{DD}$ = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Note
Input leakage current	I$_{LI}$			−2	+2	μA	
I/O leakage current	I$_{LO}$			−2	+2	μA	
Operating supply current (Read cycle / Write cycle)	I$_{DD}$	V$_{IN}$ ≤ V$_{IL}$ or V$_{IN}$ ≥ V$_{IH}$, I$_{I/O}$ = 0 mA, Cycle = MAX.	-E33		440	mA	
			-E35		430		
			-E40		400		
			-E50		360		
Standby supply current (NOP)	I$_{SB1}$	V$_{IN}$ ≤ V$_{IL}$ or V$_{IN}$ ≥ V$_{IH}$, I$_{I/O}$ = 0 mA, Cycle = MAX. Inputs static	-E33		400	mA	
			-E35		390		
			-E40		380		
			-E50		350		
Output HIGH voltage	V$_{OH(Low)}$	|I$_{OH}$| ≤ 0.1 mA		V$_{DD}$Q−0.2	V$_{DD}$Q	V	3, 4
	V$_{OH}$	Note1		V$_{DD}$Q/2−0.12	V$_{DD}$Q/2+0.12	V	3, 4
Output LOW voltage	V$_{OL(Low)}$	I$_{OL}$ ≤ 0.1 mA		V$_{SS}$	0.2	V	3, 4
	V$_{OL}$	Note2		V$_{DD}$Q/2−0.12	V$_{DD}$Q/2+0.12	V	3, 4

Notes **1.** Outputs are impedance-controlled. $| I_{OH} |$ = (V$_{DD}$Q/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.
      2. Outputs are impedance-controlled. I$_{OL}$ = (V$_{DD}$Q/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.
      3. AC load current is higher than the shown DC values.
      4. HSTL outputs meet JEDEC HSTL Class I standards.

DC Characteristics 2 (T$_A$ = −40 to 85°C, V$_{DD}$ = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Note
Input leakage current	I$_{LI}$			−2	+2	μA	
I/O leakage current	I$_{LO}$			−2	+2	μA	
Operating supply current (Read cycle / Write cycle)	I$_{DD}$	V$_{IN}$ ≤ V$_{IL}$ or V$_{IN}$ ≥ V$_{IH}$, I$_{I/O}$ = 0 mA, Cycle = MAX.	-E33Y		560	mA	
			-E35Y		550		
			-E40Y		520		
			-E50Y		480		
Standby supply current (NOP)	I$_{SB1}$	V$_{IN}$ ≤ V$_{IL}$ or V$_{IN}$ ≥ V$_{IH}$, I$_{I/O}$ = 0 mA, Cycle = MAX. Inputs static	-E33Y		520	mA	
			-E35Y		510		
			-E40Y		500		
			-E50Y		470		
Output HIGH voltage	V$_{OH(Low)}$	|I$_{OH}$| ≤ 0.1 mA		V$_{DD}$Q−0.2	V$_{DD}$Q	V	3, 4
	V$_{OH}$	Note1		V$_{DD}$Q/2−0.12	V$_{DD}$Q/2+0.12	V	3, 4
Output LOW voltage	V$_{OL(Low)}$	I$_{OL}$ ≤ 0.1 mA		V$_{SS}$	0.2	V	3, 4
	V$_{OL}$	Note2		V$_{DD}$Q/2−0.12	V$_{DD}$Q/2+0.12	V	3, 4

Notes **1.** Outputs are impedance-controlled. $| I_{OH} |$ = (V$_{DD}$Q/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.
      2. Outputs are impedance-controlled. I$_{OL}$ = (V$_{DD}$Q/2)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.
      3. AC load current is higher than the shown DC values.
      4. HSTL outputs meet JEDEC HSTL Class I standards.

Capacitance (T$_A$ = 25°C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Input capacitance (Address, Control)	C$_{IN}$	V$_{IN}$ = 0 V		5	pF
Input / Output capacitance (DQ, CQ, CQ#)	C$_{I/O}$	V$_{I/O}$ = 0 V		7	pF
Clock Input capacitance	C$_{clk}$	V$_{clk}$ = 0 V		6	pF

Remark These parameters are periodically sampled and not 100% tested.

Thermal Characteristics

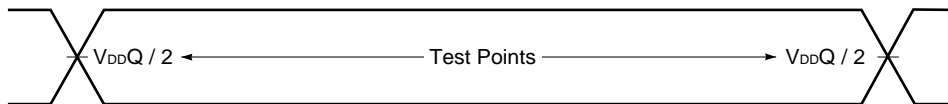| Parameter	Symbol	Substrate	Airflow	TYP.	Unit
Thermal resistance from junction to ambient air	θ_{ja}	4-layer	0 m/s	21.4	°C/W
			1 m/s	13.6	°C/W
		8-layer	0 m/s	20.3	°C/W
			1 m/s	13.1	°C/W
Thermal characterization parameter from junction to the top center of the package surface	Ψ_{jt}	4-layer	0 m/s	0.02	°C/W
			1 m/s	0.06	°C/W
		8-layer	0 m/s	0.02	°C/W
			1 m/s	0.06	°C/W
Thermal resistance from junction to case	θ_{jc}			2.65	°C/W

AC Characteristics (T$_A$ = 0 to 70°C or T$_A$ = −40 to 85°C, V$_{DD}$ = 1.8 ± 0.1 V)

AC Test Conditions (V$_{DD}$ = 1.8 ± 0.1 V, V$_{DD}$Q = 1.4 V to V$_{DD}$)

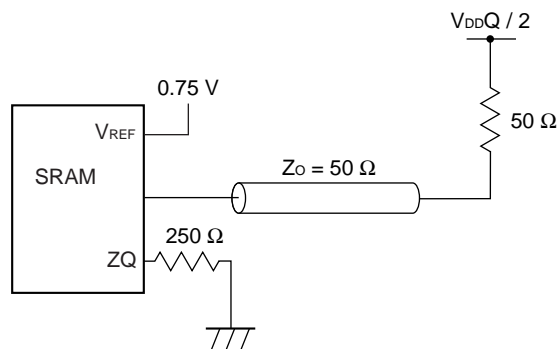**Input waveform (Rise / Fall time ≤ 0.3 ns)**

1.25 V

0.75 V ← Test Points → 0.75 V

0.25 V

Output waveform

V$_{DD}$Q / 2 ← Test Points → V$_{DD}$Q / 2
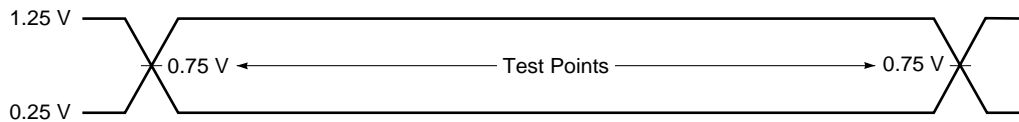
Output load condition

Figure 1. External load at test

V$_{DD}$Q / 2

50 Ω

0.75 V

V$_{REF}$

SRAM

Z$_O$ = 50 Ω

250 Ω

ZQ

Read and Write Cycle

| Parameter	Symbol	-E33, E33Y (300 MHz)		-E35, E35Y (287 MHz)		-E40, E40Y (250 MHz)		-E50, E50Y (200 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock											
Average Clock cycle time (K, K#, C, C#)	TKHKH	3.3	8.4	3.5	8.4	4.0	8.4	5.0	8.4	ns	1
Clock phase jitter (K, K#, C, C#)	TKC var		0.2		0.2		0.2		0.2	ns	2
Clock HIGH time (K, K#, C, C#)	TKHKL	1.32		1.5		1.6		2.0		ns	
Clock LOW time (K, K#, C, C#)	TKLKH	1.32		1.5		1.6		2.0		ns	
Clock HIGH to Clock# HIGH (K → K#, C → C#)	TKHK#H	1.49		1.7		1.8		2.2		ns	
Clock# HIGH to Clock HIGH (K# → K, C# → C)	TK#HKH	1.49		1.7		1.8		2.2		ns	
Clock to data clock (K → C, K# → C#)	TKHCH	0	1.45	0	1.65	0	1.8	0	2.3	ns	
PLL lock time (K, C)	TKC lock	20		20		20		20		μs	3
K static to PLL reset	TKC reset	30		30		30		30		ns	4
Output Times											
CQ HIGH to CQ# HIGH (CQ → CQ#)	TCQHCQ#H	1.24		1.35		1.55		1.95		ns	5
CQ# HIGH to CQ HIGH (CQ# → CQ)	TCQ#HCQH	1.24		1.35		1.55		1.95		ns	5
C, C# HIGH to output valid	TCHQV		0.45		0.45		0.45		0.45	ns	
C, C# HIGH to output hold	TCHQX	−0.45		−0.45		−0.45		−0.45		ns	
C, C# HIGH to echo clock valid	TCHCQV		0.45		0.45		0.45		0.45	ns	
C, C# HIGH to echo clock hold	TCHCQX	−0.45		−0.45		−0.45		−0.45		ns	
CQ, CQ# HIGH to output valid	TCQHQV		0.27		0.3		0.3		0.35	ns	6
CQ, CQ# HIGH to output hold	TCQHQX	−0.27		−0.3		−0.3		−0.35		ns	6
C HIGH to output High-Z	TCHQZ		0.45		0.45		0.45		0.45	ns	
C HIGH to output Low-Z	TCHQX1	−0.45		−0.45		−0.45		−0.45		ns	
Setup Times											
Address valid to K rising edge	TAVKH	0.4		0.5		0.5		0.6		ns	7
Synchronous load input (LD#), read write input (R, W#) valid to K rising edge	TIVKH	0.4		0.5		0.5		0.6		ns	7
Data inputs and write data select inputs (BWx#) valid to K, K# rising edge	TDVKH	0.3		0.35		0.35		0.4		ns	7
Hold Times											
K rising edge to address hold	TKHAX	0.4		0.5		0.5		0.6		ns	7
K rising edge to synchronous load input (LD#), read write input (R, W#) hold	TKHIX	0.4		0.5		0.5		0.6		ns	7
K, K# rising edge to data inputs and write data select inputs (BWx#) hold	TKHDX	0.3		0.35		0.35		0.4		ns	7

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Notes 1. When debugging the system or board, these products can operate at a clock frequency slower than TKHKH (MAX.) without the PLL circuit being used, if DLL# = LOW. Read latency (RL) is changed to 1.0 clock cycle in this operation. The AC/DC characteristics cannot be guaranteed, however.

2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge. TKC var (MAX.) indicates a peak-to-peak value.

3. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for PLL lock retention.
PLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept NOP (LD# = HIGH) during these cycles.

4. K input is monitored for this operation. See below for the timing.
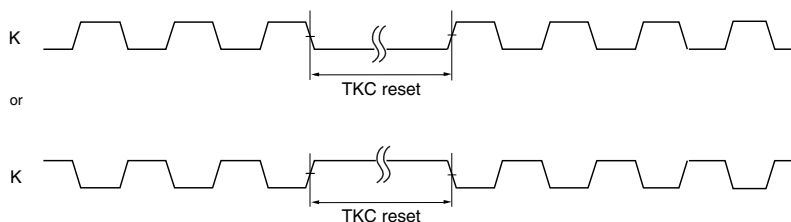
5. Guaranteed by design.

6. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.

7. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

Remarks 1. This parameter is sampled.

2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).

4. If C, C# are tied HIGH, K, K# become the references for C, C# timing parameters.

5. $V_{DD}Q$ is 1.5 V DC.

Read and Write Timing
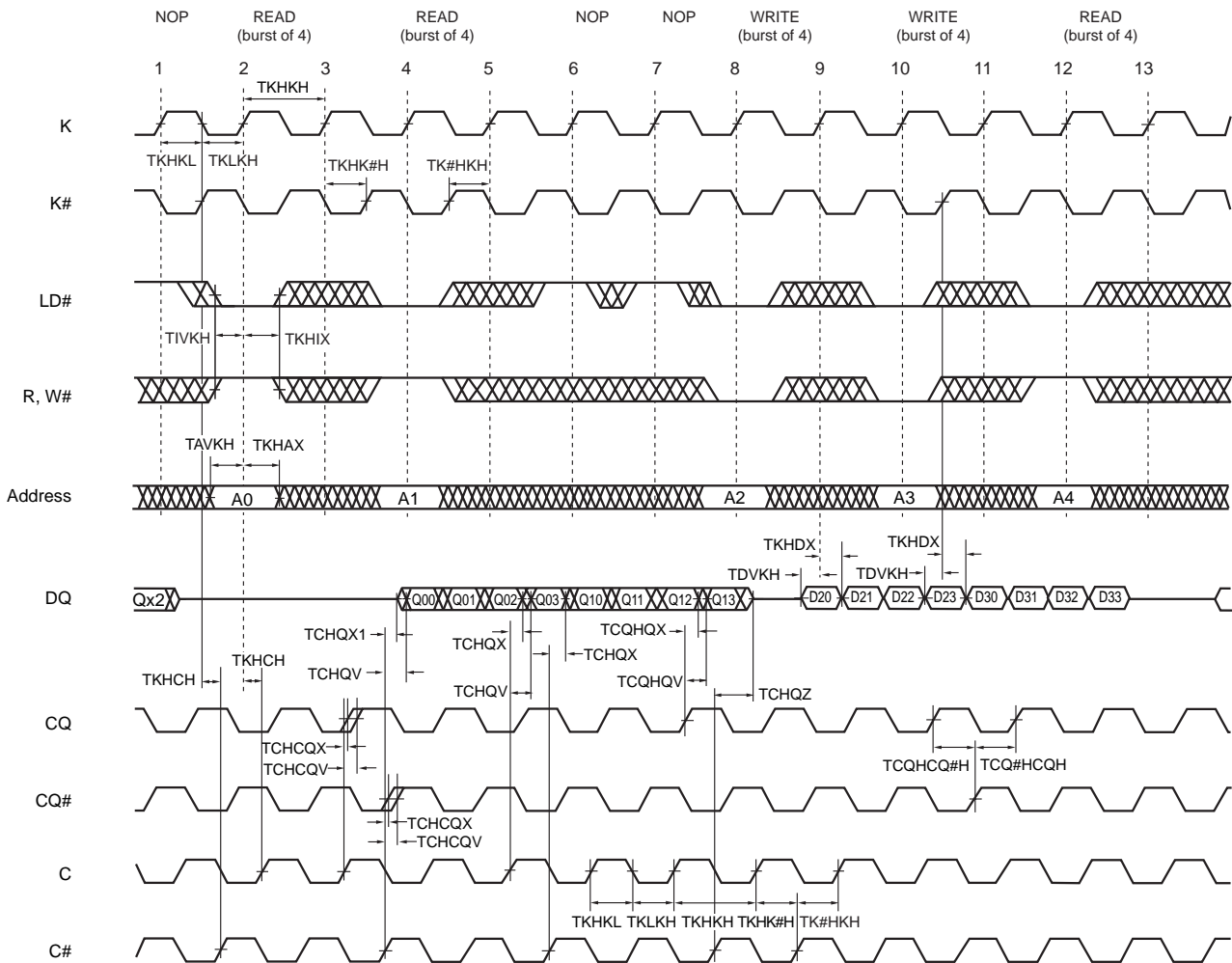
Remarks 1. Q01 refers to output from address A0.

Q02 refers to output from the next internal burst address following A0, etc.

2. Outputs are disabled (high impedance) 3.5 clock cycles after the last READ (LD# = LOW, R, W# = HIGH) is input in the sequences of [READ]-[NOP].

3. The second NOP cycle at the cycle "7" is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

Application Example

R = 50 Ω   V$_t$ = V$_{ref}$
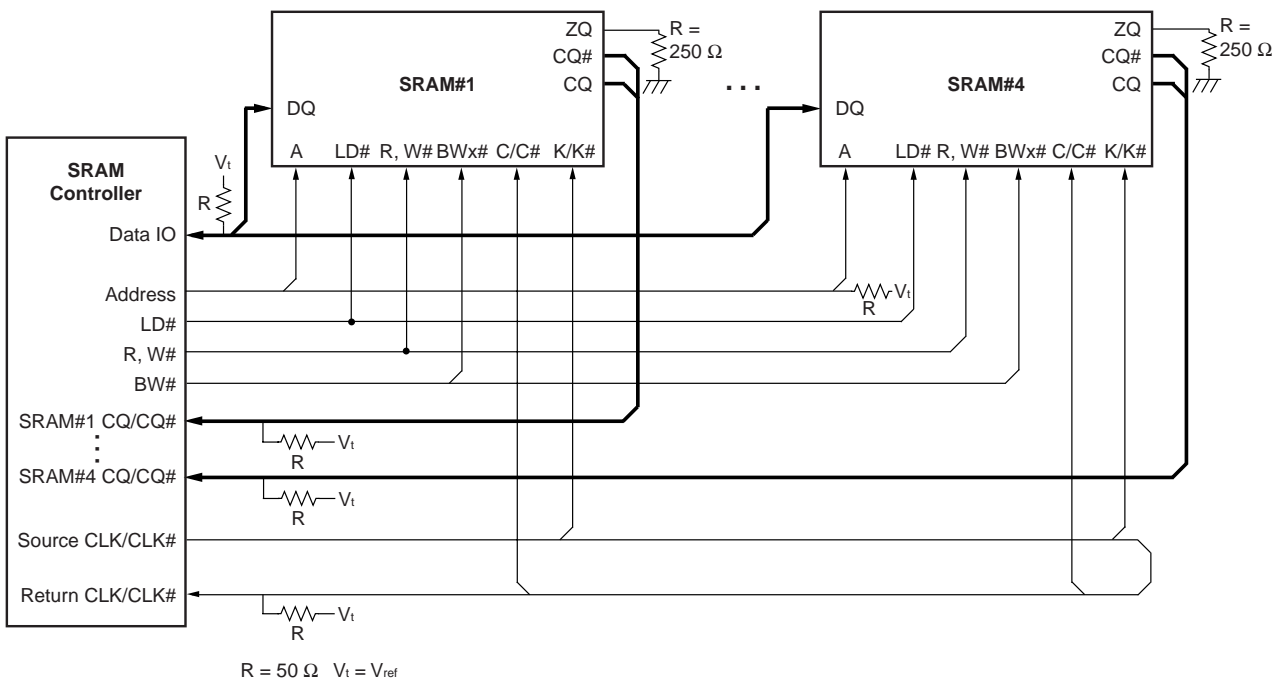
Remark AC characteristics are defined at the condition of SRAM outputs, CQ, CQ# and DQ with termination.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

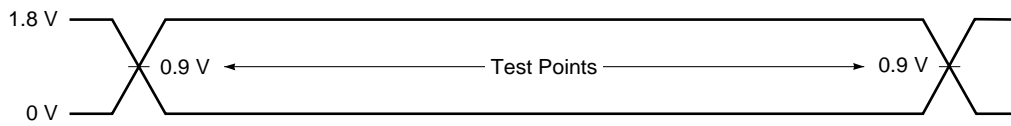| Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

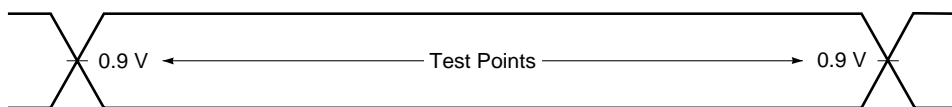**JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V, unless otherwise noted)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	−5.0	+5.0	μA
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DD}Q, Outputs disabled	−5.0	+5.0	μA
JTAG input HIGH voltage	V_{IH}		1.3	V_{DD}+0.3	V
JTAG input LOW voltage	V_{IL}		−0.3	+0.5	V
JTAG output HIGH voltage	V_{OH1}	| I_{OHC} | = 100 μA	1.6		V
	V_{OH2}	| I_{OHT} | = 2 mA	1.4		V
JTAG output LOW voltage	V_{OL1}	I_{OLC} = 100 μA		0.2	V
	V_{OL2}	I_{OLT} = 2 mA		0.4	V

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JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

```
1.8 V ─┐      ┌──────────────────────────────────┐      ┌──
        X   0.9 V  ◄──────────── Test Points ──────────►  0.9 V   X
0 V  ──┘      └──────────────────────────────────┘      └──
```

Output waveform

```
──┐      ┌──────────────────────────────────┐      ┌──
    X  0.9 V  ◄──────────── Test Points ──────────►  0.9 V   X
──┘      └──────────────────────────────────┘      └──
```

Output load

Figure 2. External load at test

$V_{TT} = 0.9$ V

50 Ω

$Z_O = 50$ Ω

TDO

20 pF

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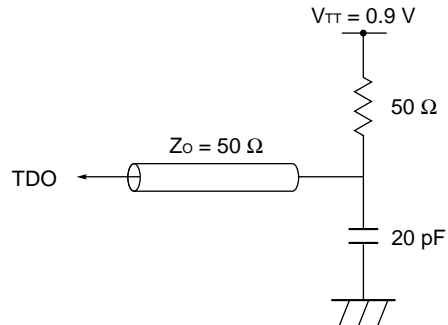
JTAG AC Characteristics (T$_A$ = 0 to 70°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock					
Clock cycle time	t$_{THTH}$		50		ns
Clock frequency	f$_{TF}$			20	MHz
Clock HIGH time	t$_{THTL}$		20		ns
Clock LOW time	t$_{TLTH}$		20		ns
Output time					
TCK LOW to TDO unknown	t$_{TLOX}$		0		ns
TCK LOW to TDO valid	t$_{TLOV}$			10	ns
Setup time					
TMS setup time	t$_{MVTH}$		5		ns
TDI valid to TCK HIGH	t$_{DVTH}$		5		ns
Capture setup time	t$_{CS}$		5		ns
Hold time					
TMS hold time	t$_{THMX}$		5		ns
TCK HIGH to TDI invalid	t$_{THDX}$		5		ns
Capture hold time	t$_{CH}$		5		ns

JTAG Timing Diagram
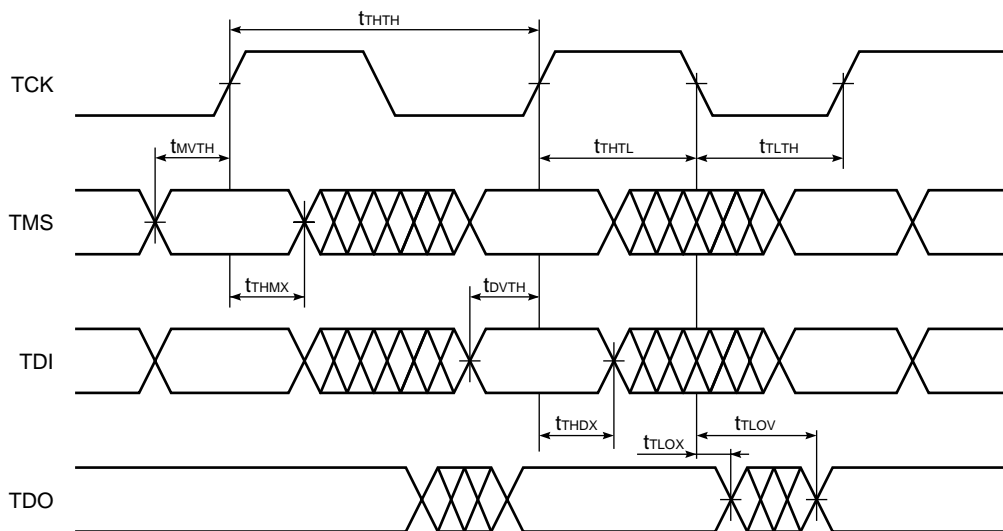
Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	107	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44164184B	1M x 18	XXXX	0000 0000 0001 0110	00000010000	1

SCAN Exit Order

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	C#	6R	37	NC	10D	73	NC	2C
2	C	6P	38	NC	9E	74	DQ11	3E
3	A	6N	39	DQ7	10C	75	NC	2D
4	A	7P	40	NC	11D	76	NC	2E
5	A	7N	41	NC	9C	77	NC	1E
6	A	7R	42	NC	9D	78	DQ12	2F
7	A	8R	43	DQ8	11B	79	NC	3F
8	A	8P	44	NC	11C	80	NC	1G
9	A	9R	45	NC	9B	81	NC	1F
10	DQ0	11P	46	NC	10B	82	DQ13	3G
11	NC	10P	47	CQ	11A	83	NC	2G
12	NC	10N	48	–	Internal	84	NC	1J
13	NC	9P	49	A	9A	85	NC	2J
14	DQ1	10M	50	A	8B	86	DQ14	3K
15	NC	11N	51	A1	7C	87	NC	3J
16	NC	9M	52	A0	6C	88	NC	2K
17	NC	9N	53	LD#	8A	89	NC	1K
18	DQ2	11L	54	NC	7A	90	DQ15	2L
19	NC	11M	55	BW0#	7B	91	NC	3L
20	NC	9L	56	K	6B	92	NC	1M
21	NC	10L	57	K#	6A	93	NC	1L
22	DQ3	11K	58	NC	5B	94	DQ16	3N
23	NC	10K	59	BW1#	5A	95	NC	3M
24	NC	9J	60	R, W#	4A	96	NC	1N
25	NC	9K	61	A	5C	97	NC	2M
26	DQ4	10J	62	A	4B	98	DQ17	3P
27	NC	11J	63	A	3A	99	NC	2N
28	ZQ	11H	64	DLL#	1H	100	NC	2P
29	NC	10G	65	CQ#	1A	101	NC	1P
30	NC	9G	66	DQ9	2B	102	A	3R
31	DQ5	11F	67	NC	3B	103	A	4R
32	NC	11G	68	NC	1C	104	A	4P
33	NC	9F	69	NC	1B	105	A	5P
34	NC	10F	70	DQ10	3D	106	A	5N
35	DQ6	11E	71	NC	3C	107	A	5R
36	NC	10E	72	NC	1D			

JTAG Instructions

Instructions	Description
EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE / PRELOAD	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and DQ pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (tCS plus tCH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM DQ pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	2
1	0	0	SAMPLE / PRELOAD	
1	0	1	RESERVED	2
1	1	0	RESERVED	2
1	1	1	BYPASS	

Notes 1. TRISTATE all DQ pins and CAPTURE the pad values into a SERIAL SCAN LATCH.

2. Do not use this instruction code because the vendor uses it to evaluate this product.

Output Pin States of CQ, CQ# and DQ

Instructions	Control-Register Status	Output Pin Status	
		CQ,CQ#	DQ
EXTEST	0	Update	High-Z
	1	Update	Update
IDCODE	0	SRAM	SRAM
	1	SRAM	SRAM
SAMPLE-Z	0	High-Z	High-Z
	1	High-Z	High-Z
SAMPLE	0	SRAM	SRAM
	1	SRAM	SRAM
BYPASS	0	SRAM	SRAM
	1	SRAM	SRAM

Remark The output pin statuses during each instruction vary according to the Control-Register status (value of Boundary Scan Register, bit no. 107).
There are three statuses:

  Update : Contents of the "Update Register" are output to the output pin (DDR Pad).

  SRAM : Contents of the SRAM internal output "SRAM Output" are output to the output pin (DDR Pad).

  High-Z : The output pin (DDR Pad) becomes high impedance by controlling of the "High-Z JTAG ctrl".

The Control-Register status is set during Update-DR at the EXTEST or SAMPLE instruction.
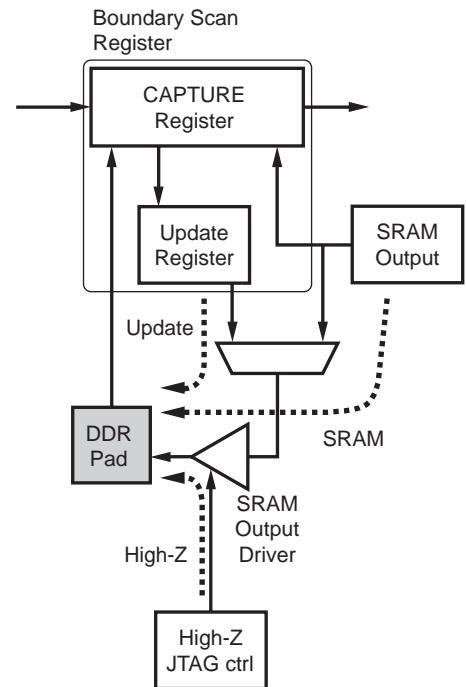
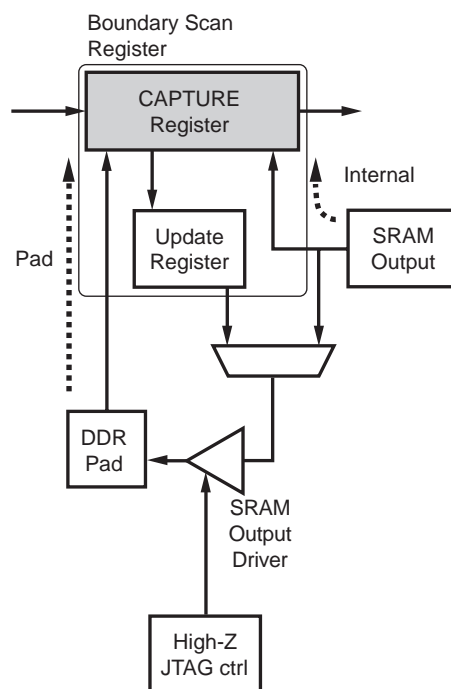**Boundary Scan Register Status of Output Pins CQ, CQ# and DQ**

Instructions	SRAM Status	Boundary Scan Register Status		Note
		CQ,CQ#	DQ	
EXTEST	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
IDCODE	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	
SAMPLE-Z	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
SAMPLE	READ (Low-Z)	Internal	Internal	
	NOP (High-Z)	Internal	Pad	
BYPASS	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	

Remark The Boundary Scan Register statuses during execution each instruction vary according to the instruction code and SRAM operation mode.
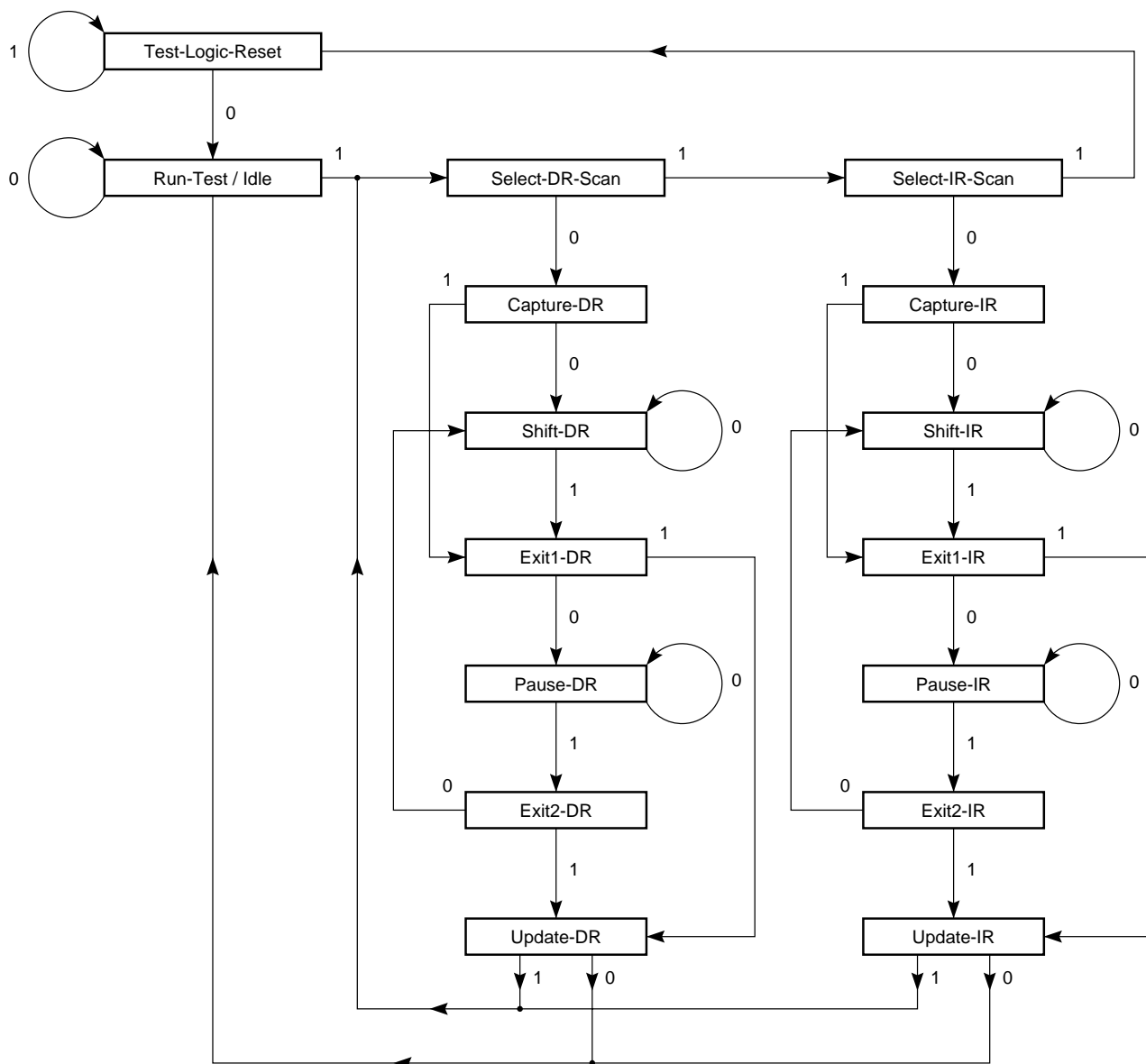There are two statuses:

Pad : Contents of the output pin (DDR Pad) are captured in the "CAPTURE Register" in the Boundary Scan Register.

Internal : Contents of the SRAM internal output "SRAM Output" are captured in the "CAPTURE Register" in the Boundary Scan Register.

TAP Controller State Diagram

Test-Logic-Reset (1 — self loop)

0 → Run-Test / Idle (0 — self loop)

1 → Select-DR-Scan — 1 → Select-IR-Scan — 1 → (back to Test-Logic-Reset)

Select-DR-Scan — 0 → Capture-DR
Select-IR-Scan — 0 → Capture-IR

Capture-DR — 0 → Shift-DR (0 — self loop)
Capture-IR — 0 → Shift-IR (0 — self loop)

Shift-DR — 1 → Exit1-DR
Shift-IR — 1 → Exit1-IR

Exit1-DR — 0 → Pause-DR (0 — self loop); Exit1-DR — 1 → Update-DR
Exit1-IR — 0 → Pause-IR (0 — self loop); Exit1-IR — 1 → Update-IR

Pause-DR — 1 → Exit2-DR
Pause-IR — 1 → Exit2-IR

Exit2-DR — 0 → Shift-DR; Exit2-DR — 1 → Update-DR
Exit2-IR — 0 → Shift-IR; Exit2-IR — 1 → Update-IR

Capture-DR — 1 → Exit1-DR
Capture-IR — 1 → Exit1-IR

Update-DR — 1 → Select-DR-Scan; Update-DR — 0 → Run-Test / Idle
Update-IR — 1 → Select-DR-Scan; Update-IR — 0 → Run-Test / Idle

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS may be left open but fix them to V_{DD} via a resistor of about 1 kΩ when the TAP controller is not used. TDO should be left unconnected also when the TAP controller is not used.
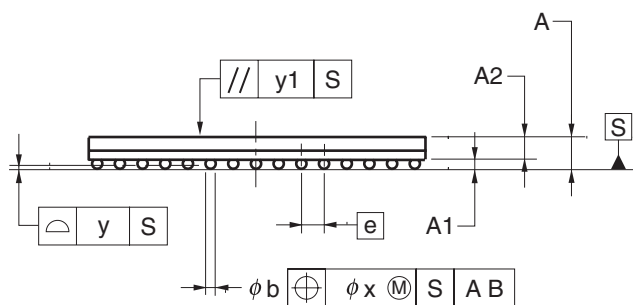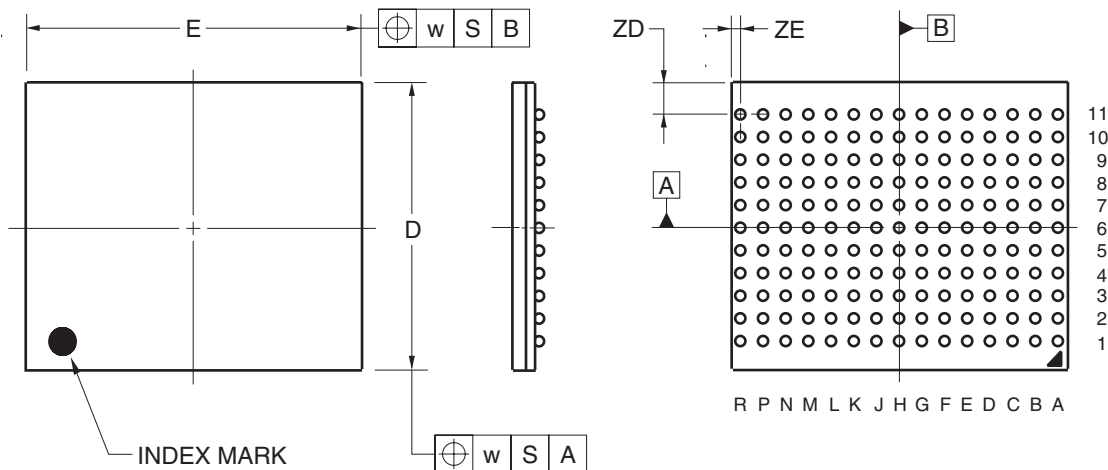
Test Logic Operation (Instruction Scan)

RENESAS
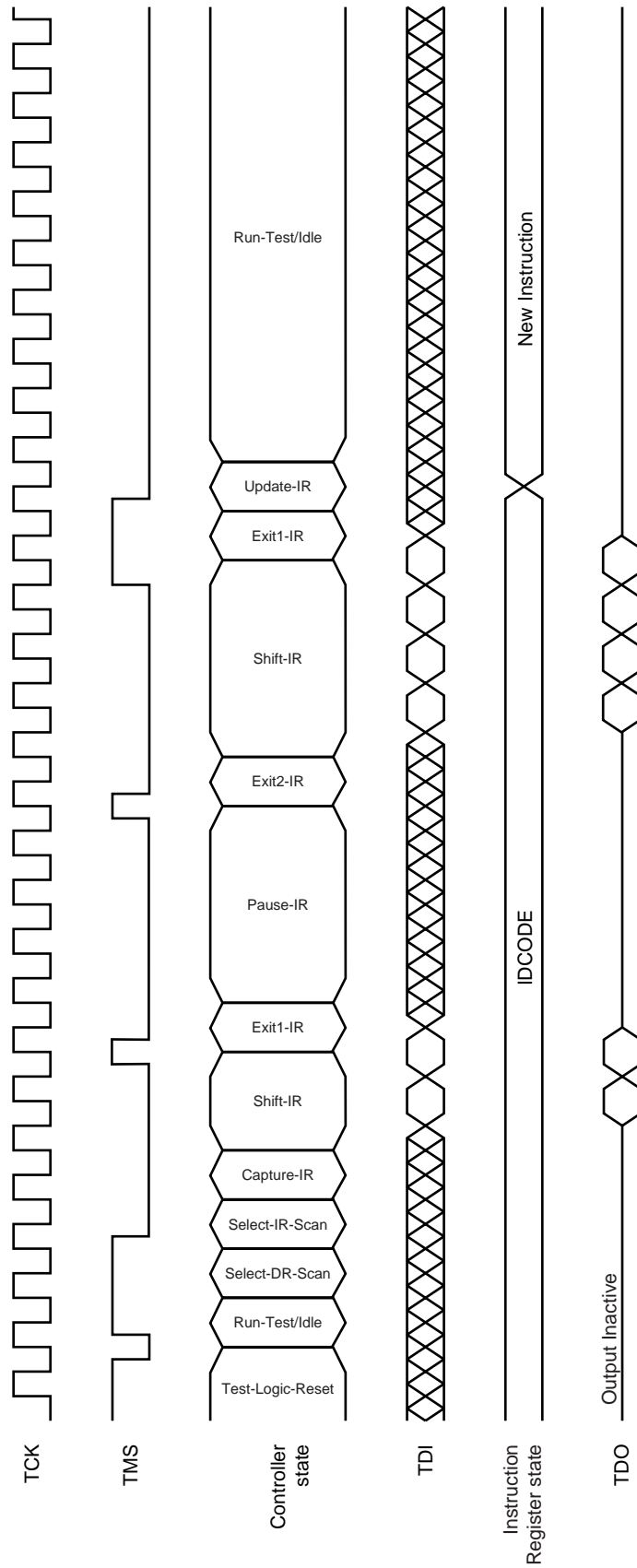
Test Logic (Data Scan)
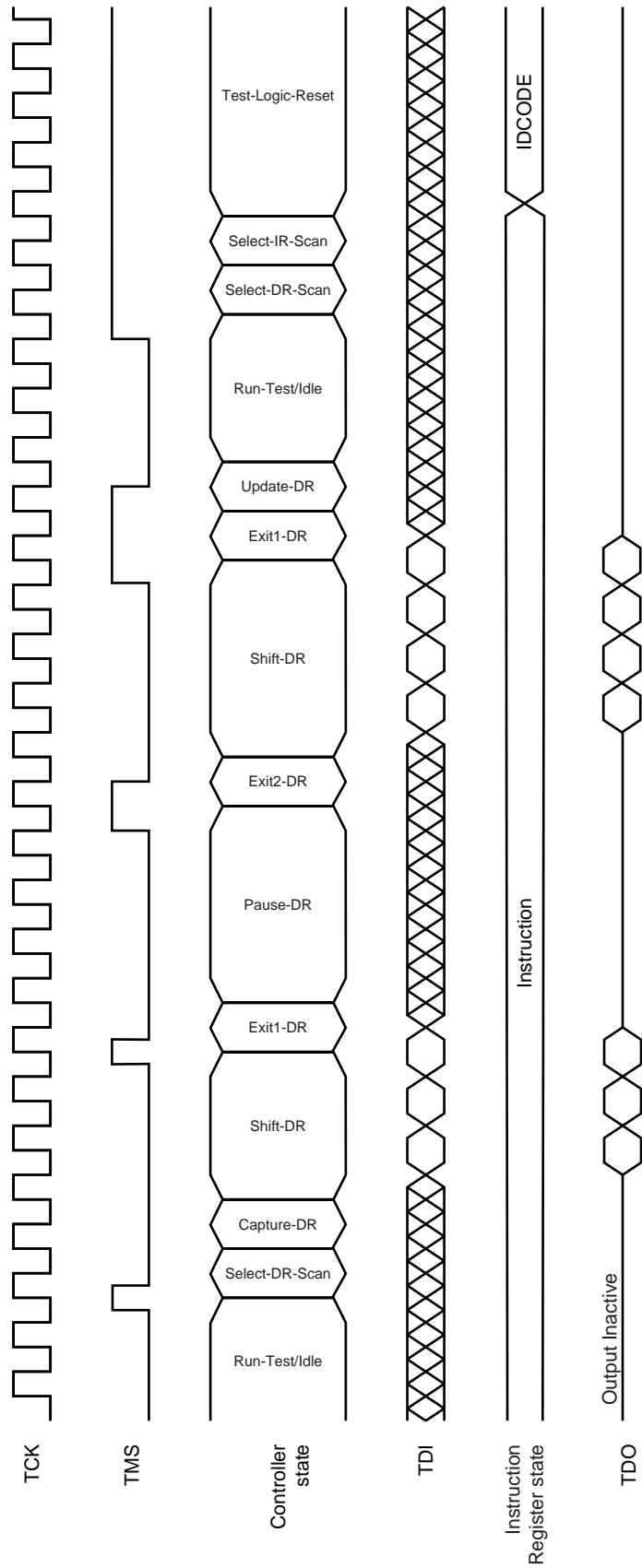
Package Dimensions

165-PIN PLASTIC BGA(13x15)

	(UNIT:mm)
ITEM	**DIMENSIONS**
D	13.00±0.10
E	15.00±0.10
w	0.30
A	1.35±0.11
A1	0.37±0.05
A2	0.98
e	1.00
b	$0.50^{+0.10}_{-0.05}$
x	0.10
y	0.15
y1	0.25
ZD	1.50
ZE	0.50

P165F5-100-EQ3

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD44164184BF5-EQ3 :   165-pin PLASTIC BGA (13 x 15)

Quality Grade

• A quality grade of the products is "Standard".

• Anti-radioactive design is not implemented in the products.

• Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

Revision History			μ**PD44164184B**	

<table>
<tr><th rowspan="2">Rev.</th><th rowspan="2">Date</th><th colspan="3">Description</th></tr>
<tr><th>Page</th><th colspan="2">Summary</th></tr>
<tr><td>1st edition</td><td>'10.02.01</td><td>-</td><td colspan="2">New Preliminary Data Sheet</td></tr>
<tr><td>Rev.0.02</td><td>'10.08.18</td><td>P12</td><td colspan="2">DC Characteristics   (Modification, Spec of I$_{DD}$ and I$_{SB1}$)</td></tr>
<tr><td></td><td></td><td>P13</td><td colspan="2">Thermal Characteristics   (Modification, Spec)</td></tr>
<tr><td>Rev.1.00</td><td>'11.01.05</td><td>P29</td><td colspan="2">Package Dimensions   (Modification, Dimensions)</td></tr>
<tr><td></td><td></td><td>Throughout</td><td colspan="2">Preliminary Data Sheet → Data Sheet</td></tr>
<tr><td>Rev.2.00</td><td>'11.10.06</td><td>Throughout</td><td colspan="2">Add Lead and the extended temperature operation product</td></tr>
</table>

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