STANDARD MICROSYSTEMS CORPORATION

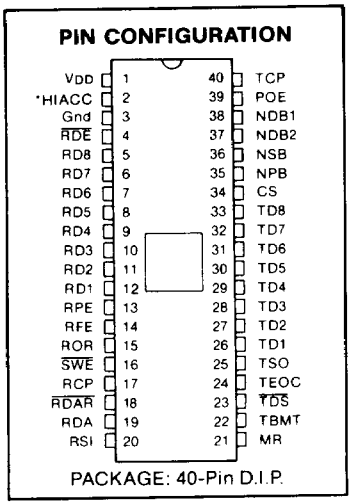
COM 1863
COM 8018
μPC FAMILY

Universal Asynchronous Receiver/Transmitter
UART

FEATURES

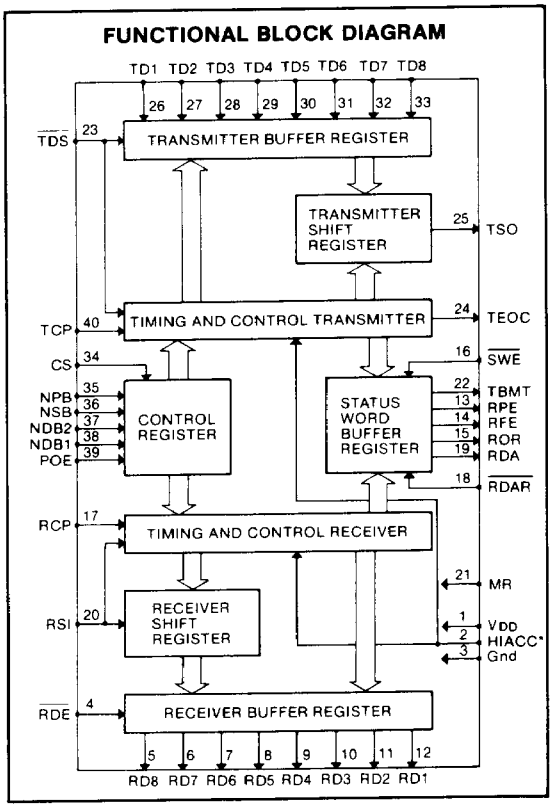
- ☐ Compatible with TR1863 timing
- ☐ High accuracy 32X clock mode 48.4375% Receiver Distortion Immunity and improved RDA/ROR operation (COM 8018 only)
- ☐ High Speed Operation—62.5K baud, 200ns strobes
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Input pull-up options: COM 8018 has low current pull-up resistors; COM 1863 has no pull up resistors
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Improved Start Bit Verification—decreases error rate
- ☐ 46.875% Receiver Distortion Immunity
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ Master Reset—Resets all status outputs and Receiver Buffer Register
- ☐ Three State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic DIP Package—easy board insertion
- ☐ Baud Rates available from SMC's COM 8046, COM 8116, COM 8126, COM 8136, COM 8146 baud rate generators

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1 or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

*If pin 2 is taken to a logic 1 the COM 8018 will operate in a high accuracy mode. If pin 2 is connected to −12V, GND, a valid logic zero, or left unconnected, the high accuracy feature is disabled, and the UART will operate in a 16X clock mode. Pin 2 is not connected on the COM 1863.

DESCRIPTION OF OPERATION—TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied, and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

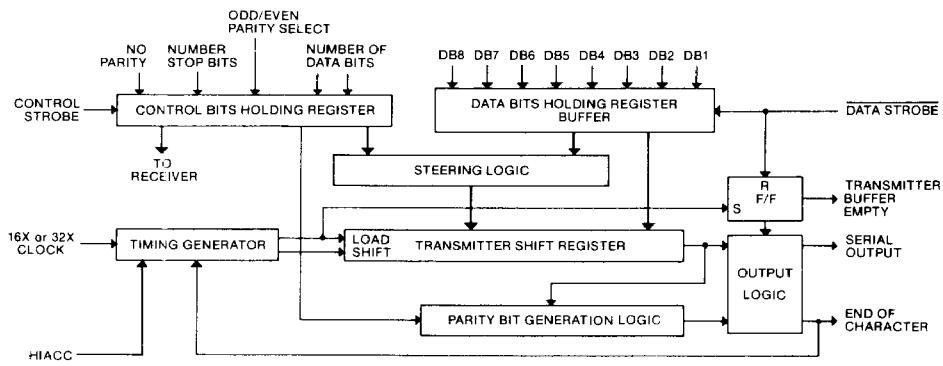
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the data strobe ($\overline{TDS}$) has been pulsed, the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the $\overline{TBMT}$ signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TEOC goes low, TSO goes low (the start bit), and TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

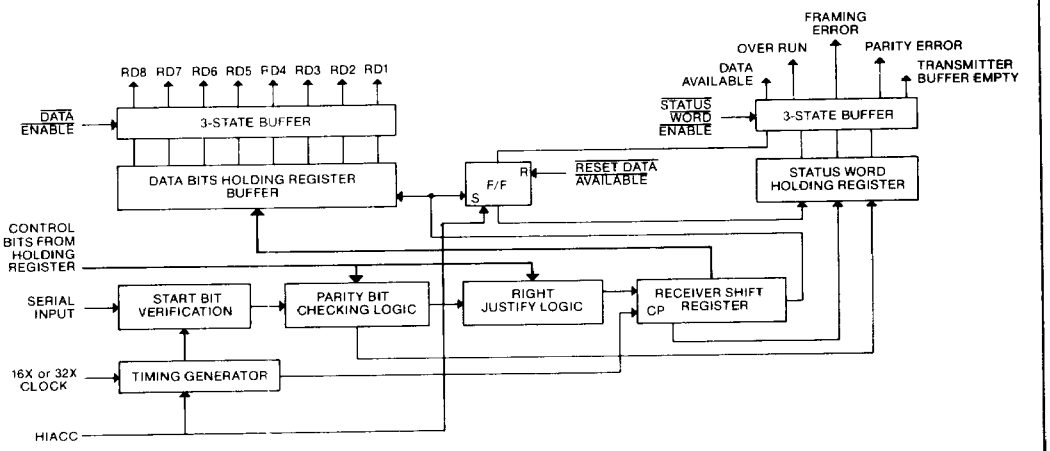
Data reception begins when the serial input line transitions for mark (high) to space (low). If the RSI line remains spacing for 15/32 to 17/32 bit times (in the 16X mode, HIACC = 0) or 31/64 to 33/64 bit times (in the 32X mode, HIACC = 1), a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the received parity bit is incorrect, the parity error flip-flop of the status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, the framing error flip-flop is set high, indicating a framing error.

On the negative RCP edge preceding the stop-bit center sample, internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high, or the $\overline{RDAR}$ signal is low, the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

Subsequently the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{DD}	Power Supply	+5 volt Supply
2	HIACC	High Accuracy Mode	Enables 32X clock and improved RDA/ROR operation. See NOTE on high accuracy mode.
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the eight 3-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

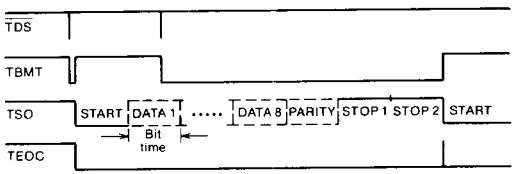
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output reset not completed) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level. $\overline{RDAR}$ must have gone low and come high again before ROR is sampled to avoid overrun indication.
19	RDA	Receiver Data Available	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE, ROR and RD1-RD8 to a low-level.
22	TBMT	Transmitter Buffer Empty	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level during the last half clock cycle of the last stop bit. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted: the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

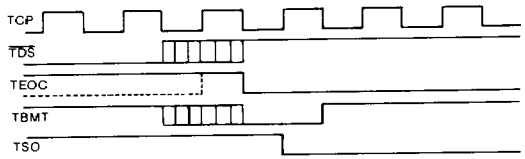
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of two stop bits when programming a 5 data bit word generates 1.5 stop bits.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired transmitter baud rate.

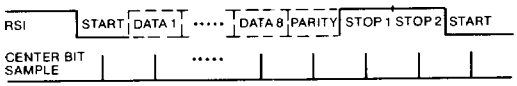
TRANSMITTER TIMING— 8 BIT, PARITY, 2 STOP BITS



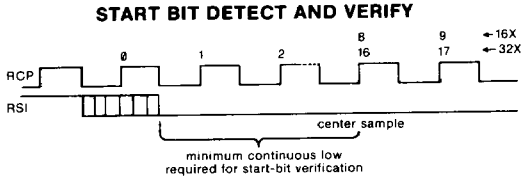
TRANSMITTER START-UP



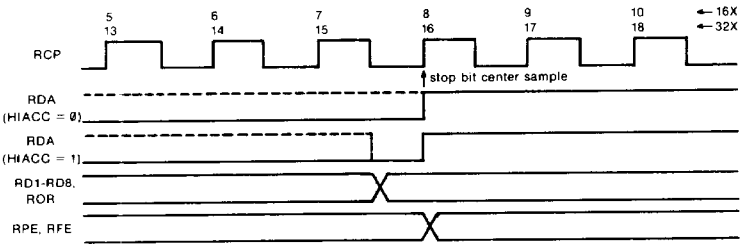
RECEIVER TIMING— 8 BIT, PARITY, 2 STOP BITS



START BIT DETECT AND VERIFY



RECEIVER TIMING DETAIL



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin (except Pin 2), with respect to ground ..... −0.3V
Negative Voltage on Pin 2, with respect to ground ..... −13.2V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	V_{IN} = GND, COM 8018 only
INPUT LEAKAGE			±10	μA	COM 1863 only
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, I_{OS}**			40	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{DD}
A.C. CHARACTERISTICS					T_A = +25°C, See Timing Diagrams
CLOCK FREQUENCY	DC		1.0	MHz	RCP, TCP
PULSE WIDTH					
Clock	0.45			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
ENABLE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			250	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			250	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			250	ns	$\overline{RDE}$, $\overline{SWE}$

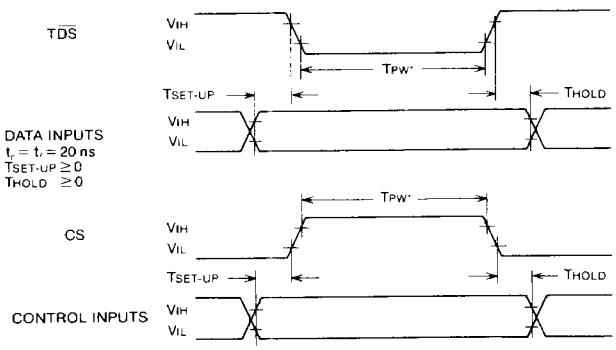
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within 1½ clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one RCP clock period, guaranteeing a maximum start bit slippage of ±1/32 or ±1/64 of a bit time.

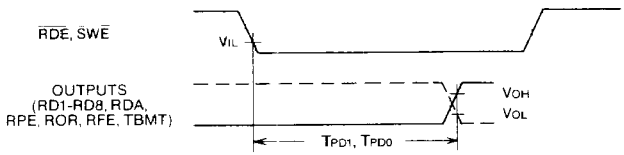
3. The 3-state output has 3 states: 1) low impedance to V_{DD} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM



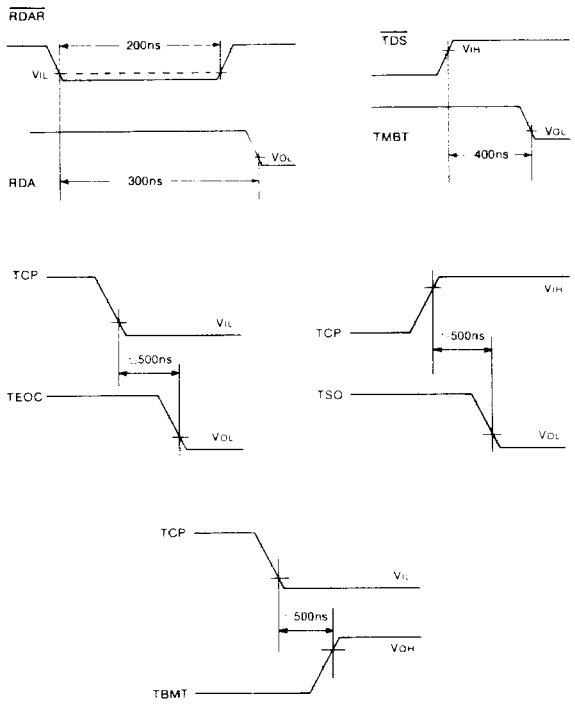
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM



NOTE: Waveform drawings not to scale for clarity.

ADDITIONAL TIMING INFORMATION



NOTES ON COM 8018 AND COM 1863 HIGH-ACCURACY AND IMPROVED RDA/ROR MODE

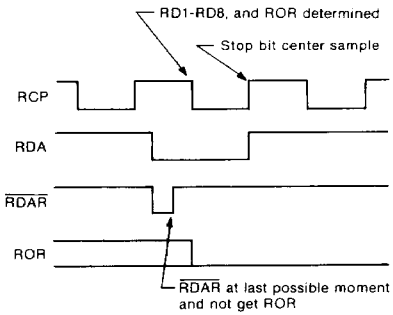
The HIACC mode is enabled by applying a logic "one" to pin 2. If this pin is left unconnected, or connected to GND, −12V, or a logic "zero," the HIACC mode is disabled. The HIACC input has an internal pull-down resistor.

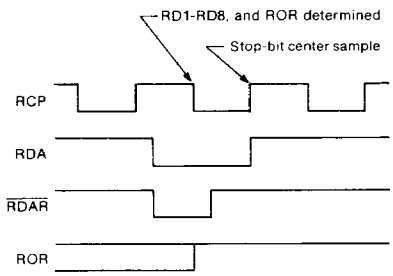
When the HIACC mode is selected, the TX and RX halves both operate on 32X instead of 16X clocks. Also, RDA is notched during the one half receiver clock cycle preceding the stop bit center sample when RD1-RD8 and ROR are changing.

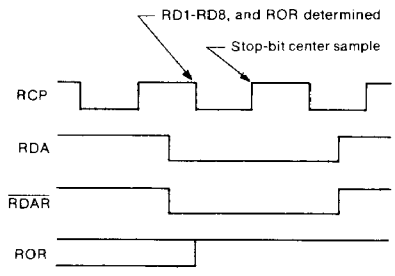
Whether or not the HIACC mode is selected, RDA must be low and $\overline{RDAR}$ must have returned high to avoid setting ROR. If $\overline{RDAR}$ is held low past the stop-bit center sample, RDA will go high after $\overline{RDAR}$ returns high.

The maximum current HIACC will supply if connected to −13.2V is 3.5mA.

IMPROVED RDA/ROR OPERATION TIMING DIAGRAMS



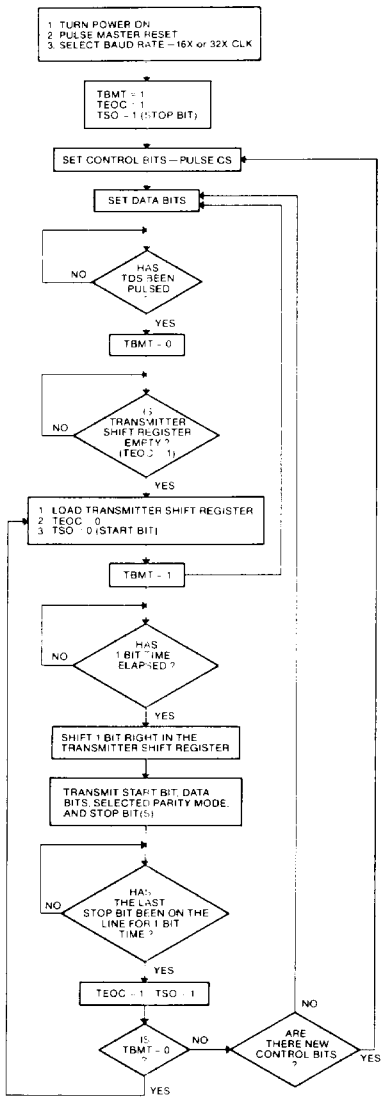




Protection against missing the ROR flag

SECTION III

FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER