Rochester Electronics®

Datasheet

# 54HC113

## *Dual J-K Negative-Edge-Triggered Flip-Flops with Preset*

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC113 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC113 is characterized for operation from -40°C to 85°C.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

FOR REFERENCE ONLY

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

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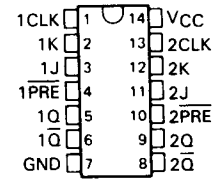
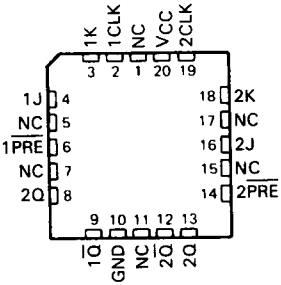
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | H | L |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

**SN54HC113 . . . J PACKAGE**
**SN74HC113 . . . D OR N PACKAGE**
**(TOP VIEW)**

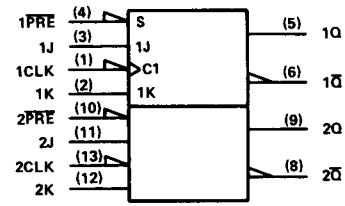



**SN54HC113 . . . FK PACKAGE**
**(TOP VIEW)**




NC—No internal connection

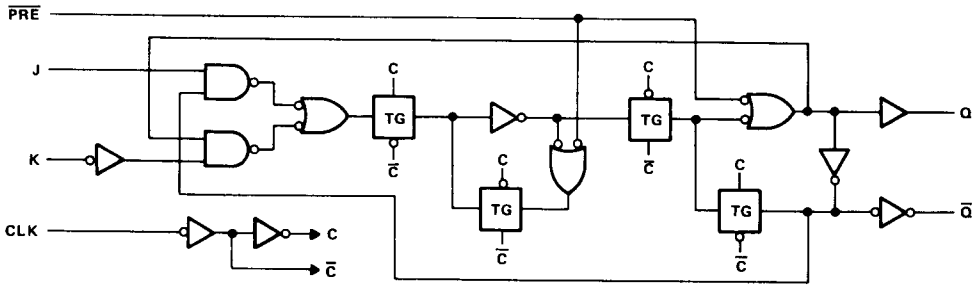
## logic symbol†




†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

2 HCMOS Devices

### logic diagram, each flip-flop (positive logic)




### absolute maximum ratings over operating free-air temperature range†

Supply voltage, $V_{CC}$ . . . . . −0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | SN54HC113 | | | SN74HC113 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | 1.5 | | | V |
| | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | $V_{CC}$ = 6 V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ Low-level input voltage | $V_{CC}$ = 2 V | 0 | | 0.3 | 0 | | 0.3 | V |
| | $V_{CC}$ = 4.5 V | 0 | | 0.9 | 0 | | 0.9 | |
| | $V_{CC}$ = 6 V | 0 | | 1.2 | 0 | | 1.2 | |
| $V_I$ Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ Input transition (rise and fall) times | $V_{CC}$ = 2 V | 0 | | 1000 | 0 | | 1000 | ns |
| | $V_{CC}$ = 4.5 V | 0 | | 500 | 0 | | 500 | |
| | $V_{CC}$ = 6 V | 0 | | 400 | 0 | | 400 | |
| $T_A$ Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC113 | | SN74HC113 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = −20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = −4 mA | 4.5 V | 3.98 | 4.30 | | 3.7 | | 3.84 | | |
| | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = −5.2 mA | 6 V | 5.48 | 5.80 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | $V_I$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | 6 V | | | 4 | | 80 | | 40 | μA |
| $C_i$ | | 2 to 6 V | | 3 | 10 | | 10 | | 10 | pF |

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC113 | | SN74HC113 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | | 4.5 V | | 31 | | 21 | | 25 | |
| | | | 6 V | | 36 | | 25 | | 29 | |
| $t_w$ | Pulse duration | $\overline{PRE}$ low | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 17 | | |
| $t_{su}$ | Setup time before CLK↓ | Data (J, K) | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | $\overline{PRE}$ inactive | 2 V | 25 | | 40 | | 30 | | |
| | | | 4.5 V | 5 | | 8 | | 6 | | |
| | | | 6 V | 4 | | 7 | | 5 | | |
| $t_h$ | Hold time, data after CLK↓ | | 2 V | 0 | | 0 | | 0 | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | |
| | | | 6 V | 0 | | 0 | | 0 | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L$ = 50 pF (see Note 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC113 | | SN74HC113 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 2 V | 6 | 10 | | 4.2 | | 5 | | MHz |
| | | | 4.5 V | 31 | 50 | | 21 | | 25 | | |
| | | | 6 V | 36 | 60 | | 25 | | 29 | | |
| $t_{pd}$ | $\overline{PRE}$ | Q or $\overline{Q}$ | 2 V | | 60 | 165 | | 250 | | 205 | ns |
| | | | 4.5 V | | 18 | 33 | | 50 | | 41 | |
| | | | 6 V | | 15 | 28 | | 43 | | 35 | |
| $t_{pd}$ | CLK | Q or $\overline{Q}$ | 2 V | | 85 | 140 | | 211 | | 175 | ns |
| | | | 4.5 V | | 19 | 28 | | 42 | | 35 | |
| | | | 6 V | | 16 | 24 | | 36 | | 30 | |
| $t_t$ | | Q or $\overline{Q}$ | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

| | | | |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per flip-flop | No load, $T_A$ = 25°C | 35 pF typ |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.





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