1.1 Scope.

This specification covers the detail requirements for an 8-bit microprocessor compatible analog-to-digital converter, which uses the successive approximation technique to achieve a conversion time of 10μs. The part operates with an external reference of +1.23V and converts input signals from 0V to $2V_{REF}$.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number[1]
−1	AD7576S(X)/883B
−2	AD7576T(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3V, +7V
V_{DD} to DGND	−0.3V, +7V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 1–3)	−0.3V, V_{DD}
Digital Output Voltage to DGND (Pins 4, 6–8, 10–14)	−0.3V, V_{DD}
CLK Input Voltage (Pin 5) to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V to V_{DD}
AIN to AGND	−0.3V to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-18 and E-20A
θ_{JA} = 120°C/W for Q-18 and E-20A

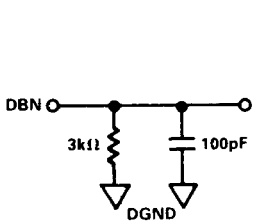
AD7576 – SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{man}–T_{max}	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	–1,2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error	TUE	–1 –2	2 1	2 2	2 1	 1		± LSB max
Relative Accuracy	RA	–1 –2	1 0.5	1 1	1 0.5	 0.5		± LSB max
Full-Scale Error		–1,2	1	1	1			± LSB max
Offset Error		–1,2	0.5	0.5	0.5		Measured with respect to an ideal first code transition which occurs at 1/2LSB.	± LSB max
Analog Input Voltage Range	AIN	–1,2	0 to $2V_{REF}$					V
DC Input Impedance	Z_{IN}	–1,2	10	10	10			MΩ min
Reference Input Current	I_{REF}	–1,2	500	500	500			μA max
Digital Input Low Voltage	V_{IL}	–1,2	0.8	0.8	0.8		$\overline{CS}$, $\overline{RD}$, MODE, CLK	V max
Digital Input High Voltage	V_{IH}	–1,2	2.4	2.4	2.4		$\overline{CS}$, $\overline{RD}$, MODE, CLK	V min
Digital Input Current	I_{IN}	–1,2	10	1	10		$\overline{CS}$, $\overline{RD}$, MODE V_{IN} = 0 or V_{DD}, V_{DD} = 5.2V	± μA max
Digital Input Capacitance	C_{IN}	–1,2	10				$\overline{CS}$, $\overline{RD}$, MODE	pF max
Digital Input Low Current	I_{IL}	–1,2	800	800	800		CLK; V_{IL} = 0V	μA max
Digital Input High Current	I_{IH}	–1,2	800	800	800		CLK; V_{IH} = V_{DD}	μA max
Digital Output Low Voltage	V_{OL}	–1,2	0.4	0.4	0.4		$\overline{BUSY}$, DB0 to DB7 I_{SINK} = 1.6mA, V_{DD} = 4.75V	V max
Digital Output High Voltage	V_{OH}	–1,2	4.0	4.0	4.0		$\overline{BUSY}$, DB0 to DB7 I_{SOURCE} = 40μA, V_{DD} = 4.75V	V min
Floating State Leakage Current	I_{OUT}	–1,2	10	10	10		DB0 to DB7 V_{OUT} = 0 to V_{DD}, V_{DD} = 5.2V	± μA max
Floating State Output Capacitance	C_{OUT}	–1,2	10				DB0 to DB7	pF max
Conversion Time with External Clock	t_{CONV}	–1,2	10	10	10		f_{CLK} = 2MHz	μs
Conversion Time with External Clock @ +25°C	t_{CONV}	–1,2	10 30			10 30	Recommended Clock Components: R = 150kΩ, C = 150pF	μs min μs max
$\overline{CS}$ to $\overline{RD}$ Setup Time, t_1	t_{WSCS}	–1,2	0					ns min
$\overline{RD}$ to BUSY Propagation Delay, t_2	t_{WBPD}	–1,2	120					ns max
Data Access Time after $\overline{RD}$[2], t_3	t_{DAR}	–1,2	120					ns max
$\overline{RD}$ Pulse Width, t_4	t_{RD}	–1,2	120					ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time, t_5	t_{RHS}	–1,2	0					ns min
Data Access Time after $\overline{BUSY}$, t_6	t_{DAB}	–1,2	100					ns max
Data Hold Time, t_7[3]	t_{DH}	–1,2	10 100					ns min ns max
$\overline{BUSY}$, to $\overline{CS}$ Delay, t_8	t_{BCD}	–1,2	0					ns min
Power Supply Current	I_{DD}	–1,2	7	7	7		V_{DD} = 5.2V	mA max
Power Supply Rejection		–1,2	0.25	0.25	0.25			± LSB max

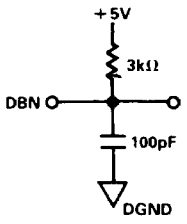
NOTES
[1]V_{DD} = +5V; (except where otherwise mentioned) V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 2MHz external. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V to 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Table 1.

REV. B

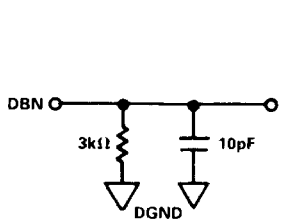


a. High-Z to V_{OH}

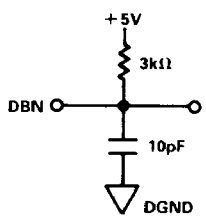


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



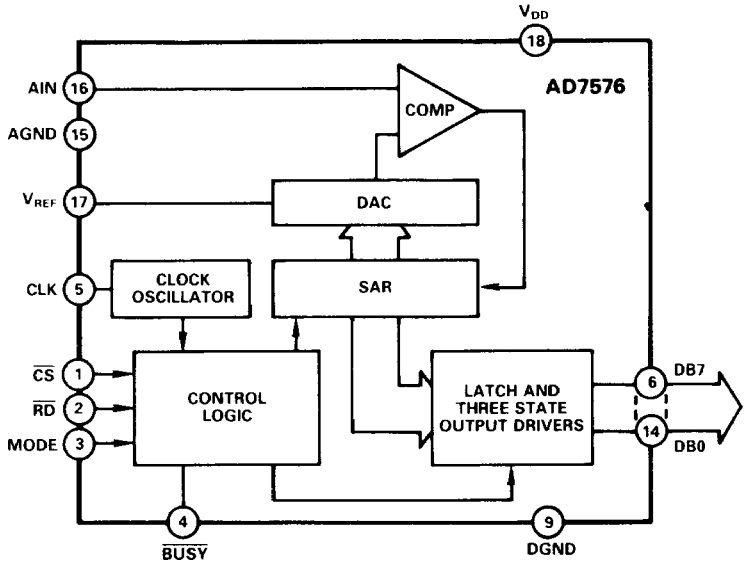
a. V_{OH} to High-Z



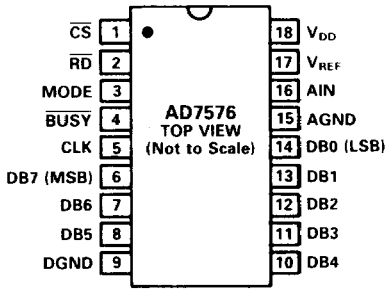
b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

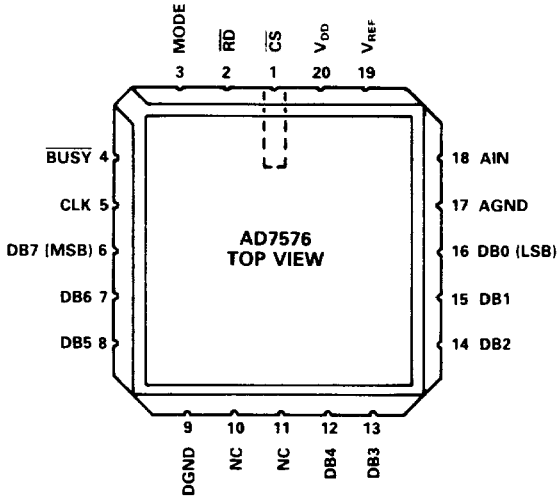
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)

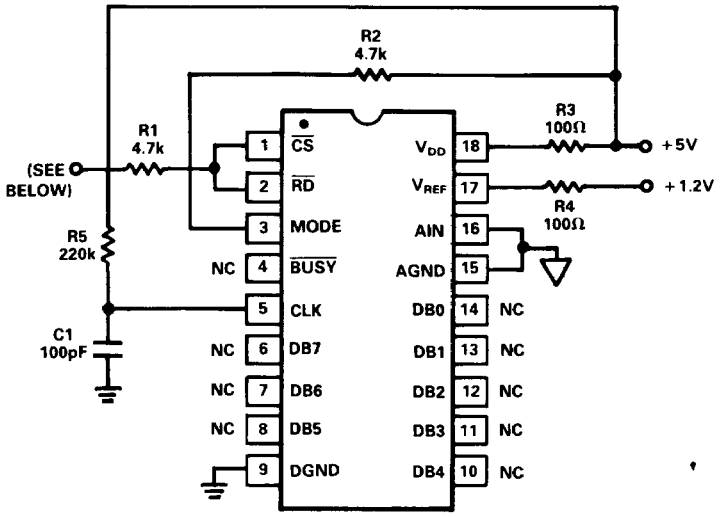


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

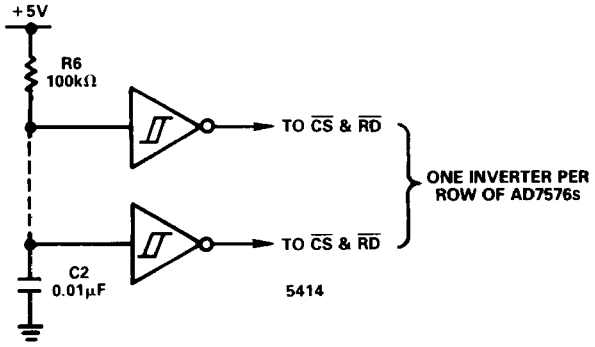
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).



ALL RESISTORS ARE 1/4W.
$\overline{CS}$ AND $\overline{RD}$ ARE TAKEN HIGH FOR 0.6ms – 0.7ms APPROXIMATELY AND ARE THEN BROUGHT LOW. THIS IS ACHIEVED AS FOLLOWS:

NOTE
$\overline{CS}/\overline{RD}$ PULSE MAY BE GENERATED EXTERNALLY.



5.0 Timing and Control of the AD7576.

The AD7576 is capable of two basic operating modes which are outlined in the timing diagrams below. These two operating modes are an Asynchronous Conversion Mode and a Synchronous Conversion Mode. The selection of the required operating mode is determined by the status of the MODE pin. When this pin is HIGH, the device performs conversions only when the required control signals ($\overline{CS}$ and $\overline{RD}$) are applied; with this pin LOW the device performs continuous conversions and $\overline{CS}$ and $\overline{RD}$ are used only to access the output data.

5.1 Synchronous Conversion Mode.

In the Synchronous Conversion mode the AD7576 will perform a conversion when requested to do so by the microprocessor. The MODE pin of the AD7576 is tied HIGH to place the device in Synchronous Conversion operation. Two interface options exist for reading the output data from the AD7576.

5.1.1 Slow Memory Interface.

The first of these interface options is intended for use with microprocessors which can be forced into a WAIT STATE for at least 10μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7576 address. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor in a WAIT state. When conversion is complete ($\overline{BUSY}$ goes HIGH) the processor completes the memory READ.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the AD7576 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time. The timing diagram for this interface is shown in Figure 3.

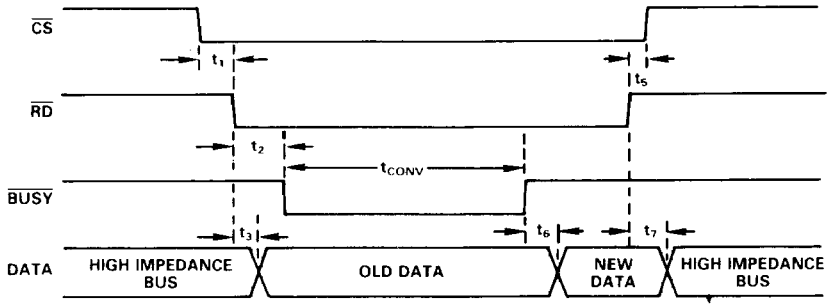


Figure 3. Slow Memory Interface Timing Diagram

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7576 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is 0 for a READ cycle) provides the READ signal to the AD7576. The AD7576 connection diagram to the 8085A-2 is shown in Figure 4.

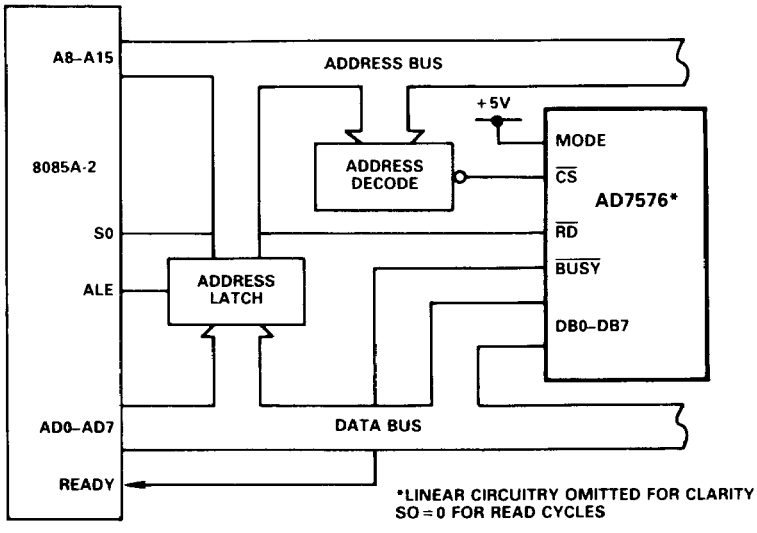


Figure 4. AD7576 to 8085A-2 Slow Memory Interface

5.1.2 ROM Interface.

The alternative interface option in the Synchronous Conversion mode avoids placing the microprocessor into a WAIT state. In this interface, conversion is started with the first read instruction and a second read instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5 while Figure 6 shows the connection diagram for the AD7576 with the 6502/6809 microprocessors.

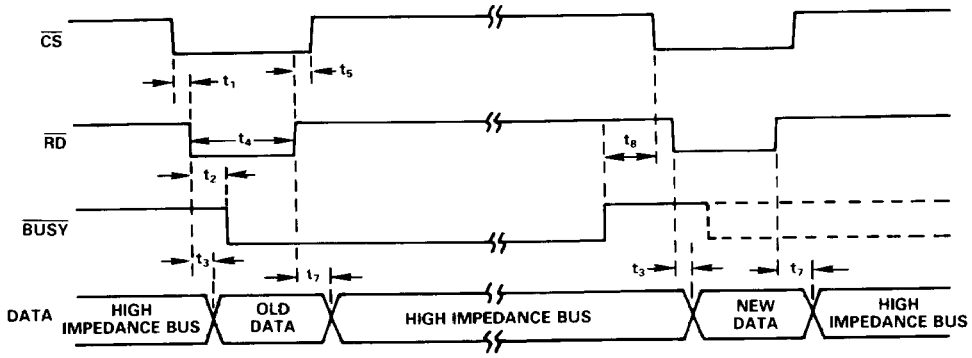


Figure 5. ROM Interface Timing Diagram

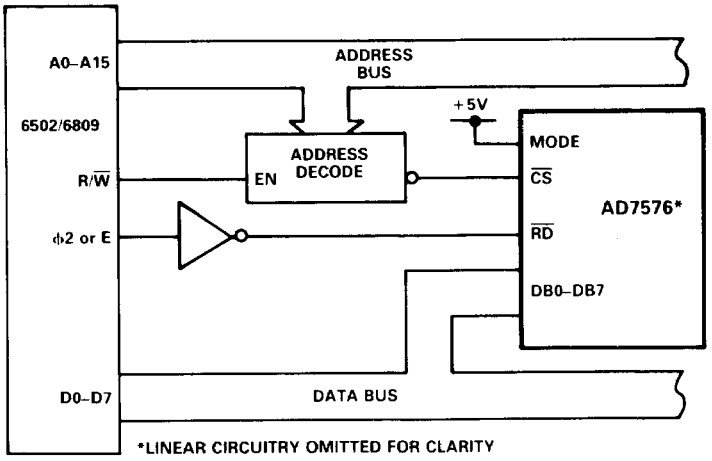


Figure 6. AD7576 to 6502/6809 ROM Interface

Conversion is initiated by executing a memory READ instruction to the AD7576 address. Data is also obtained from the AD7576 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW during conversion and returns HIGH when conversion is complete.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor indicating that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7576 conversion time. For the AD7576 to operate correctly in the ROM Interface mode $\overline{CS}$ and $\overline{RD}$ should not go low before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

REV. B

5.2 Asynchronous Conversion Mode.

When the MODE pin of the AD7576 is tied LOW, the device performs continuous conversions, and the control lines $\overline{CS}$ and $\overline{RD}$ are used only to read the data from the converter. The timing diagram for this operating mode is outlined in Figure 7, with the connection diagram to the 8085A shown in Figure 8.

Data is obtained from the AD7576 by executing a memory READ instruction to its address. The A/D process is completely transparent to the microprocessor and the AD7576 will behave like a ROM. Data may be read at any time completely independent of the clock. This is especially useful in internal clock applications where the user no longer has to worry about synchronizing the clock with the READ line of the microprocessor.

The data latches are normally updated by $\overline{BUSY}$ going HIGH. However, if $\overline{CS}$ and $\overline{RD}$ are LOW when $\overline{BUSY}$ goes HIGH, the contents of the data latches are frozen until $\overline{CS}$ or $\overline{RD}$ returns HIGH. This ensures that incorrect data cannot be read from the AD7576. The output latches are updated when $\overline{CS}$ or $\overline{RD}$ return HIGH and the converter is re-enabled. If $\overline{CS}$ or $\overline{RD}$ do not return HIGH the AD7576 will stop performing continuous conversions, and will not start again until either line goes HIGH.

The advantage of this mode is its simplicity. The disadvantage of this mode is that the data which is read is not clearly defined in time. However, it will not be older than one conversion period and if this uncertainty is a problem it can be overcome by monitoring the $\overline{BUSY}$ line.

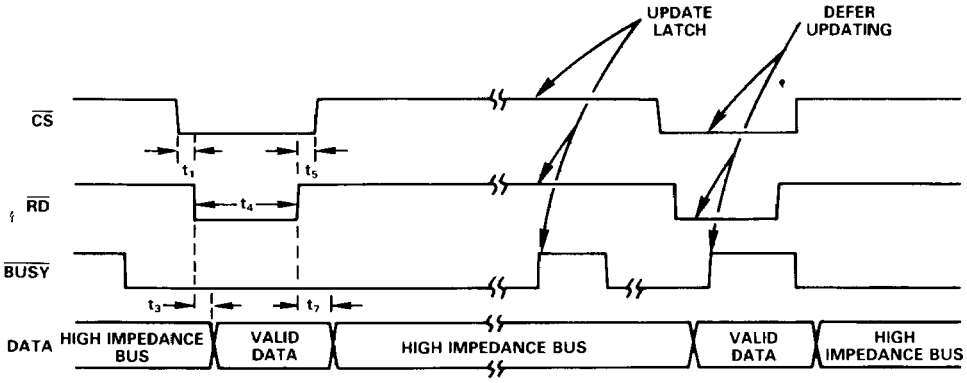


Figure 7. Asynchronous Conversion Mode Timing Diagram

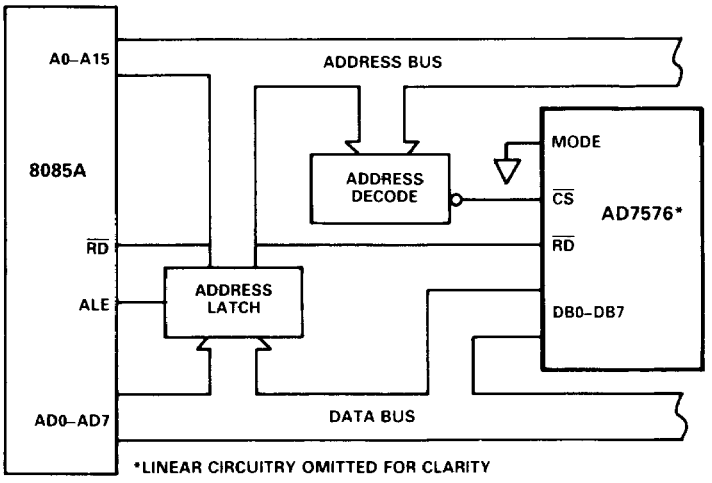


Figure 8. AD7576 to 8085A Asynchronous Conversion Mode Interface