

SEMICONDUCTOR®

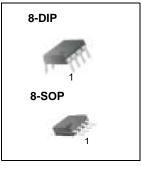
KA3882C/KA3883C SMPS Controller

Features

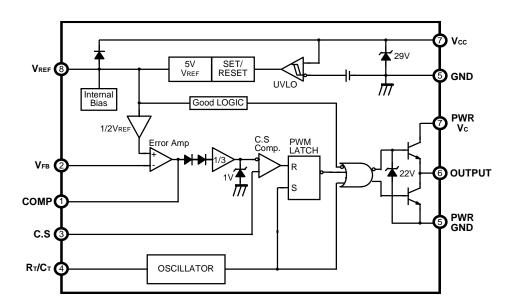
- Low Start Current 0.2mA (typ)
- Operating Range Up To 500KHz
- Cycle by Cycle Current Limiting
- Under Voltage Lock Out With Hysteresis
- Short Shutdown Delay Time: typ.100ns
- High Current Totem-pole Output
- Output Swing Limiting: 22V

Description

The KA3882C/KA3883C are fixed PWM controller for Off Line and DC to DC converter applications. The internal circuits include UVLO, low start up current circuit, temperature compensated reference, high gain error amplifier, current sensing comparator, and high current totem pole output for driving a POWER MOSFET. Also KA3882C/KA3883C provide low start up current below 0.3mA and short shutdown delay time typ. 100ns. The KA3882C has UVLO threshold of 16V(on) and 10V(off). The KA3883C is 8.4V(on) and 7.6V(off). The KA3882C and KA3883C can operate within 100% duty cycle.



Internal Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	30	V
Output Current	IO	± 1	A
Analog Inputs (pin 2, 3)	VI(ANA)	- 0.3 to 6.3	V
Error Amp. Output Sink Current	ISINK(EA)	10	mA
Power Dissipation	PD	1	W
Thermal Resistance, Junction-to-Air (Note4) 8-SOP 8-DIP	Rθja	280 95	°C/W
Storage Temperature	T _{stg}	-65 ~ 150	°C

Electrical Characteristics

(V_{CC} = 15V, R_T = 10K Ω , C_T = 3.3nF, T_A = 0°C to + 70°C ,Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	
REFERENCE SECTION							
Output Voltage	VREF	TJ = 25°C, IO = 1mA	4.9	5.0	5.1	V	
Line Regulation	$\Delta VREF$	Vcc = 12V to 25V	-	6	20	mV	
Load Regulation	$\Delta VREF$	IO = 1mA to 20mA	-	6	25	mV	
Output Short Circuit	ISC	$T_a = 25^{\circ}C$	-	- 100	- 180	mA	
OSILLATOR SECTION	OSILLATOR SECTION						
Initial Accuracy	Fosc	TJ = 25°C	47	52	57	KHz	
Voltage Stability	STγ	VCC = 12V to 25V	-	0.2	1	%	
Amplitude	Vosc	VPIN4, Peak to Peak	-	1.7	-	V	
Discharge Current	IDISCHG	TJ = 25°C, Pin4 = 2V	7.8	8.3	8.8	mA	
CURRENT SENSE SECTION							
Gain	Gv	(NOTE 2, 3)	2.85	3	3.15	V/V	
Maximum Input Signal	VI(MAX)	VPIN1 = 5V(NOTE 2)	0.9	1.0	1.1	V	
PSRR	PSRR	VCC = 12V to 25V (NOTE 1, 2)	-	70	-	dB	
Input Bias Current	IBIAS	-	-	- 2	-10	uA	
Delay to Output	TD	VPIN3 = 0 V to 2V (NOTE1)	-	100	200	ns	

Electrical Characteristics (Continued)

(VCC = 15V, RT = 10K Ω , CT = 3.3nF, TA = 0°C to + 70°C, Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
ERROR AMPLIFIER SECTIO	N		1			
Input Voltage	VI	TPIN1 = 2.5V	2.42	2.50	2.58	V
Input Bias Current	IBIAS	-	-	-0.3	- 2	uA
Open Loop Gain	Gvo	$V_O = 2V$ to 4V (NOTE 1)	65	90	-	dB
Unity Gain Bandwidth	GBW	TJ= 25°C (NOTE 1)	0.7	1	-	MHz
PSRR	PSRR	Vcc = 12V to 25V (NOTE 1)	60	70	-	dB
Output Sink Current	ISINK	VPIN2 = 2.7V VPIN1 = 1.1V	2	6	-	mA
Output Source Current	ISOURCE	VPIN2 = 2.3V VPIN1 = 5.0V	-0.5	-0.8	-	mA
Output High Voltage	Vон	V _{PIN2} = 2.3V R1 = 15KΩ to GND	5	6	-	V
Output Low Voltage	Vol	V _{PIN2} = 2.7V R1 = 15KΩ to Pin8		0.8	1.1	V
OUTPUT SECTION	 				ļ	J
Output Low Level	Vol	ISINK = 20mA	-	0.1	0.4	V
		ISINK = 200mA	-	1.5	2.2	V
Output High Level	Vон	ISOURCE = 20mA	13	13.5	-	V
		ISOURCE = 200mA	12	13.5	-	V
Rise Time	tR	TJ = 25°C, C1 = 1nF (NOTE 1)	-	40	100	ns
Fall Time	tF	TJ = 25°C, C1 = 1nF (NOTE 1)	-	40	100	ns
Output Voltage Swing Limit	Volim	VCC = 27V, C1 = 1nF	-	22	-	V
UNDER VOLTAGE LOCKOU	T SECTION					
Start Threshold	Vтн	KA3882C	15	16	17	V
Start Threshold	VIП	KA3883C	7.8	8.4	9.0	V
Min. Operating Voltage	VTL	KA3882C	9	10	11	V
(After turn on)		KA3883C	7.0	7.6	8.2	V
PWM SECTION						
Maximum Duty Cycle	DMAX	KA3882C/KA3883C	94	96	100	%
Minimum Duty Cycle	DMIN	-	-	-	0	%
TOTAL STANDBY CURREN	г <u> </u>					
Start-Up Current	IST	-	-	0.2	0.4	mA
Operating Supply Current	lcc	VPIN2 = VPIN3 = 0V	-	11	17	mA
VCC Zener Voltage	Vz	ICC = 25mA	-	29	-	V

* Adjust VCC above the start threshold before setting at 15V **Notes :**

1. These parameters, although guaranteed, are not 100% tested in production.

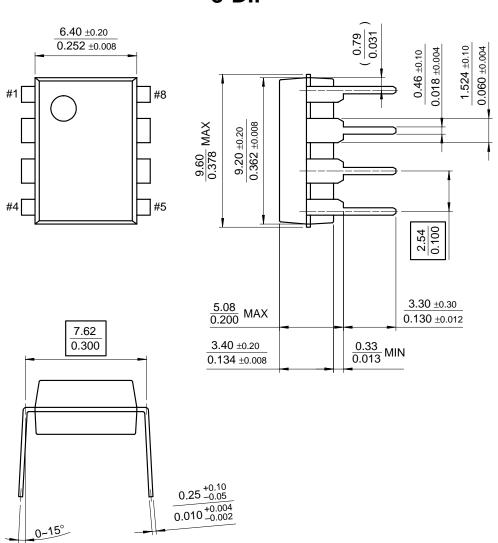
- 2. Parameter measured at trip point of latch with V2 = 0V.
- 3. Gain defined as: $G_V = \Delta V_{PIN1} \Delta V_{PIN3} (V_{PIN3} = 0 \text{ to } 0.8V)$
- 4. Junction-to-air thermal resistance test enviroments.

-. PCB information ; Board thickness : 1.6mm , Board dimension : 76.2 X 114.3mm² , Ref. : EIA / JSED51-3 and EIA / JSED51-7

-. Board structure; Using the single layer PCB.

Mechanical Dimensions

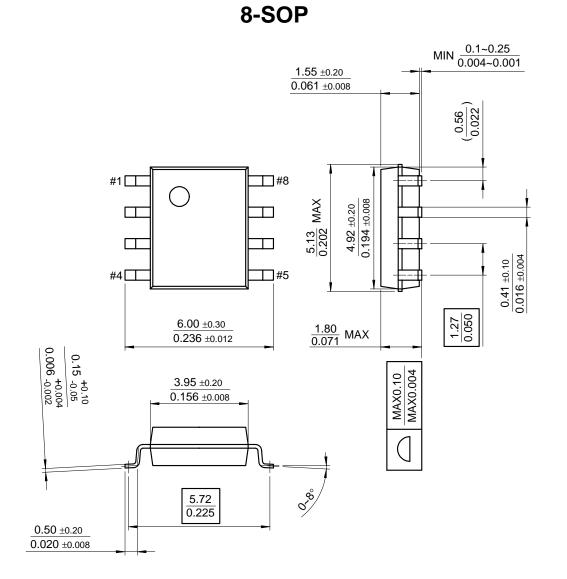
Package



8-DIP

Mechanical Dimensions (Continued)

Package



Ordering Information

Product Number	Package	Operating Temperature
KA3882C	8-DIP	
KA3882CD	8-SOP	0 ~ + 70°C
KA3883C	8-DIP	0~+70 C
KA3883CD	8-SOP	

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Features

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- Operating range up to 500KHz
- Cycle by cycle current limiting
- Under voltage lock out with hysteresis
- Short shutdown delay time: Typ. 100ns
- High current totem-pole output
- Output swing limiting: 22V

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Product status/pricing/packaging

Product Folder - Fairchild P/N KA3842A - SMPS Controller

Product	Product status	Package type	Leads	Packing method
KA3842ACDS	Full Production	SOIC	8	RAIL
KA3842ACS	Full Production	DIP	8	RAIL
KA3842ACDSTF	Full Production	SOIC	8	TAPE REEL
KA3842AES	Full Production	DIP	8	RAIL

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