November 21, 2006

Notice – PMC Product Support Scope for Specified HDMP Part Numbers

Distribution:

This notice has been added to the front of the datasheets for the “Devices Affected” listed below.

Description:

PMC-Sierra has acquired the Fibre Channel/Storage and Gigabit Ethernet Port Bypass Controllers and SERDES/PHY products of Agilent/Avago Technologies. This notice is to inform customers that PMC-Sierra is supporting these devices for existing production designs only. PMC-Sierra will only provide support for the migration of an existing design from a Pb package to a Pb-free package. The devices are not intended for new designs and PMC-Sierra will not provide support for new designs.

Devices Affected:

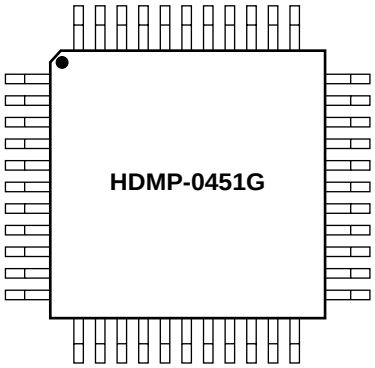
Device	Data Sheet	Device	Data Sheet	Device	Data Sheet
HDMP-0421G	PMC-2060481*	HDMP-1022G	PMC-2060487	HDMP-1638G	PMC-2060490
HDMP-0422G	PMC-2060482*	HDMP-1024G	PMC-2060487	HDMP-1646AG	PMC-2060491
HDMP-0450G	PMC-2060483	HDMP-1032AG	PMC-2060488	HDMP-1646AGR1	PMC-2060491
HDMP-0451G	PMC-2060484	HDMP-1034AG	PMC-2060488	HDMP-1687G	PMC-2060493
HDMP-0452G	PMC-2060485*	HDMP-1536AG	PMC-2060489	HDMP-T1636AG	PMC-2060491
HDMP-0480G	PMC-2062505*	HDMP-1636AG	PMC-2060491		
HDMP-0482G	PMC-2060486	HDMP-1636AGR1	PMC-2060491		

* Note – These data sheets have part numbers that reference Pb packaging. All part numbers listed above are for Pb-free packaging.

Customer Response

This notice is for customer information only and no customer response is required. If you have any questions or concerns please contact your local PMC-Sierra Sales Representative listed at this link http://www.pmc-sierra.com/contactSales/

PMC-Sierra Port Bypass Circuits for Fibre Channel Arbitrated Loop Standard and Its Extensions
Data Sheet



HDMP-0451G Quad PBC & CDR

Features

- Supports ANSI X3T11 1.0625 Gbps FC-AL loop configuration
- Supports 802.3z 1.25 Gbps Gigabit Ethernet (GE) rates
- Quad PBCs in a single package
- Clock and Data Recovery (CDR) at entry, or at exit, or after any cell
- CDR location determined by wiring configuration of pins on PCB (patent pending)
- Envelope detect on cable input (SD) for CDR at entry case
- Equalizers on all inputs
- High speed PECL I/Os referenced to V_{CC}
- Buffered Line Logic (BLL) outputs remove need for external resistors
- 0.7 W typical power at V_{CC} = 3.3 V
- 5 V tolerant LVTTL I/O
- 44 pin, 10 mm, low cost plastic QFP

Applications

- RAID, JBOD cabinets
- 1=> 1-4 serial buffer with or without CDR

Description

The HDMP-0451G is a Quad Port Bypass Circuit (PBC). Four Fibre Channel PBCs are combined into a daisy chain in a single integrated circuit. In addition, a single clock and data recovery (CDR) circuit is provided. This configuration will minimize part count, cost, jitter accumulation, and will repeat incoming signals without an additional CDR IC. Port Bypass Circuits are used to provide loops that are continuously on in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. Hard disks may be pulled out or swapped while other disks in the array are available to the system.

A Port Bypass Circuit is a 2:1 Multiplexer array with two modes of operation: DISK IN LOOP and DISK BYPASSED. In DISK IN LOOP mode, the loop goes into and out of the disk drive. Data go from the HDMP-0451G's TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC (for example, an HDMP-15X6) Rx± differential input pins. Data from Disk Drive Transceiver IC Tx± differential output pins go to HDMP-0451G's FM_NODE[n]± differential input pins. Figures 4 and 5 show connection diagrams for disk drive array applications. In DISK BYPASSED mode, the disk drive is either absent or nonfunctional and the loop bypasses the hard disk. DISK IN LOOP mode is enabled with a HIGH on the BYPASS[n]– pin and DISK BYPASSED mode is enabled with a LOW on the same pin.

Multiple HDMP-0451Gs may be cascaded or connected to other members of the HDMP-04XXG family through the FM_LOOP and TO_LOOP pins to create loops for arrays of disk drives greater than 4. See Table 2 to identify which of the 5 cells (0:4) will provide FM_LOOP, TO_LOOP pins (cell connected to cable). Combinations of Quad PBCs can be utilized to accommodate any number of

hard disks. The unused cells in a quad may be bypassed with pulldown resistors on the BYPASS[n]– pins for these cells. An HDMP-0451G can be wired as a single or double mux cell with a CDR. It may also be used as a single or double mux cell without a CDR. All TO_NODE outputs of HDMP-0451G are of equal strength. Therefore, this part may be used as a 1=>1- 4 buffer.

The design of HDMP-0451G allows for placement of CDR at any location with respect to hard disk slots. For example, if BYPASS[0]– pin is tied to V_{CC} and hard disk slots A to D are connected to PBC cells 1 to 4 in the same order, CDR function will be performed at entry to the HDMP-0451G (Figure 4). To achieve a CDR function at exit from the HDMP-0451G, BYPASS[1]– must be tied to V_{CC} and hard disk slots A to D must be connected to PBC cells 2,3,4,0 in that order (Figure 5). Table 2 shows all possible connections. In case of CDR at entry, a Signal Detect (SD) pin shows the status of the signal at the incoming cable. The recommended method of setting the BYPASS[i]– pins HIGH is to drive them with a high-impedance signal. Internal pull-up resistors will force the BYPASS[i]– pins to V_{CC}.

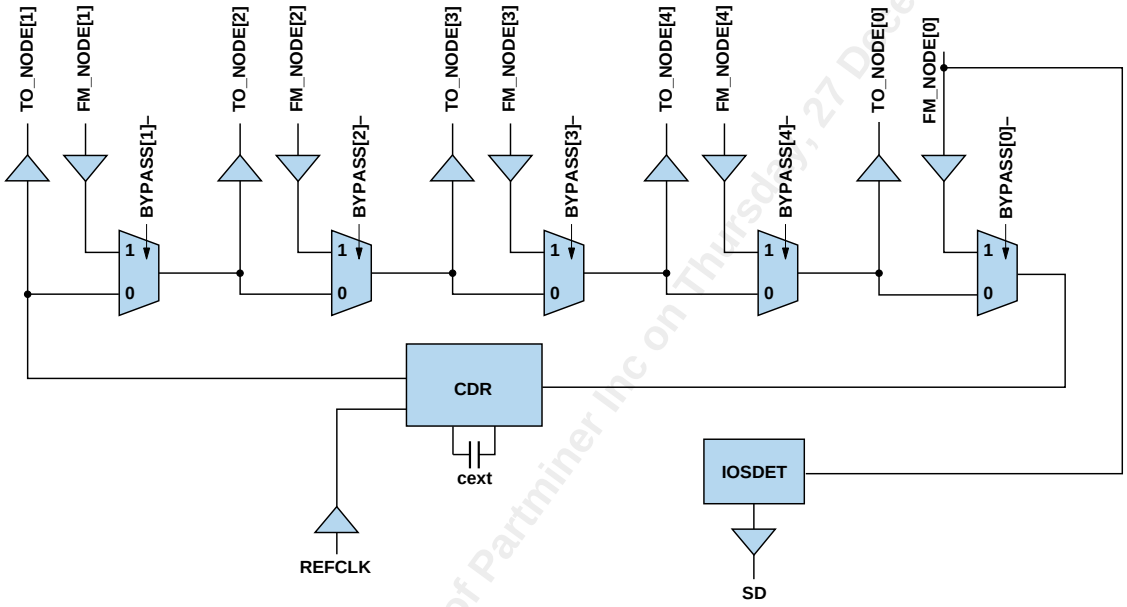


Figure 1. Block diagram of HDMP-0451G.

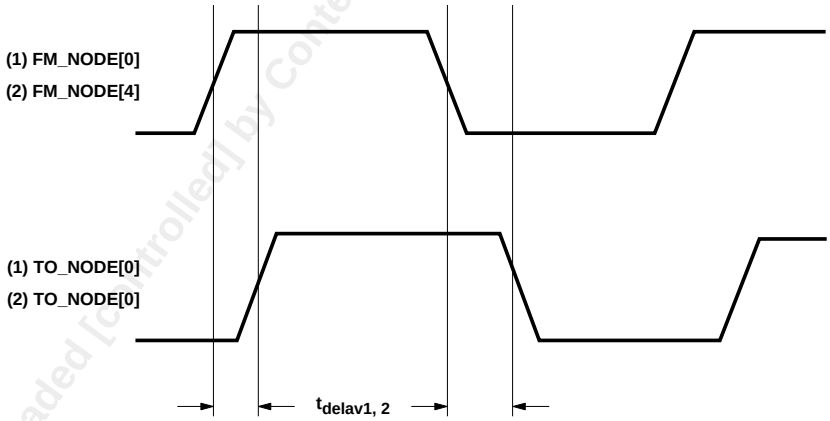


Figure 2. Timing waveforms.

Table 1. Truth Table for CDR at Entry Configuration
FM_LOOP = FM_NODE[0], TO_LOOP = TO_NODE[0], BYPASS[0]– = 1

TO_LOOP	TO_NODE[4]	TO_NODE[3]	TO_NODE[2]	TO_NODE[1]	BYPASS[4]–	BYPASS[3]–	BYPASS[2]–	BYPASS[1]–
FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	0	0	0	0
FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	0	0	0	1
FM_NODE[2]	FM_NODE[2]	FM_NODE[2]	FM_LOOP	FM_LOOP	0	0	1	0
FM_NODE[2]	FM_NODE[2]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	0	0	1	1
FM_NODE[3]	FM_NODE[3]	FM_LOOP	FM_LOOP	FM_LOOP	0	1	0	0
FM_NODE[3]	FM_NODE[3]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	0	1	0	1
FM_NODE[3]	FM_NODE[3]	FM_NODE[2]	FM_LOOP	FM_LOOP	0	1	1	0
FM_NODE[3]	FM_NODE[3]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	0	1	1	1
FM_NODE[4]	FM_LOOP	FM_LOOP	FM_LOOP	FM_LOOP	1	0	0	0
FM_NODE[4]	FM_NODE[1]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	1	0	0	1
FM_NODE[4]	FM_NODE[2]	FM_NODE[2]	FM_LOOP	FM_LOOP	1	0	1	0
FM_NODE[4]	FM_NODE[2]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	1	0	1	1
FM_NODE[4]	FM_NODE[3]	FM_LOOP	FM_LOOP	FM_LOOP	1	1	0	0
FM_NODE[4]	FM_NODE[3]	FM_NODE[1]	FM_NODE[1]	FM_LOOP	1	1	0	1
FM_NODE[4]	FM_NODE[3]	FM_NODE[2]	FM_LOOP	FM_LOOP	1	1	1	0
FM_NODE[4]	FM_NODE[3]	FM_NODE[2]	FM_NODE[1]	FM_LOOP	1	1	1	1

Table 2. Pin Connection Diagram to Achieve Desired CDR Location (See Figures 4, 5)
X Denotes CDR Position with Respect to Hard Disks

Hard Disks	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Connection to PBC Cells	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0
CDR Position (x)	xA	B	C	D	Ax	B	C	D	A	Bx	C	D	A	B	Cx	D	A	B	C	Dx
Cell Connected to Cable	0				4				3				2				1			

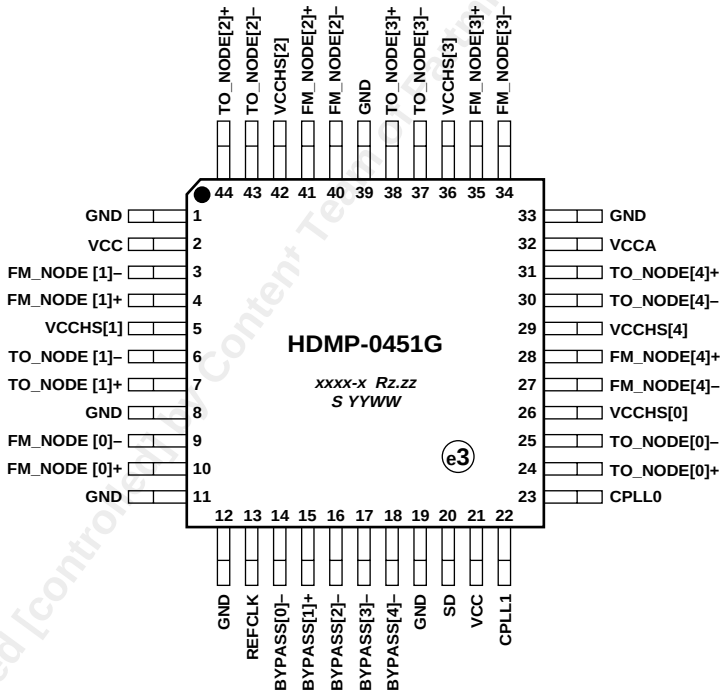


Figure 3. HDMP-0451G package layout and marking, top view.
xxxx-x = wafer lot - build number; Rz.zz = Die Revision; S = Supplier Code; YYWW = Date Code (YY = year, WW = Work Week); COUNTRY = country of manufacture (on back side).

Table 3. Pinout

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+	24	O-PECL	In CDR at entry configuration, this pin is the Serial Output (TO_LOOP+). In other configurations, this pin is wired to the hard disk.
TO_NODE[0]–	25	O-PECL	In CDR at entry configuration, this pin is the Serial Output (TO_LOOP–). In other configurations, this pin is wired to the hard disk.
FM_NODE[4]+	28	I-PECL	Input from Transceiver IC to Cell 4.
FM_NODE[4]–	27	I-PECL	Input from Transceiver IC to Cell 4.
FM_NODE[3]+	35	I-PECL	Input from Transceiver IC to Cell 3.
FM_NODE[3]–	34	I-PECL	Input from Transceiver IC to Cell 3.
FM_NODE[2]+	41	I-PECL	Input from Transceiver IC to Cell 2.
FM_NODE[2]–	40	I-PECL	Input from Transceiver IC to Cell 2.
FM_NODE[1]+	04	I-PECL	Input from Transceiver IC to Cell 1.
FM_NODE[1]–	03	I-PECL	Input from Transceiver IC to Cell 1.
TO_NODE[4]+	31	O-PECL	Output to Transceiver IC from Cell 4.
TO_NODE[4]–	30	O-PECL	Output to Transceiver IC from Cell 4.
TO_NODE[3]+	38	O-PECL	Output to Transceiver IC from Cell 3.
TO_NODE[3]–	37	O-PECL	Output to Transceiver IC from Cell 3.
TO_NODE[2]+	44	O-PECL	Output to Transceiver IC from Cell 2.
TO_NODE[2]–	43	O-PECL	Output to Transceiver IC from Cell 2.
TO_NODE[1]+	07	O-PECL	Output to Transceiver IC from Cell 1.
TO_NODE[1]–	06	O-PECL	Output to Transceiver IC from Cell 1.
FM_NODE[0]+	10	I-PECL	In CDR at entry configuration, this pin is the Serial Input (FM_LOOP+). In other configurations, this pin is wired to the hard disk.
FM_NODE[0]–	09	I-PECL	In CDR at entry configuration, this pin is the Serial Input (FM_LOOP–). In other configurations, this pin is wired to the hard disk.
BYPASS[4]–	18	I-LVTTL	Bypass pin for cell 4. In CDR between Dis k A and Disk B configuration (Table 2) float to HIGH else ground connect through a 1 k Ohm resistor.
BYPASS[3]–	17	I-LVTTL	Bypass pin for cell 3. In CDR between Disk B and Disk C configuration (Table 2) float to HIGH else ground connect through a 1 k Ohm resistor.
BYPASS[2]–	16	I-LVTTL	Bypass pin for cell 2. In CDR between Disk C and Disk D configuration (Table 2) float to HIGH else ground connect through a 1 k Ohm resistor.
BYPASS[1]–	15	I-LVTTL	Bypass pin for cell 1. In CDR at exit configuration, float to HIGH else ground connect through a 1 k Ohm resistor.
BYPASS[0]–	14	I-LVTTL	Bypass pin for cell 0. In CDR at entry configuration, float to HIGH else ground connect through a 1 k Ohm resistor.
REFCLK	13	I-LVTTL	Reference Clock Input for Clock and Data Recovery (CDR) circuit.
CDRCAP1	22	C	PLL cap pin. Connected to pin 23 with a 0.1 microFarad capacitor.
CDRCAP0	23	C	PLL cap pin. Connected to pin 22 with a 0.1 microFarad capacitor.
SD	20	O-LVTTL	Signal Detect via envelope detect method. In CDR at entry case, detects signal on incoming cable. Active High when signal is detected. If FM_NODE[0]± >= 200 mV peak-to-peak, SD = 1. If 200 mV >= FM_NODE[0]± >= 50 mV, SD = unpredictable. If 50 mV >= FM_NODE[0]±, SD = 0.
GND		S	1, 8, 11, 12, 19, 33, 39. Ground pins.
VCCA	32	S	Analog Power Supply pin.
VCCHS	05 42 36 29 26	S S S S S	Cell 1 High Speed Output Pins Power Supply. Cell 2 High Speed Output Pins Power Supply. Cell 3 High Speed Output Pins Power Supply. Cell 4 High Speed Output Pins Power Supply. Cell 0 High Speed Output Pins Power Supply.
VCC		S	2, 21. Logic Power Supply pins.

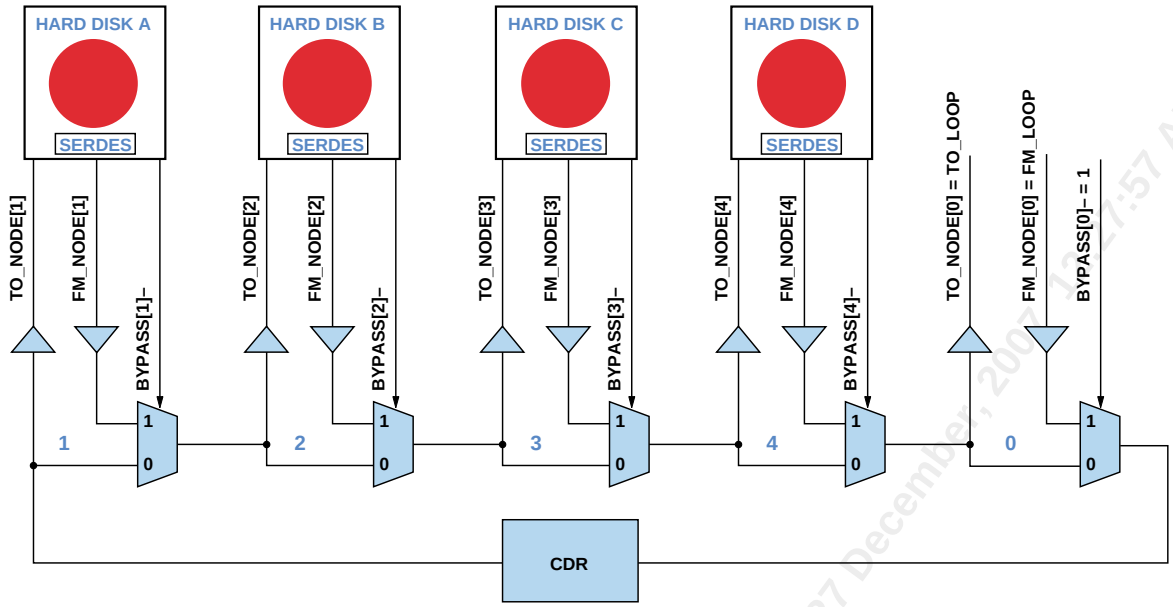


Figure 4. Connection diagram. Case of CDR at first cell.

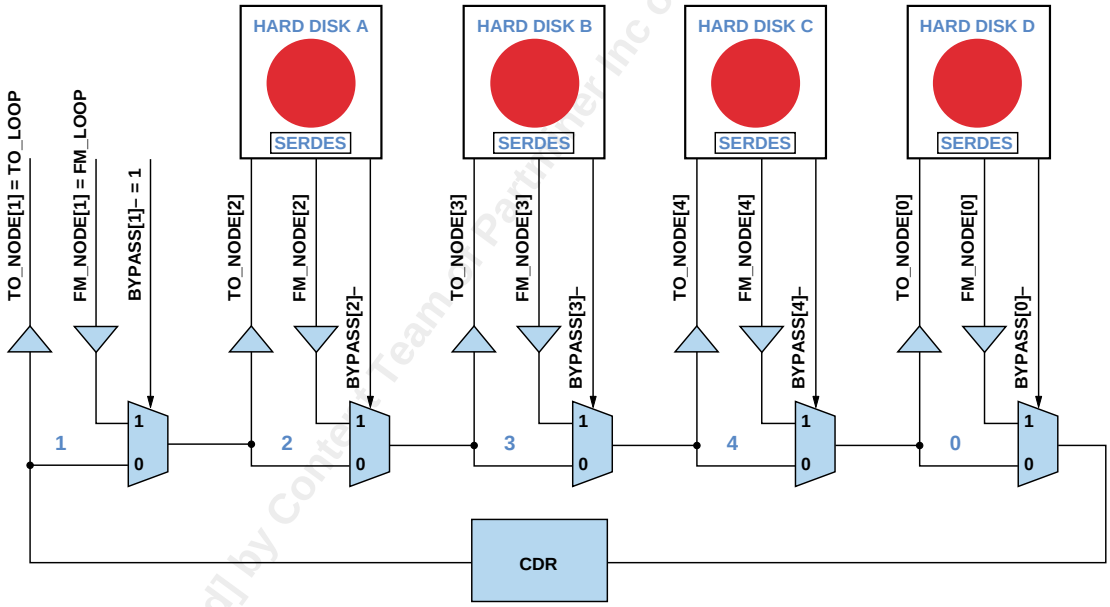


Figure 5. Connection diagram. Case of CDR at last cell.

HDMP-0451G Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.7	4.0
$V_{IN, LVTTL}$	LVTTL Input Voltage	V	–0.7	4.0
V_{IN,HS_IN}	HS_IN Input Voltage	V	2.0	V_{CC}
$I_{O,LVTTL}$	LVTTL Output Current	mA		±13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125

HDMP-0451G Guaranteed Operating Rates

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Serial Clock Rate FC (MBd)		Serial Clock Rate GE (MBd)	
Min.	Max.	Min.	Max.
1,040	1,080	1,240	1,260

HDMP-0451G Clock and Data Recovery Circuit (CDR) Reference Clock Requirements

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.	Min.	Typ.	Max.
f	Nominal Frequency	MHz		106.25			125.00	
F_{tol}	Frequency Tolerance	ppm	–100		+100	–100		+100
Symm	Symmetry (Duty Cycle)	%	40		60	40		60

HDMP-0451G DC Electrical Specifications

T_A =0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	V	2.0		4.0
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	V	0		0.8
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = –400 µA	V	2.2		3.45
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA		.003	40
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA		300	600
I_{CC}	Total Supply Current, T_A = 25°C	mA		210	

HDMP-0451G AC Electrical Specifications
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_{delay1}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	nsec		4.0	
t_{delay2}	Per Cell Latency from FM_NODE[4] to TO_NODE[0]	nsec		2.0	
$t_{r, LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	nsec		2	
$t_{f, LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	nsec		2	
$t_{r, LVTTLout}$	Output LVTTL Rise Time Range, 0.8 V to 2.0 V, 10 pF Load	nsec		1.5	2.4
$t_{f, LVTTLout}$	Output LVTTL Fall Time Range, 2.0 V to 0.8 V, 10 pF Load	nsec		2.0	3.5
t_{rs, HS_OUT}	HS_OUT Single-Ended Rise Time	psec		200	350
t_{fs, HS_OUT}	HS_OUT Single-Ended Fall Time	psec		200	350
t_{rd, HS_OUT}	HS_OUT Differential Rise Time	psec		200	350
t_{fd, HS_OUT}	HS_OUT Differential Fall Time	psec		200	350
V_{IP, HS_IN}	HS_IN Input Peak to Peak Required Differential Voltage Range	mV	200	1200	2000
V_{OP, HS_OUT}	HS_OUT Output Pk-Pk Diff. Voltage Range (Z0 = 75 Ω, Figure 10)	mV	1100	1400	2000

HDMP-0451G Power Dissipation and Thermal Resistance
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Typ.	Max.
PD	Power Dissipation	mW	690	950
Θ_{jc}	Thermal Resistance, Junction to Case	°C/W	7	

HDMP-0451G Output Jitter Characteristics
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Typ.	Max.
RJ	Random Jitter at TO_NODE pins (1 sigma rms)	ps	6	
DJ	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	16	

Please refer to Figures 7 and 8 for jitter measurement setup information.

HDMP-0451G Locking Characteristics
T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parameter	Unit	Max.
Bit Sync Time (Phase Lock)	bits	2500
Frequency Lock at Powerup	µs	500

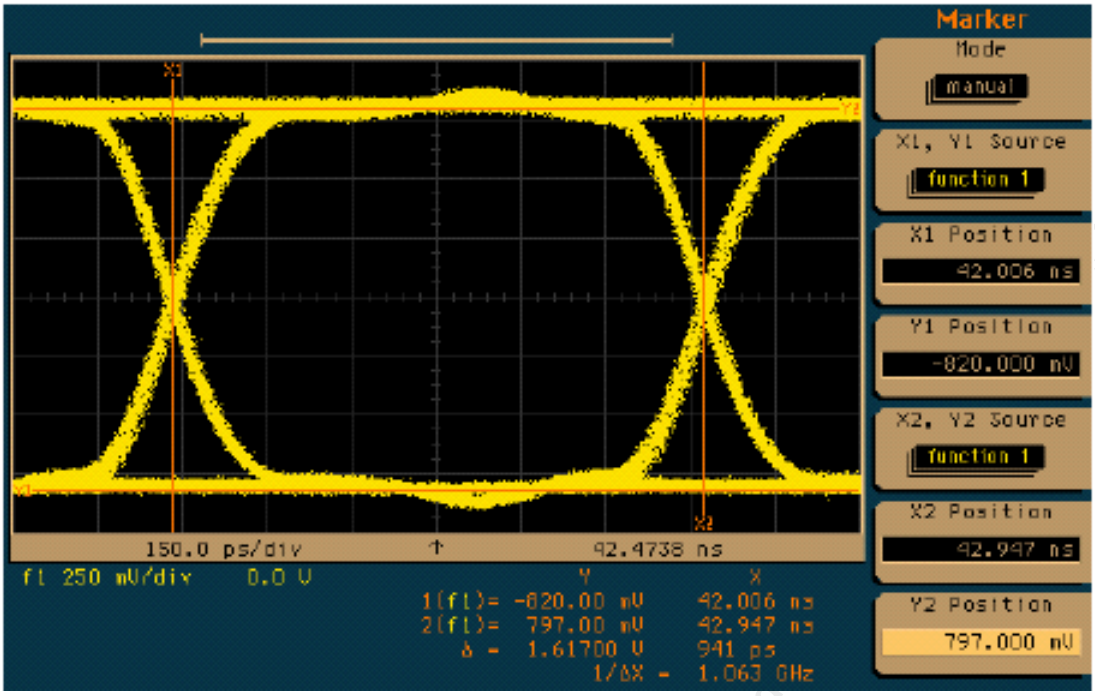


Figure 6. Eye diagram of a high speed differential output.

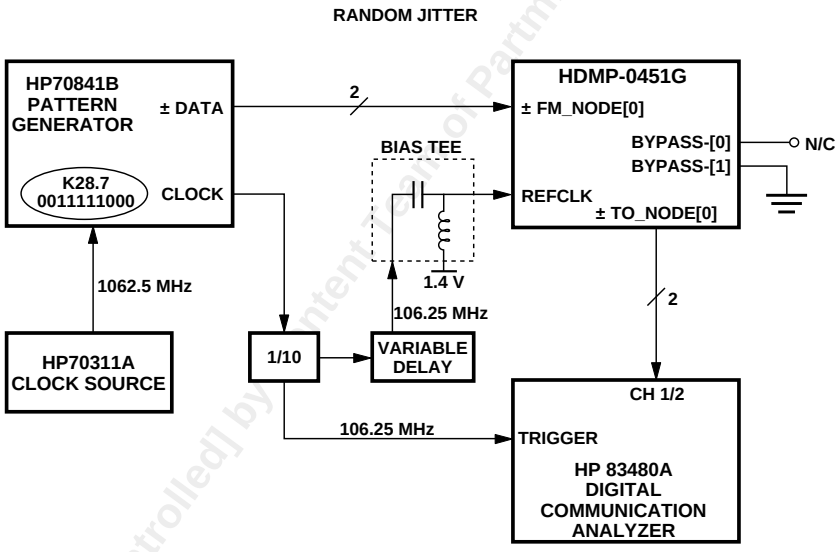


Figure 7. Setup for measurement of random jitter.

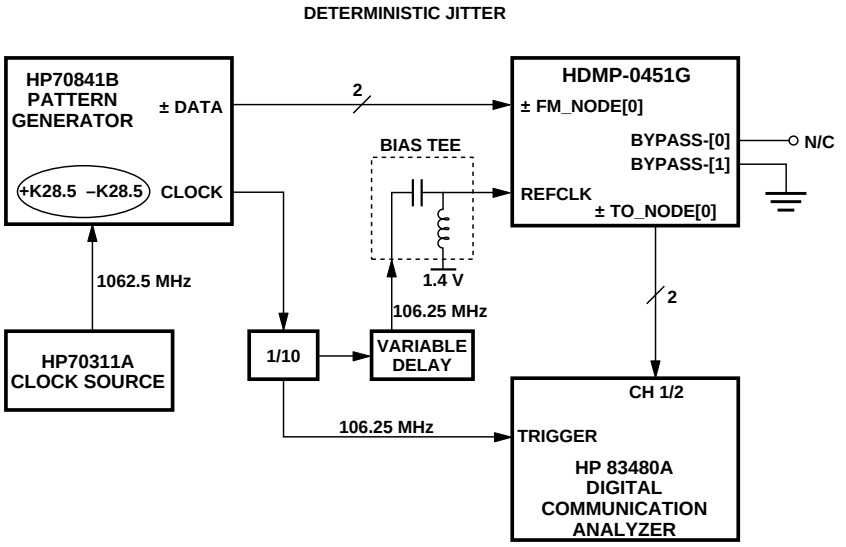


Figure 8. Setup for measurement of deterministic jitter.

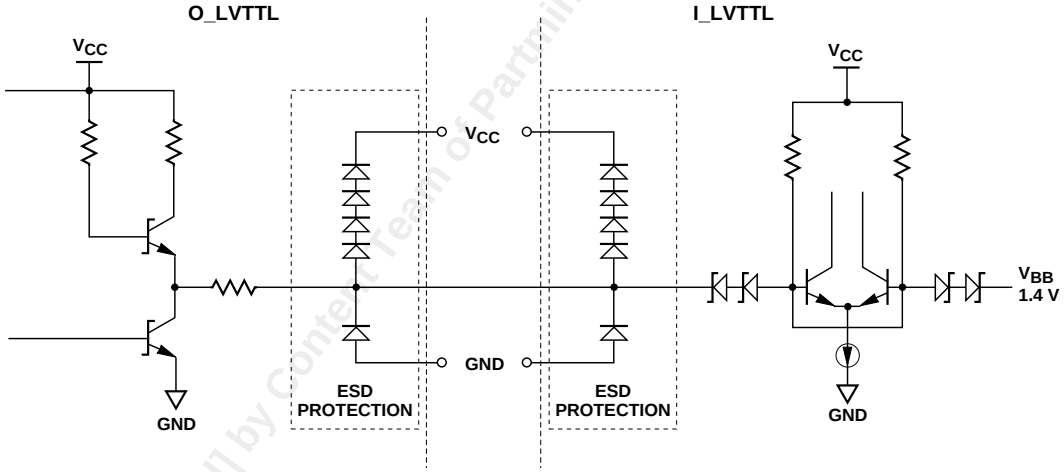
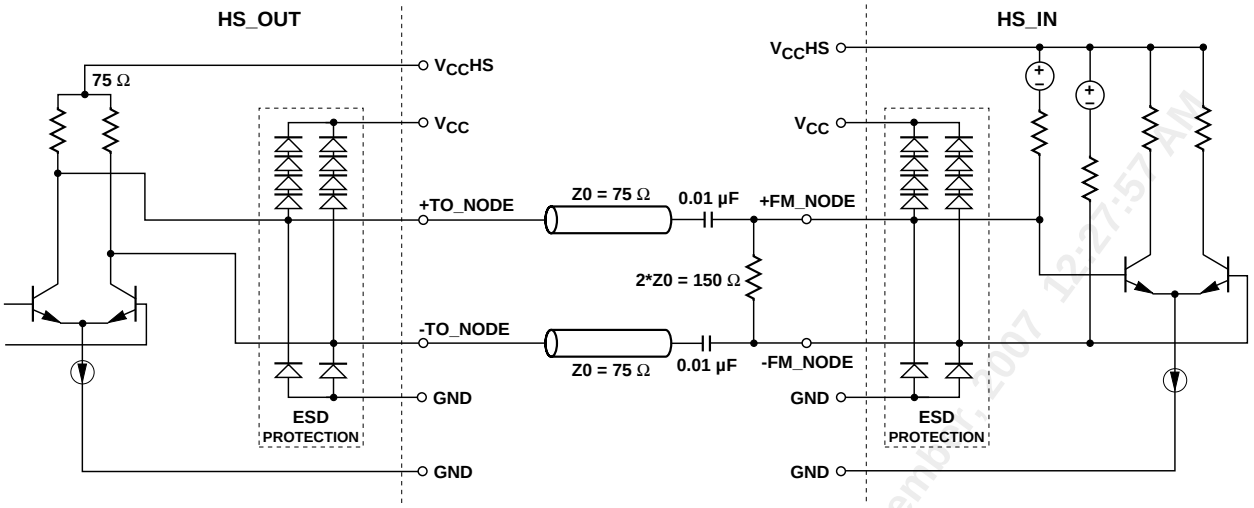


Figure 9. O-LVTTL and I-LVTTL simplified circuit schematic.



NOTE:
1. HS_IN INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.

Figure 10. O-PECL and I-PECL simplified circuit schematic.
Note: HS_IN inputs should never be connected to ground as permanent damage to the device may result.

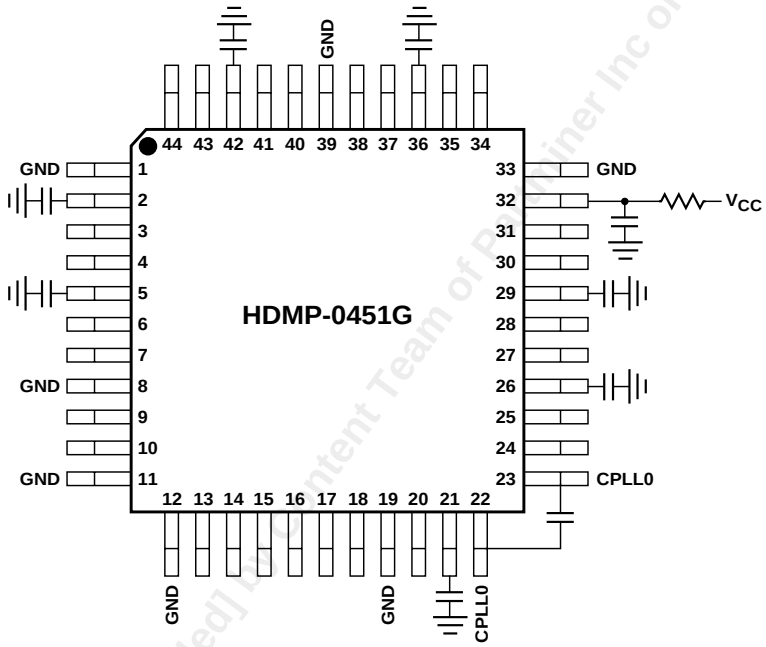


Figure 11. Recommended power supply filtering.
Capacitances = 0.1 microfarads. Resistor = 10 Ohms.

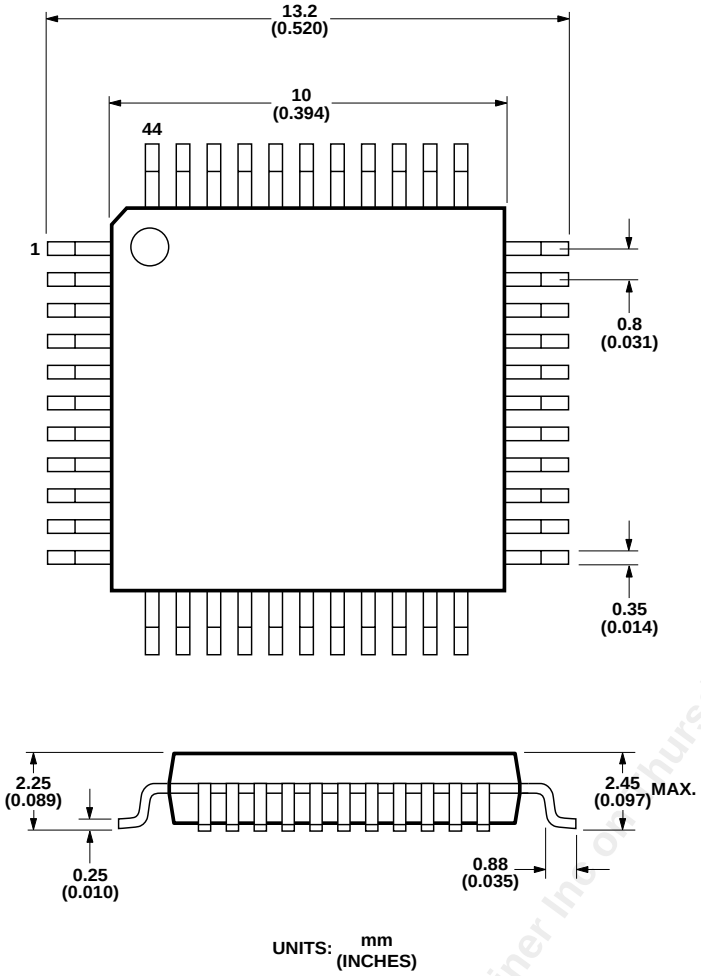


Figure 12. Package drawings.

www.pmc-sierra.com
For product information and a complete list of distributors, please go to our web site.