



# CY54/74FCT374T CY54/74FCT574T

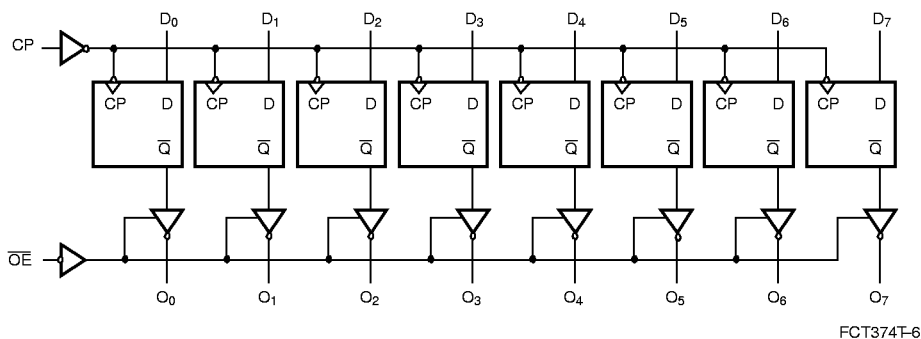
## 8-Bit Registers

### Features

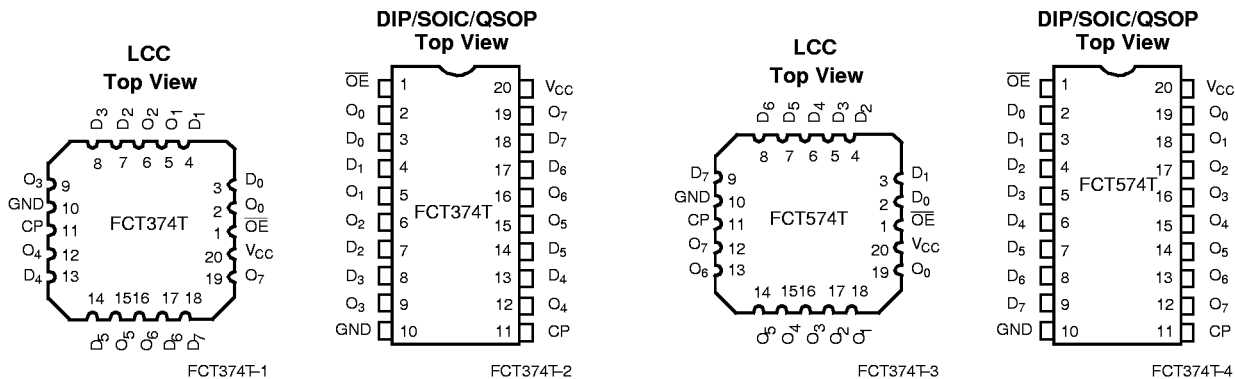
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.2 ns max. (Com'l)  
FCT-A speed at 6.5 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature

- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Sink Current 64 mA (Com'l), 32 mA (Mil)  
Source Current 32 mA (Com'l), 12 mA (Mil)
- Edge-triggered D-type inputs
- 250 MHz typical toggle rate

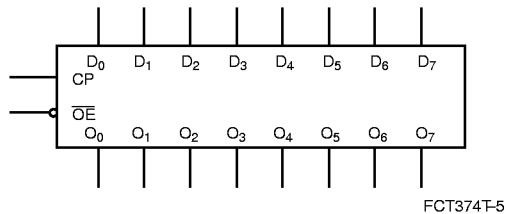
### Logic Block Diagram



### Pin Configurations



### Logic Symbol





## Functional Description

The FCT374T and FCT574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have three-state outputs for bus oriented applications. A buffered clock (CP) and output enable ( $\overline{OE}$ ) are common to all flip-flops. The FCT574T is identical to FCT374T except for flow-through pinout to simplify board design. The eight flip-flops contained in the FCT374T and FCT574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When  $\overline{OE}$  is LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs will be in the high-impedance state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

## Function Table<sup>[1]</sup>

Inputs			Outputs
D	CP	OE	O
H	┐	L	H
L	┐	L	L
X	X	H	Z

## Maximum Ratings<sup>[2, 3]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-65°C to +135°C
Supply Voltage to Ground Potential .....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage .....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....	120 mA
Power Dissipation.....	0.5W
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)

## Operating Range

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	Com'l	2.0		V	
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3	V	
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =32 mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	
V <sub>IL</sub>	Input LOW Voltage				0.8	V	
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs		0.2		V	
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V	
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>			5	μA	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V			±1	μA	
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V			±1	μA	
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.7V			10	μA	
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V			-10	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V	-60	-120	-225	mA	
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V			±1	μA	

### Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level X = Don't Care Z = HIGH Impedance = LOW-to-HIGH clock transition
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.



**Capacitance<sup>[2]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.1	0.2	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V, <sup>[8]</sup> f <sub>1</sub> =0, Outputs Open	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.06	0.12	mA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, OE=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.7	1.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, OE=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.2	3.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, OE=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	1.6	3.2 <sup>[11]</sup>	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, OE=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	3.9	12.2 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>1</sub>)  
I<sub>CC</sub> = Quiescent Current with CMOS input levels  
ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
D<sub>H</sub> = Duty Cycle for TTL inputs HIGH  
N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
f<sub>1</sub> = Input signal frequency  
N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>  
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I<sub>C</sub> formula. These limits are guaranteed but not tested.



Switching Characteristics<sup>[12]</sup> Over the Operating Range

Parameter	Description	FCT374T/FCT574T				FCT374AT/FCT574AT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t <sub>W</sub>	Clock Pulse Width <sup>[14]</sup> HIGH or LOW	7.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT374CT/FCT574CT				FCT374DT/ FCT574DT		Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output	2.0	6.2	2.0	5.2	2.0	4.2	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	6.2	1.5	5.5	1.5	4.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.7	1.5	5.0	1.5	4.0	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		ns	4
t <sub>W</sub>	Clock Pulse Width <sup>[14]</sup> HIGH or LOW	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.
14. With one data channel toggling, t<sub>W(L)</sub>=t<sub>W(H)</sub>=4.0 ns and t<sub>r</sub>=t<sub>f</sub>=1.0 ns.



**Ordering Information—FCT374T**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT374CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT374ATLMB	L61	20-Pin Square Leadless Chip Carrier	Military
10.0	CY74FCT374TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374TLMB	L61	20-Pin Square Leadless Chip Carrier-	

**Ordering Information—FCT574T**

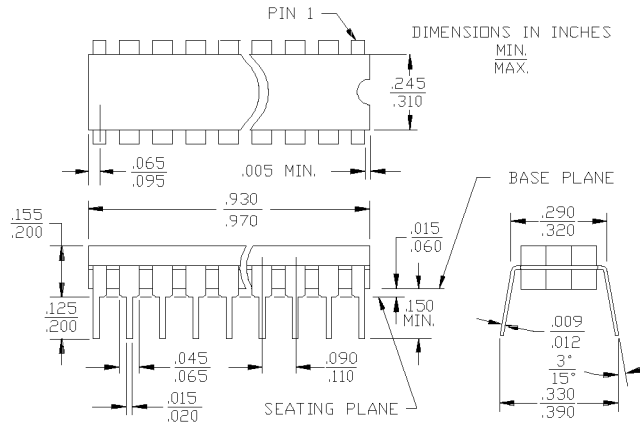
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT574CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
6.5	CY74FCT574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT574ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
10.0	CY74FCT574TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT574TDMB	D6	20-Lead (300-Mil) CerDIP	Military

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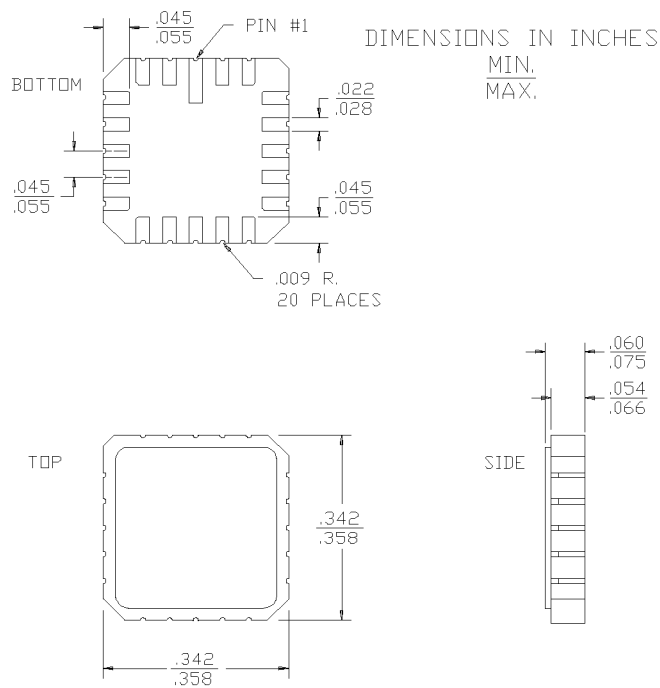
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**Package Diagrams**

**20-Lead (300-Mil) CerDIP D6**  
 MIL-STD-1835 D-8Config.A



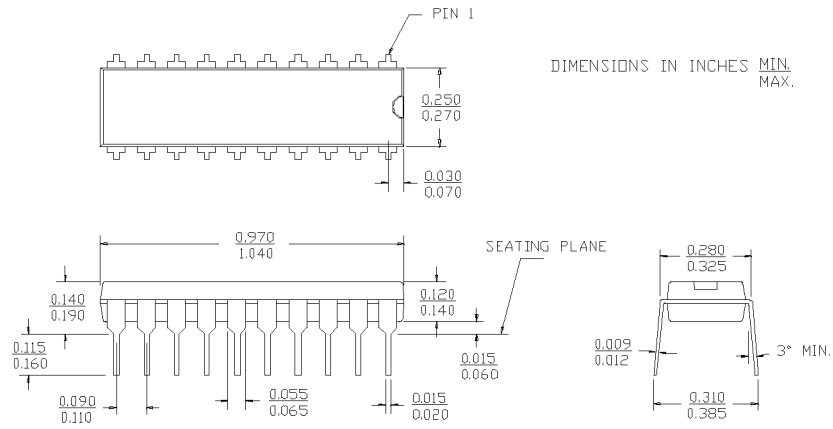
**20-Pin Square Leadless Chip Carrier L61**  
 MIL-STD-1835 C-2A



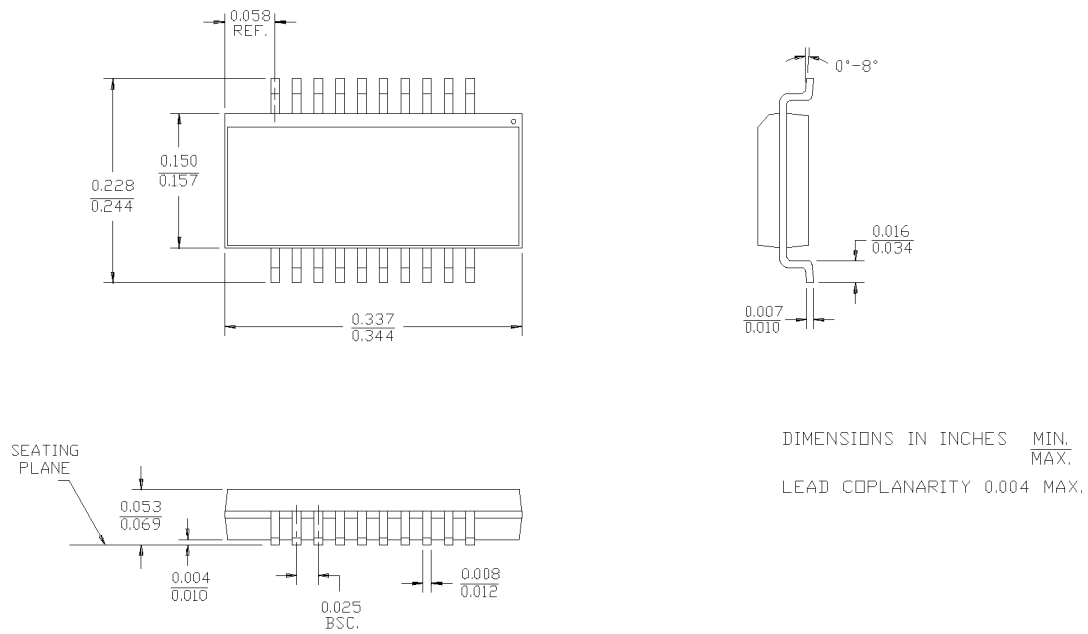


**Package Diagrams (continued)**

**20-Lead (300-Mil) Molded DIP P5**



**20-Lead Quarter Size Outline Q5**





**Package Diagrams (continued)**

**20-Lead (300-Mil) Molded SOIC S5**

