

# MM74C175 Quad D-Type Flip-Flop

## General Description

The MM74C175 consists of four positive-edge triggered D-type flip-flops implemented with monolithic CMOS technology. Both true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D-type inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

All inputs are protected from static discharge by diode clamps to  $V_{CC}$  and GND.

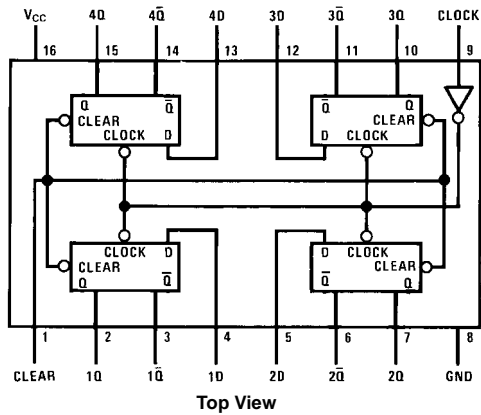
## Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45  $V_{CC}$  (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L

## Ordering Code:

| Order Number | Package Number | Package Description  |
|--------------|----------------|--|
| MM74C175N    | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

## Connection Diagram



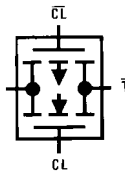
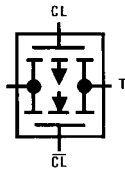
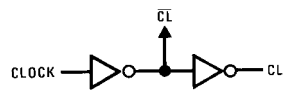
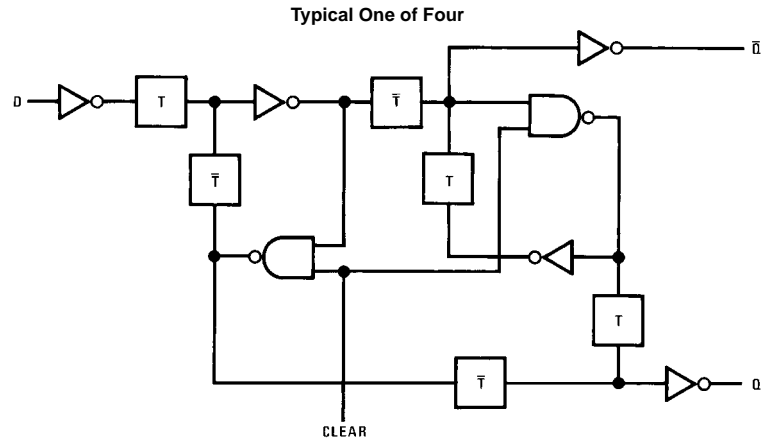
## Truth Table

Each Flip-Flop

| Inputs |       |   | Outputs |           |
|--------|-------|---|---------|-----------|
| Clear  | Clock | D | Q       | $\bar{Q}$ |
| L      | X     | X | L       | H         |
| H      | ↑     | H | H       | L         |
| H      | ↑     | L | L       | H         |
| H      | H     | X | NC      | NC        |
| H      | L     | X | NC      | NC        |

H = HIGH Level  
L = LOW Level  
X = Irrelevant  
↑ = Transition from LOW-to-HIGH level  
NC = No Change

Block Diagrams



**Absolute Maximum Ratings**(Note 1)

|                             |                          |
|-----------------------------|--------------------------|
| Voltage at Any Pin          | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range | -55°C to +125°C          |
| Storage Temperature Range   | -65°C to +150°C          |
| Power Dissipation ( $P_D$ ) |                          |
| Dual-In-Line                | 700 mW                   |
| Small Outline               | 500 mW                   |
| Operating $V_{CC}$ Range    | 3V to 15V                |
| Absolute Maximum $V_{CC}$   | 18V                      |
| Lead Temperature            |                          |
| (Soldering, 10 seconds)     | 260°C                    |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

**DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise specified

| Symbol  | Parameter                            | Conditions  | Min            | Typ    | Max        | Units   |
|---|--------------------------------------|---|----------------|--------|------------|---------|
| <b>CMOS TO CMOS</b>   |                                      |   |                |        |            |         |
| $V_{IN(1)}$   | Logical "1" Input Voltage            | $V_{CC} = 5V$<br>$V_{CC} = 10V$                                   | 3.5<br>8.0     |        |            | V       |
| $V_{IN(0)}$   | Logical "0" Input Voltage            | $V_{CC} = 5V$<br>$V_{CC} = 10V$                                   |                |        | 1.5<br>2.0 | V       |
| $V_{OUT(1)}$  | Logical "1" Output Voltage           | $V_{CC} = 5V, I_O = -10 \mu A$<br>$V_{CC} = 10V, I_O = -10 \mu A$ | 4.5<br>9.0     |        |            | V       |
| $V_{OUT(0)}$  | Logical "0" Output Voltage           | $V_{CC} = 5V, I_O = 10 \mu A$<br>$V_{CC} = 10V, I_O = 10 \mu A$   |                |        | 0.5<br>1.0 | V       |
| $I_{IN(1)}$   | Logical "1" Input Current            | $V_{CC} = 15V, V_{IN} = 15V$                                      |                | 0.005  | 1.0        | $\mu A$ |
| $I_{IN(0)}$   | Logical "0" Input Current            | $V_{CC} = 15V, V_{IN} = 0V$                                       | -1.0           | -0.005 |            | $\mu A$ |
| $I_{CC}$  | Supply Current                       | $V_{CC} = 15V$  |                | 0.05   | 300        | $\mu A$ |
| <b>CMOS/LPTTL INTERFACE</b>   |                                      |   |                |        |            |         |
| $V_{IN(1)}$   | Logical "1" Input Voltage            | 74C, $V_{CC} = 4.75V$   | $V_{CC} - 1.5$ |        |            | V       |
| $V_{IN(0)}$   | Logical "0" Input Voltage            | 74C, $V_{CC} = 4.75V$   |                |        | 0.8        | V       |
| $V_{OUT(1)}$  | Logical "1" Output Voltage           | 74C, $V_{CC} = 4.75V, I_O = -360 \mu A$                           | 2.4            |        |            | V       |
| $V_{OUT(0)}$  | Logical "0" Output Voltage           | 74C, $V_{CC} = 4.75V, I_O = 360 \mu A$                            |                |        | 0.4        | V       |
| <b>OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)</b> |                                      |   |                |        |            |         |
| $I_{SOURCE}$  | Output Source Current<br>(P-Channel) | $V_{CC} = 5V, T_A = 25^\circ C,$<br>$V_{OUT} = 0V$                | -1.75          | -3.3   |            | mA      |
| $I_{SOURCE}$  | Output Source Current<br>(P-Channel) | $V_{CC} = 10V, T_A = 25^\circ C,$<br>$V_{OUT} = 0V$               | -8.0           | -15    |            | mA      |
| $I_{SINK}$  | Output Sink Current<br>(N-Channel)   | $V_{CC} = 5V, T_A = 25^\circ C,$<br>$V_{OUT} = V_{CC}$            | 1.75           | 3.6    |            | mA      |
| $I_{SINK}$  | Output Sink Current<br>(N-Channel)   | $V_{CC} = 10V, T_A = 25^\circ C,$<br>$V_{OUT} = V_{CC}$           | 8.0            | 16     |            | mA      |

## AC Electrical Characteristics (Note 2)

$T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise noted

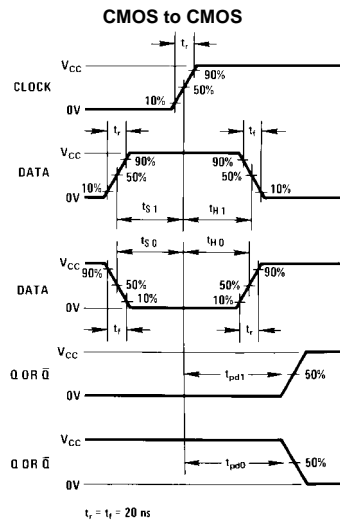
| Symbol    | Parameter   | Conditions                              | Min        | Typ        | Max        | Units         |
|-----------|---|---|------------|------------|------------|---------------|
| $t_{pd}$  | Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\bar{Q}$ | $V_{CC} = 5V$<br>$V_{CC} = 10V$         |            | 190<br>75  | 300<br>110 | ns            |
| $t_{pd}$  | Propagation Delay Time to a Logical "0" from Clear to Q                             | $V_{CC} = 5V$<br>$V_{CC} = 10V$         |            | 180<br>70  | 300<br>110 | ns            |
| $t_{pd}$  | Propagation Delay Time to a Logical "1" from Clear to Q                             | $V_{CC} = 5V$<br>$V_{CC} = 10V$         |            | 230<br>90  | 400<br>150 | ns            |
| $t_S$     | Time Prior to Clock Pulse that Data Must be Present                                 | $V_{CC} = 5V$<br>$V_{CC} = 10V$         | 100<br>40  | 45<br>16   |            | ns            |
| $t_H$     | Time After Clock Pulse that Data Must be Held                                       | $V_{CC} = 5V$<br>$V_{CC} = 10V$         | 0<br>0     | -11<br>-4  |            | ns            |
| $t_W$     | Minimum Clock Pulse Width   | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$       |            | 130<br>45  | 250<br>100 | ns            |
| $t_W$     | Minimum Clear Pulse Width   | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$       |            | 120<br>45  | 250<br>100 | ns            |
| $t_r$     | Maximum Clock Rise Time   | $V_{CC} = 5V$<br>$V_{CC} = 10V$         | 15<br>5.0  | 450<br>125 |            | $\mu\text{s}$ |
| $t_f$     | Maximum Clock Fall Time   | $V_{CC} = 5V$<br>$V_{CC} = 10V$         | 15<br>5.0  | 50<br>50   |            | $\mu\text{s}$ |
| $f_{MAX}$ | Maximum Clock Frequency   | $V_{CC} = 5V$<br>$V_{CC} = 10V$         | 2.0<br>5.0 | 3.5<br>10  |            | MHz           |
| $C_{IN}$  | Input Capacitance   | Clear Input (Note 3)<br>Any Other Input |            | 10<br>5.0  |            | pF            |
| $C_{PD}$  | Power Dissipation Capacitance   | Per Package (Note 4)                    |            | 130        |            | pF            |

**Note 2:** AC Parameters are guaranteed by DC correlated testing.

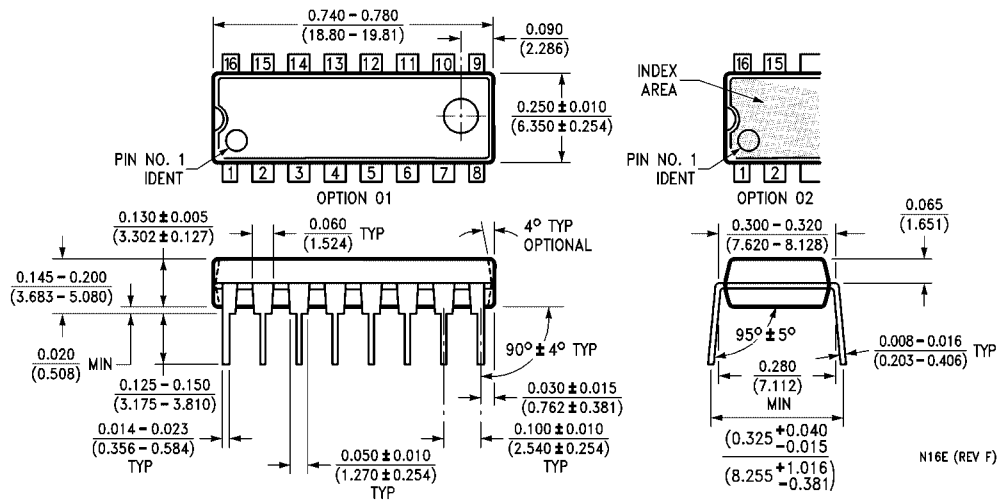
**Note 3:** Capacitance is guaranteed by periodic testing.

**Note 4:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note AN-90.

## Switching Time Waveforms



**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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