Rochester Electronics

Datasheet

PART NUMBER

N82C501AD-ROC

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

82C501AD
ETHERNET SERIAL INTERFACE

- **CHMOS Replacement for Intel 82C501, 82501, or SEEQ 8023A**
- **Conforms to IEEE 802.3 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) Specifications**
- **Direct Interface to Intel LAN Controllers and the Attachment Unit Interface (Transceiver) Cable**
- **10-Mb/s Operation**
- **Manchester Encoding/Decoding and Receive Clock Recovery**
- **10-MHz Transmit Clock Generator**
- **Drives/Receives 802.3 AUI Cables**
- **Defeatable Watchdog Timer Circuit to Prevent Continuous Transmission**
- **Diagnostic Loopback for Network Node Fault Detection and Isolation**

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The 82C501AD Ethernet Serial Interface (ESI) chip is designed to work directly with Intel LAN Controllers (82586, 82590, and 82596) in IEEE 802.3 (10BASE5 and 10BASE2), 10-Mb/s, Local Area Network applications. The major functions of the 82C501AD are to generate the 10-MHz transmit clock for the Intel LAN Controller, perform Manchester encoding/decoding of the transmitted/received frames, and provide the electrical interface to the Ethernet transceiver cable (AUI). Diagnostic loopback control enables the 82C501AD to route the signal to be transmitted from the Intel LAN Controller through its Manchester encoding and decoding circuitry and back to the Intel LAN Controller. The combined loopback capabilities of the Intel LAN Controller and 82C501AD result in highly effective fault detection and isolation through sequential testing of the communications interface. A (defeatable) on-chip watchdog timer circuit prevents the station from locking up in a continuous transmit mode. The 82C501AD is pin compatible with the 82C501 and functionally compatible with the 82501 and SEEQ 8023A.

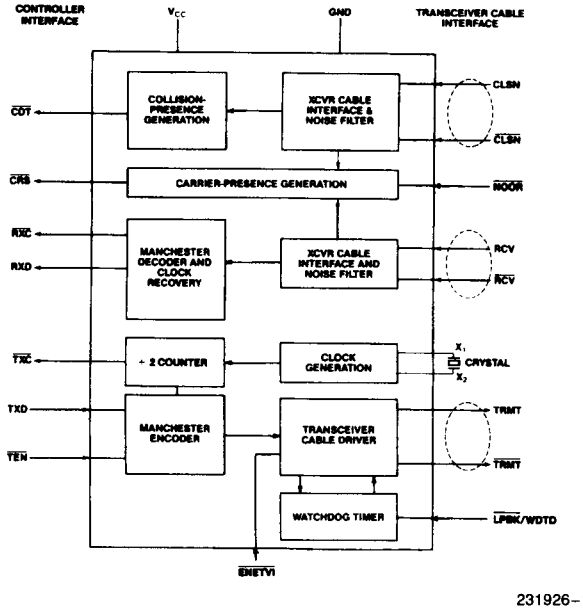

Figure 1. 82C501AD Functional Block Diagram

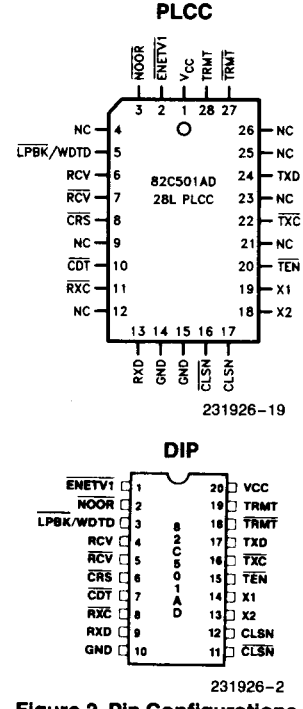

Figure 2. Pin Configurations (PLCC and DIP)

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Table 1. Pin Description

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
$\overline{\text{ENETV1}}$	1	2	I	**ETHERNET VERSION 1.0:** An active low, MOS-level input intended for use as a strapping option. When $\overline{\text{ENETV1}}$ is asserted, the TRMT/$\overline{\text{TRMT}}$ pair remains at high differential voltage at the end of transmission. This operation is compatible with the Ethernet Version 1.0 specification. If the $\overline{\text{ENETV1}}$ pin is left floating, an internal pull-up resistor biases the input inactive high. When $\overline{\text{ENETV1}}$ is high, the TRMT/$\overline{\text{TRMT}}$ differential voltage gradually approaches 0V at the end of transmission.
$\overline{\text{NOOR}}$	2	3	I	**CRS 'OR':** An active low, MOS-level input intended for use as a strapping option. When $\overline{\text{NOOR}}$ is low, only the presence of a valid signal on the RCV/$\overline{\text{RCV}}$ pair will force $\overline{\text{CRS}}$ active. If the $\overline{\text{NOOR}}$ pin is floating, an internal pull-up resistor biases the input inactive high. When $\overline{\text{NOOR}}$ is inactive high, either the presence of a valid signal on CLSN/$\overline{\text{CLSN}}$ or on RCV/$\overline{\text{RCV}}$ will force $\overline{\text{CRS}}$ active.
$\overline{\text{LPBK}}$/ WDTD	3	5	I	**LOOPBACK/WATCHDOG TIMER DISABLE:** An active low, TTL-level control signal that enables the loopback mode. In loopback mode serial data on the TXD input is routed through the 82C501AD internal circuits and back to the RXD output without driving the TRMT/$\overline{\text{TRMT}}$ output pair to the transceiver cable. During loopback $\overline{\text{CDT}}$ is asserted at the end of each transmission to simulate the SQE test. The $\overline{\text{LPBK}}$ signal should be driven high once V_{CC} is stabilized. **WATCHDOG TIMER DISABLE:** An input voltage of 10 to 16 V through a 1 kΩ resistor will disable the on-chip watchdog timer.
RCV $\overline{\text{RCV}}$	4 5	6 7	I I	**RECEIVE PAIR:** A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV is negative-going to indicate the beginning of a frame. The last transition is positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.
$\overline{\text{CRS}}$	6	8	O	**CARRIER SENSE:** An active low, MOS-level output which notifies the Intel LAN Controller that there is activity on the coaxial cable. The signal is asserted when a valid signal on RCV/$\overline{\text{RCV}}$ is present. If the $\overline{\text{NOOR}}$ input is inactive high, then $\overline{\text{CRS}}$ is also asserted when a valid signal on CLSN/$\overline{\text{CLSN}}$ is present. It is deasserted at the end of a frame or when the end of the collision-presence signal is detected, synchronous to $\overline{\text{RXC}}$. After transmission, when $\overline{\text{NOOR}}$ = 1, $\overline{\text{CRS}}$ is inhibited for a period of 5 μs minimum to 7 μs maximum, regardless of any activity on the collision-presence signal (CLSN/$\overline{\text{CLSN}}$) and RCV/$\overline{\text{RCV}}$ inputs. When $\overline{\text{NOOR}}$ = 0, $\overline{\text{CRS}}$ is not inhibited.
$\overline{\text{CDT}}$	7	10	O	**COLLISION DETECT:** An active-low, MOS-level signal which drives the $\overline{\text{CDT}}$ input of the Intel LAN Controller. It is asserted as long as there is activity on the collision pair (CLSN/$\overline{\text{CLSN}}$), and during SQE (heartbeat) test in loopback.
$\overline{\text{RXC}}$	8	11	O	**RECEIVE CLOCK:** A 10-MHz MOS level clock output with 5-ns rise and fall times. This output is connected to the Intel LAN Controller receive clock input $\overline{\text{RXC}}$. There is a maximum 1.4-μs delay at the beginning of a frame reception before the clock recovery circuit gains lock. During idle (no incoming frames) $\overline{\text{RXC}}$ is forced low.
RXD	9	13	O	**RECEIVE DATA:** A MOS-level output tied directly to the RXD input of the Intel LAN Controller and sampled by the Intel LAN Controller at the negative edge of $\overline{\text{RXC}}$. The bit stream received from the transceiver cable is Manchester decoded prior to being transferred to the controller. This output remains high during idle.

Table 1. Pin Description (Continued)

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
GND	10	14 15		**GROUND**
CLSN $\overline{CLSN}$	12 11	17 16	I I	**COLLISION PAIR:** A differentially driven input pair tied to the collision-presence pair of the Ethernet transceiver cable. The collision-presence signal is a 10-MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going.
X_1 X_2	14 13	19 18	I I	**CLOCK CRYSTAL:** 20-MHz crystal inputs. When X_2 is floated, X_1 can be driven by an external MOS level input clock.
$\overline{TEN}$	15	20	I	**TRANSMIT ENABLE:** An active low, TTL level signal synchronous to $\overline{TXC}$ that enables data transmission to the transceiver cable and starts the watchdog timer. $\overline{TEN}$ can be driven by the $\overline{RTS}$ signal from the Intel LAN Controller.
$\overline{TXC}$	16	22	O	**TRANSMIT CLOCK:** A 10-MHz MOS level clock output with 5-ns rise and fall times. This clock is connected directly to the $\overline{TXC}$ input of the Intel LAN Controller.
TXD	17	24	I	**TRANSMIT DATA:** A TTL-level input signal that is directly connected to the serial data output, TXD, of the Intel LAN Controller.
TRMT $\overline{TRMT}$	19 18	28 27	O O	**TRANSMIT PAIR:** A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transmission, which is always positive at TRMT, the differential voltage is slowly reduced to zero volts in a series of steps. If $\overline{ENETV1}$ is asserted this voltage stepping is disabled.
V_{CC}	20	1		**POWER:** 5V ±10%.

FUNCTIONAL DESCRIPTION

Clock Generation

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ± 0.01% clock required by the IEEE 802.3 specification.

It is recommended that a crystal meeting the following specifications be used:

- Quartz Crystal
- 20.00 MHz ± 0.002% at 25°C
- Accuracy ±0.005% Over Full Operating Temperature, 0 to 70°C
- Parallel Resonant with 20-pF Load Fundamental Mode

Several vendors have these crystals available; either off the shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc
   Yankton, SD 57078
2. Crystek Corporation
   100 Crystal Drive
   Ft Myers, FL 33907

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advised to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 and 35 pF.

An external, 20 MHz, MOS-level clock may be applied to pin X_1 while pin X_2 is left floating.

TRANSMIT SECTION

Manchester Encoder and Transceiver Cable Driver

The 20-MHz clock is used to Manchester encode data on the TXD input line. The clock is also divided by two to produce the 10-MHz clock required by the

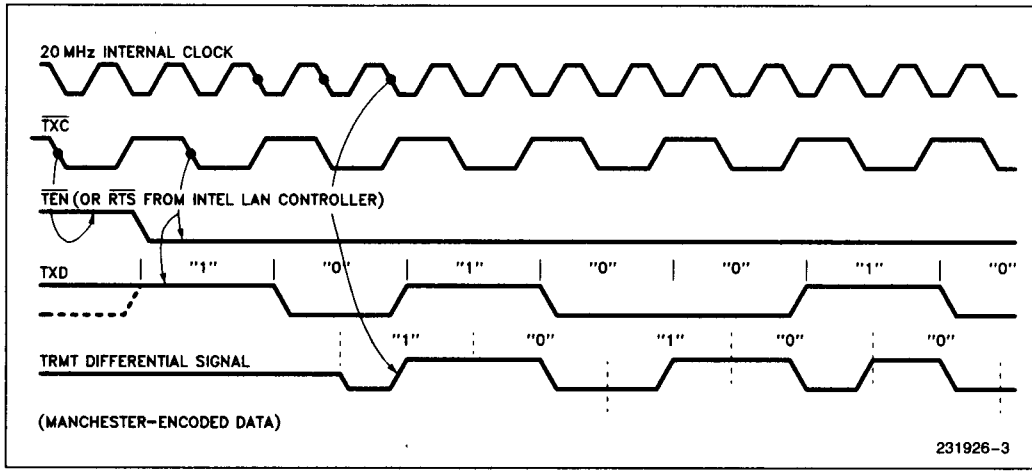

Figure 3. Start of Transmission and Manchester Encoding

Intel LAN Controller for synchronizing its $\overline{RTS}$ and TXD signals. See Figure 3. (Note that the Intel LAN Controller $\overline{RTS}$ is tied to the 82C501AD $\overline{TEN}$ input as shown in Figure 4.)

Data encoding and transmission begins with $\overline{TEN}$ going low. Since the first bit is a '1', the first transition on the transmit output TRMT is always negative. Transmission ends with the $\overline{TEN}$ going high. The last transition is always positive at TRMT and can occur at the center of the bit cell (last bit = 1) or at the boundary of the bit cell (last bit = 0). A 1.5-bit delay is introduced by the 82C501AD between its TXD input and TRMT/$\overline{TRMT}$ output as shown in Figure 3. If the signal applied to the $\overline{ENETV1}$ input is inactive high, the TRMT differential output is kept at high differential for 200 ns, after the last transmit data transition, then it is gradually reduced. The TRMT/$\overline{TRMT}$ differential voltage will become less than 40 mV within t_{18} after the last positive transition. The undershoot for return to idle is less than 100 mV differentially. This mode of operation is compatible with the IEEE 802.3 transceiver specifications.

If an active signal is present at the $\overline{ENETV1}$ input at the end of transmission, the TRMT/$\overline{TRMT}$ pair output will remain at a high differential voltage. As a result there is a positive differential voltage during the entire transmit idle time. This mode of operation is compatible with the Ethernet Version 1.0 specification.

Immediately after the end of a transmission all signals on the receive pair are inhibited for 5 μs minimum to 7 μs maximum (when $\overline{NOOR}$ = 1). This dead time is required for proper operation of the SQE (heartbeat) test.

An internal watchdog timer is started when $\overline{TEN}$ is asserted low at the beginning of the frame. The duration of the watchdog timer is 25 ms ± 15%. If the transmission terminates (by deasserting the $\overline{TEN}$) before the timer expires, the timer is reset (and ready for the next transmission). If the timer expires before the transmission ends, the frame is aborted. The frame is aborted by disabling the output driver for the TRMT/$\overline{TRMT}$ pair. RXD and $\overline{RXC}$ are not affected. The watchdog timer is reset only when the $\overline{TEN}$ is deasserted.

The cable driver is a differential circuit requiring external pulldown resistors of 240Ω ±5%. In addition, high-voltage protection to +10V maximum, and short circuit protection to ground is provided.

To provide additional high voltage protection if the cable is shorted, an isolation transformer can be used to isolate the TRMT and $\overline{\text{TRMT}}$ outputs from the transceiver cable. Transmit circuit inductance (including the IEEE 802.3 transceiver transformers) should be a minimum of 27 μH. We recommend that the transformer at the 82C501AD end have a minimum inductance of 75 μH.

RECEIVE SECTION

Cable Interface

The 82C501AD input circuits can be driven directly from the Ethernet transceiver cable receive pair. In this case the cable is terminated with a resistor of 78Ω ±6% for proper impedance matching. See Figure 4.

The signal received on the RCV/$\overline{\text{RCV}}$ pair from the transceiver defines both the $\overline{\text{RXC}}$ and RXD outputs to the Intel LAN Controller. The $\overline{\text{RXC}}$ and RXD signals are recovered from the encoded RCV/$\overline{\text{RCV}}$ pair signal by the Manchester decode circuitry.

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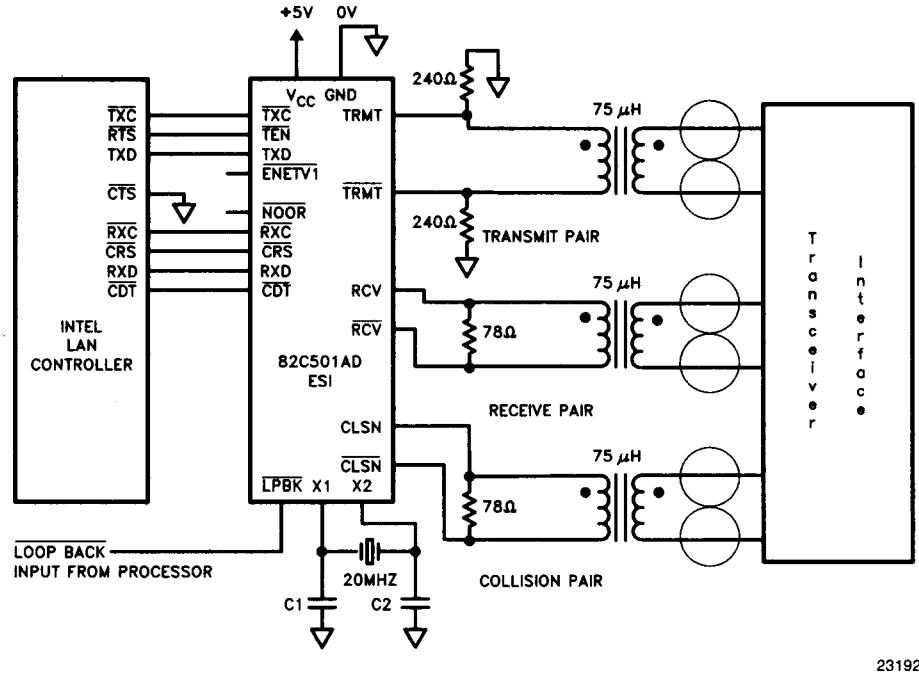


NOTE:
$C_1 = C_2 = 22$ pF to 35 pF.
For best operation, a decoupling capacitor should be used between V_{CC} and GND.

Figure 4. LAN Controller/82C501AD/Transceiver Interface

The input circuits can also be driven with ECL voltage levels. In either case, the input common mode voltage must be in the range of 0-V_{CC} volts to allow for wide driver supply variation at the transceiver. To provide additional high voltage protection, if the cable is shorted, an isolation transformer can be used to isolate the RCV and $\overline{RCV}$ inputs from the cable.

Manchester Decoder and Clock Recovery

The Manchester-encoded data stream is decoded to separate the Receive Clock ($\overline{RXC}$) and the Receive Data ($\overline{RXD}$) from the stream. The 82C501AD uses an advanced digital technique to perform the decoding function. The use of digital circuitry instead of analog circuitry (e.g., a phase-lock loop) to perform the decoding ensures that the decoding function is less sensitive to variations in operating conditions.

A simplified diagram of the decoder appears in Figure 5. A high-resolution phase reference is used to digitize the phase of the incoming data bit-center transition. The digitizer has a phase resolution of 1/32 bit time.

The digitized phase is filtered by a digital low-pass filter to remove rapid phase variations; i.e., phase jitter. Slow phase variations, such as those caused by small differences between the data frequency and the clock frequency, are passed unfiltered by the low-pass filter.

The $\overline{RXC}$ generator digitally sets the phases of the two $\overline{RXC}$ transitions to respectively lead and lag the bit-center transition by 1/4 bit time. $\overline{RXC}$ is used to recover RXD by sampling the incoming data with an edge-triggered flip-flop.

The Frame_Detect signal informs the decoder that the first valid negative transition of a new frame has been detected. This signal is used to initiate the lock-on sequence of the decoder. Lock is achieved by reducing the time constant of the digital filter to zero at the start of a new frame. With a time constant of zero, the filter immediately outputs the phase of the second bit-center transition. Any uncertainty in the bit-center phase of the first transition that is caused by jitter is subsequently removed by gradually increasing the filter time constant during the following preamble. By that time, the exact phase of the bit center is output by the filter, and the lock is achieved. Lock is achieved within the first 14 bit times as seen by the RCV/$\overline{RCV}$ inputs. The maximum bit-cell timing distortion (jitter) tolerated by the Manchester Decoder Circuitry is ±12 ns for the preamble and ±18 ns for the data.

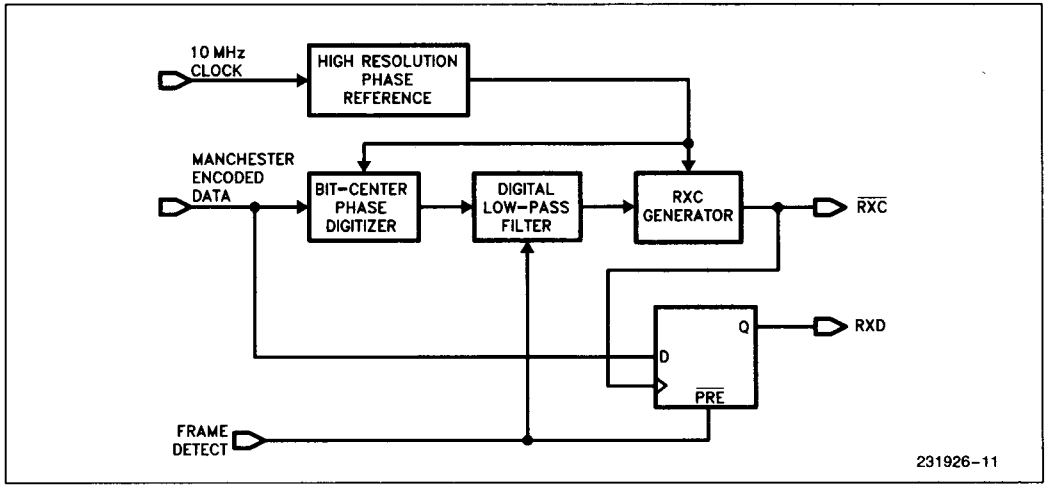


Figure 5. Manchester Decoder

COLLISION-PRESENCE SECTION

The CLSN/$\overline{CLSN}$ input signal is a 10 MHz +25%/−15% square-wave generated by the transceiver whenever two or more data frames are superimposed on the coaxial cable. The pulse width of the CLSN/$\overline{CLSN}$ signal can be no less than 35 ns and no greater than 70 ns measured at the 0-V crossing.

The common-mode voltage and external termination are identical to the RCV/$\overline{RCV}$ input. (See Figure 4.)

A valid collision presence signal will assert the 82C501AD $\overline{CDT}$ output, which can be directly tied to the $\overline{CDT}$ input of the Intel LAN Controller. During normal operation the 82C501AD logically "ORs" the collision presence signal with an internal signal, indicating valid data reception on the RCV/$\overline{RCV}$ pair, to generate $\overline{CRS}$ output. If, however, the $\overline{NOOR}$ input is asserted low, this "OR" function is removed and $\overline{CRS}$ is only asserted by the presence of valid data on the RCV/$\overline{RCV}$ pair. This mode of operation is required for repeater design.

During the time that valid collision-presence transitions are present on the CLSN/$\overline{CLSN}$ input, invalid data transitions may be present on the receive data pair due to the superposition of signals from two or more stations transmitting simultaneously. It is possible for RCV/$\overline{RCV}$ to lose transitions for a few bit times due to perfect cancellation of the signals; this may cause the 82C501AD to abort the reception.

The $\overline{CRS}$ signal is asserted low (along with $\overline{CDT}$) whenever a valid collision-presence signal is present and $\overline{NOOR}$ = 1. If this collision-presence signal arrives within 5 μs to 7 μs after the last transmission, only $\overline{CDT}$ is generated. This ensures that the LAN Controller recognizes the active $\overline{CDT}$ as a valid SQE (heartbeat) test signal.

NOISE FILTERING ON RCV AND CLSN PAIRS

Both the receive and collision pairs have the following characteristics.

- At idle, the noise filter is turned on.
- A pulse is rejected if:

a. Its peak voltage is more positive than −150 mV, with no restriction on width, or:

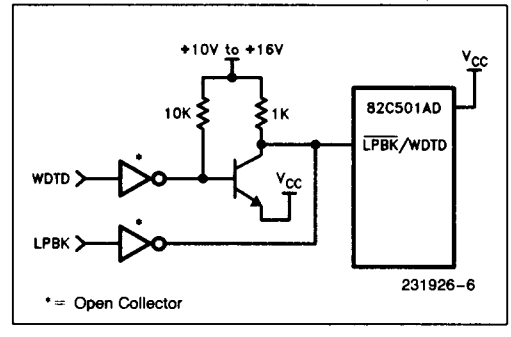
b. Its peak voltage is more positive than −600 mV and its width is less than 5 ns (measured at a reference level of −285 mV).

- The filter is turned off by the first valid negative pulse on the RCV or CLSN pair. A pulse whose peak voltage is more negative than −300 mV and whose width is greater than 30 ns (measured at −285 mV) is considered valid.
- The filter is turned on again when no positive transition is observed on the RCV or CLSN pair for 160 ns.

Internal Loopback

When asserted, $\overline{LPBK}$ causes the 82C501AD to route serial data from its TXD input through its transmit logic (retiming and Manchester encoding); returning it through the receive logic (Manchester decoding and receive clock generation) to RXD output. The internal routing prevents the data from passing through the output drivers and onto the transmit output pair TRMT/$\overline{TRMT}$. When in loopback mode all of the transmit and receive circuits, are tested except for the transceiver cable output driver and input receivers. Also, at the end of each frame transmitted in loopback mode the 82C501AD generates the SQE test (heartbeat) signal within 1 μs after the end of the frame. Thus, the collision circuits are also tested in loopback mode. During loopback, as in any normal reception, the 82C501AD receive circuitry uses 14 bit times while the Manchester Decoder locks on the data. As a result, the first 14 bits are lost and $\overline{RXC}$ is held low during that time.

The watchdog timer remains enabled in loopback mode, terminating test frames that exceed its timeout period. The watchdog timer can be inhibited by connecting $\overline{LPBK}$ to a 1 kΩ resistor connected to 10 to 16V. The loopback feature can still be used to test the integrity of the 82C501AD by using the circuit shown in Figure 6.



LPBK	WDTD	Function
1	X	LPBK mode
0	0	Normal mode
0	1	Normal mode with watchdog timer disabled

Figure 6. Watchdog Timer Disable

The 82C501AD operates as a full-duplex device, being able to transmit and receive simultaneously. By

combining the internal and external loopback modes of the Intel LAN Controller, and the internal loopback and normal modes of the 82C501AD, incremental testing of an Intel LAN Controller/82C501AD-based interface can be performed under program control for systematic fault detection and fault isolation.

Interface Example

The 82C501AD is designed to work directly with the Intel LAN Controller in IEEE 802.3 10 Mb/s, as well as other 10 Mb/s LAN applications. The control and data signals connect directly between the two devices without the need for additional external logic. The complete Intel LAN Controller/82C501AD Ethernet Transceiver interface is shown in Figure 4. The 82C501AD provides the driver and receivers needed to directly connect to the transceiver cable or requiring only terminating resistors on each input signal pair and 240Ω pull-down resistors.

It is recommended that a decoupling capacitor be used between V_{CC} and GND.

The Transmit, Receive, and Collision pairs have a maximum 10V overvoltage protection.

If additional high voltage protection is desired, a pulse transformer should be included for Ethernet applications. IEEE 802.3 10BASE5 (Ethernet) specifications require at least 16V protection for the Transmit, Receive, and Collision pairs. In 10BASE2 (Cheapernet) a pulse transformer is required to be inserted between the DTE (Intel LAN Controller/82C501AD) and the transceiver. In an Ethernet/Cheapernet design, a single transformer can be used for both connections at minimal additional cost.

The pulse transformer should have the following characteristics:

1. A minimum inductance of 75 μH.
2. 2000V isolation between primary and secondary windings.
3. 2000V isolation between primaries of separate transformers.

Since Ethernet Version 1.0 transceivers can require a positive differential on the TRMT pair during idle, check with the transceiver vendor before including the pulse transformer.

ABSOLUTE MAXIMUM RATING*

Case Temperature Under Bias .....0°C to +85°C
Storage Temperature .....−65°C to +140°C
All Output and Supply Voltages .....−0.5V to +7V
All Input Voltages .....−1.0V to +6.0V(1)
Operating Power Dissipation 0.75W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_C = 0°C to +85°C, V_{CC} = 5V ±10%

Symbol	Parameter		Min	Max
V_{IL}	Input Low Voltage	TTL MOS	−0.5V −0.5V	0.8V 0.6V
V_{IH}	Input High Voltage	TTL MOS	2.0V 3.9V	V_{CC} + 0.5V V_{CC} + 0.5V
V_{ACCEPT}	Differential Input Accept Voltage		±285 mV	
V_{REJECT}	Differential Input Reject Voltage			±150 mV
V_{CM}	Input Common Mode Voltage		0V	V_{CC}
V_{OCM}	Common Mode Output Voltage(2)		0.5V	5.0V
V_{OL}	Output Low Voltage @ I_{OL} = 4 mA			0.45V
V_{OH}	Output High Voltage (MOS) @ I_{OH} = −500 μA		3.9V	
V_{ODF}	Differential Output Voltage(2)		±0.45V	±1.2V
V_U	TRMT Pair Differential Return to Zero Undershoot(2)			−100 mV
V_{DI}	TRMT Pair Differential Idle Voltage(2)			±40 mV(5)
I_{LI}	Input Leakage Current @ V_{IN} = 0V to V_{CC}(3)			±10 μA
I_{CC}	Power Supply Current @ T_C = 85°C(4)			135 mA
I_{SP}	Short Protection Activation Current		60 mA	150 mA
I_L	Input Load Current(6)			±1 mA
C_{IN}	Input Capacitance @ fc = 1 MHz(7)			10 pF

NOTES:
1. The voltage levels for CLSN/$\overline{\text{CLSN}}$, RCV/$\overline{\text{RCV}}$ inputs are −0.75V to +10V.
2. The testing load is a 78Ω ±1% resistor in parallel with a 27 μH ±1% inductor and two 240Ω ±5% pulldown resistors.
3. Applies to TXD and $\overline{\text{TEN}}$ pins.
4. Part of the power is dissipated through the pulldown resistors connected to the TRMT/$\overline{\text{TRMT}}$ outputs.
5. Measured after t_{18} has expired.
6. Applies to RCV/$\overline{\text{RCV}}$, X_1, CLSN/$\overline{\text{CLSN}}$, $\overline{\text{LPBK}}$/WDTD, $\overline{\text{NOOR}}$, and $\overline{\text{ENETV1}}$ inputs for input voltages from 0V to V_{CC}.
7. Characterized, not tested.

A.C. MEASUREMENT CONDITIONS

1. T_C = 0°C to +85°C, V_{CC} = 5V ±10%.
2. The AC MOS, TTL and differential signals are referred to in Figures 7, 8, 9, 10 and 10A.
3. AC Loads:
   a) MOS: a 20 pF total capacitance to ground.
   b) Differential: a 10 pF total capacitance from each terminal to ground, two 240Ω ±5% pull down resistors, and a load resistor of 78Ω ±1% in parallel with a 27 μH ±1% inductor between terminals.
4. All AC Parameters become valid 100 μs after the supply voltage has stabilized.

Clock Timing(1)

Symbol	Parameter	Min	Max	Unit
t_1	X_1 Cycle Time	49.995	50.005	ns
t_2	X_1 Fall Time(2)		5	ns
t_3	X_1 Rise Time(2)		5	ns
t_4	X_1 Low Time(2)	15		ns
t_5	X_1 High Time(2)	15		ns

NOTES:
1. Refer to Figure 9.
2. Applies to external clock inputs.

TRANSMIT TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_6	$\overline{TXC}$ Cycle Time(2)	99.99	100.01	ns
t_7	$\overline{TXC}$ Rise/Fall Time		5	ns
t_8	TXD Rise/Fall Time		10	ns
t_9	$\overline{TXC}$ Low Time	40		ns
t_{10}	$\overline{TXC}$ High Time	40		ns
t_{11}	Transmit Enable/Disable to $\overline{TXC}$ Low	45		ns
t_{12}	TXD Stable to $\overline{TXC}$ Low	45		ns
t_{13}	Bit Cell Center to Bit Cell Center of Transmit Pair Data(3)	99.5	100.5	ns
t_{14}	$\overline{TEN}$ Rise/Fall Time		10	ns
t_{15}	Transmit Differential Signal Rise/Fall Time		5.0	ns
t_{16}	Bit Cell Center to Bit Cell Boundary of Transmit Pair Data(3)	49.5	50.5	ns
t_{17}	$\overline{TRMT}$ held low from Last Positive Transition of the Transmit Pair at the End of Frame	200		ns
t_{18}	From Last Positive Transition of Transmit Pair Differential Output Approaches Within 40 mV of zero volts.		8000	ns

NOTES:
1. Refer to Figure 11.
2. This parameter is exactly twice t_1.
3. Characterized, not tested.

RECEIVE TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{19}	Duration which the $\overline{RXC}$ is held at Low State at the Start of a Packet		1400	ns
t_{20}	Receive Pair Signal Rise/Fall Time(5)		10	ns
t_{21}	Receive Pair Bit Cell Center Jitter in Preamble(2)		±12	ns
t_{22}	Receive Pair Bit Cell Center Jitter in Data(2)		±18	ns
t_{23}	Receive Idle Time after Transmission in a Transmitting Station	8		μs
t_{24}	Receive Pair Signal Return to Zero Level from Last Valid Positive Transition	160		ns
t_{25}	$\overline{CRS}$ Assertion Delay from the First Received Valid Negative Transition of Receive Pair Signal		100	ns
t_{26}	$\overline{CRS}$ Deassertion Delay from the Last Valid Positive Transition Received (when no Collision-Presence Signal Exists on the Transceiver Cable)(3)		300	ns
t_{27}	$\overline{RXC}$ Cycle Time	96	104	ns
t_{28}	$\overline{RXC}$ Rise/Fall Time		5.0	ns
t_{29}	$\overline{RXC}$ Low Time	40		ns
t_{30}	$\overline{RXC}$ High Time	36		ns
t_{31}	Receive Data Stable Before the Negative Edge of $\overline{RXC}$	30		ns
t_{32}	Receive Data Held Valid Past the Negative Edge of $\overline{RXC}$	30		ns
t_{33}	Carrier Sense Active → Inactive Hold Time from $\overline{RXC}$ High	10	40	ns
t_{34}	Receive Data Rise/Fall Time(5)		10	ns
t_{35}	$\overline{CRS}$ Inhibit Time After Frame Transmission(4)	5	7	μs

NOTES:
1. Refer to Figures 12 and 13.
2. Measured per 802.3 Para B1.1.4.2 recommendations.
3. $\overline{CRS}$ is deasserted synchronously with the $\overline{RXC}$. This condition is not specified in the IEEE 802.3 specification.
4. Required for SQE test. Applies when $\overline{NOOR}$ = 1. For $\overline{NOOR}$ = 0 there is no inhibit of $\overline{CRS}$.
5. Characterized, not tested.

COLLISION TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{36}	CLSN/$\overline{\text{CLSN}}$ Cycle Time	80	118	ns
t_{37}	CLSN/$\overline{\text{CLSN}}$ Rise/Fall Time(2)		10	ns
t_{38}	CLSN/$\overline{\text{CLSN}}$ High/Low Time	35	70	ns
t_{39}	CLSN Pair Return to Zero from Last Positive Transition	160		ns
t_{40}	$\overline{\text{CDT}}$ Assertion from the First Valid Negative Edge of Collision Pair Signal		75	ns
t_{41}	$\overline{\text{CDT}}$ Deassertion from the Last Positive Edge of CLSN/$\overline{\text{CLSN}}$ Signal		300	ns
t_{42}	$\overline{\text{CRS}}$ Deassertion from the Last Positive Edge of CLSN/$\overline{\text{CLSN}}$ Signal (if no Post-Collision Signal Remains on the Receive Pair)		450	ns

NOTE:
1. Refer to Figure 14.
2. Characterized, not tested.

LOOPBACK TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{43}	$\overline{\text{LPBK}}$ asserted before the first attempted transmission (2)	500		ns
t_{44}	Simulated collision test delay from the end of each attempted transmission	0.5	1.5	μs
t_{45}	Simulated collision test duration(3)	0.6	1.6	μs
t_{46}	$\overline{\text{LPBK}}$ deasserted after the last attempted transmission	5		μs

NOTES:
1. Refer to Figure 15.
2. In Loopback mode, $\overline{\text{RXC}}$ and $\overline{\text{CRS}}$ function in the same manner as a normal Receive.
3. SQE test (heartbeat) signal

NOISE FILTER(1)

Symbol	Parameter	Min	Max	Unit
t_{47}	RCV/$\overline{\text{RCV}}$ Noise Filter Pulse Width Rejected		5	ns
t_{48}	RCV/$\overline{\text{RCV}}$ Noise Filter Pulse Width Accepted	30		ns
t_{49}	CLSN/$\overline{\text{CLSN}}$ Noise Filter Pulse Width Rejected		5	ns
t_{50}	CLSN/$\overline{\text{CLSN}}$ Noise Filter Pulse Width Accepted	25		ns

NOTE:
1. Refer to Figure 16.

A.C. TIMING CHARACTERISTICS

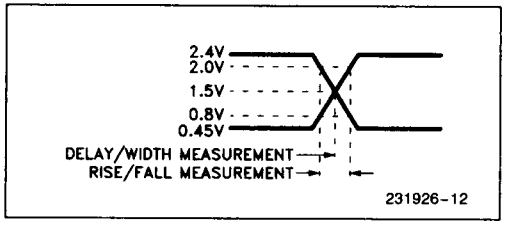


Figure 7. TTL Input Voltage Levels for Timing Measurements ($\overline{TEN}$, TXD, $\overline{LPBK}$/WDTD).

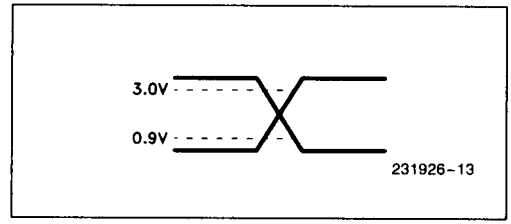


Figure 8. Voltage Levels for MOS Level Output-Timing Measurements ($\overline{TXC}$, $\overline{RXC}$, $\overline{CRS}$, $\overline{CDT}$, and RXD).

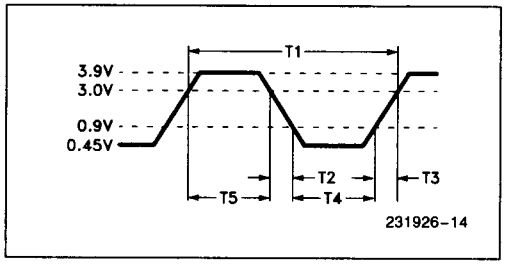


Figure 9. X1 Input Voltage Levels for Timing Measurements

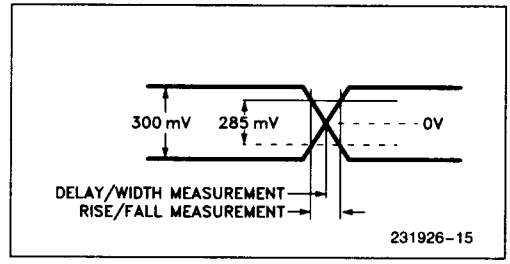


Figure 10. Voltage Levels for Differential-Input Timing Measurements (RCV/$\overline{RCV}$ and CLSN/$\overline{CLSN}$).

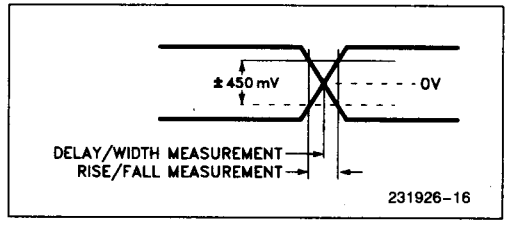


Figure 10A. Voltage Levels for TRMT/$\overline{TRMT}$ Output-Timing Measurements

TRANSMIT TIMING

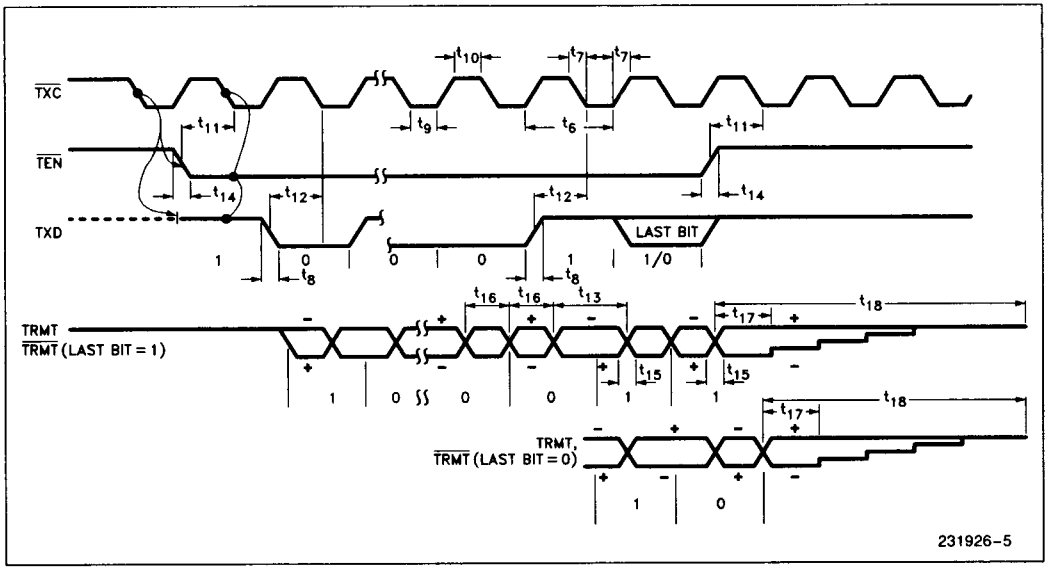


Figure 11

RECEIVE TIMING: START OF FRAME

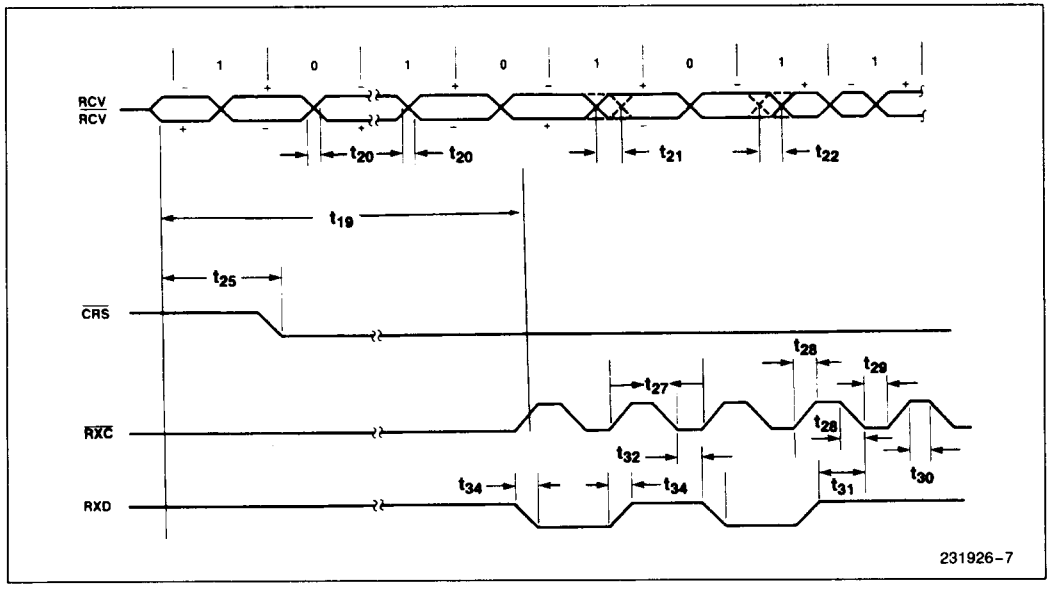


Figure 12

RECEIVE TIMING: END OF FRAME

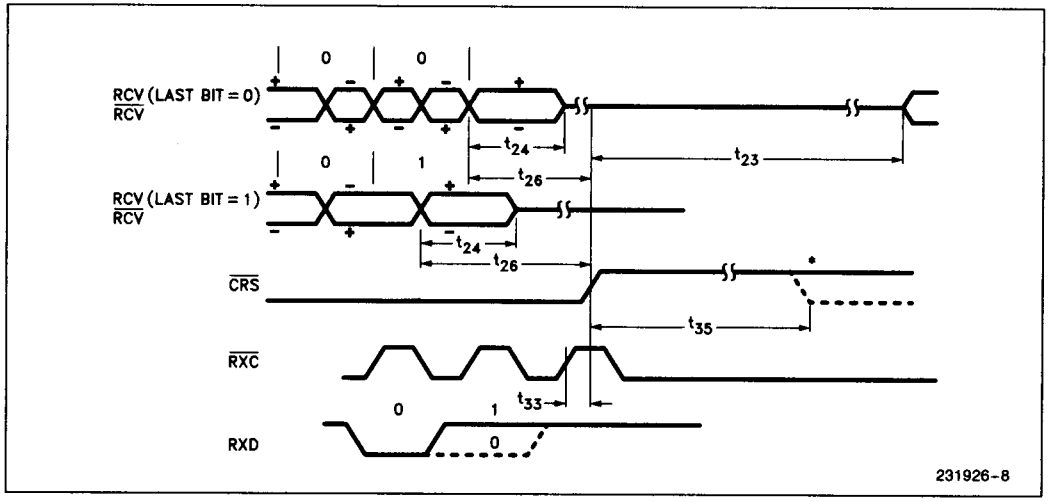


Figure 13

COLLISION TIMING

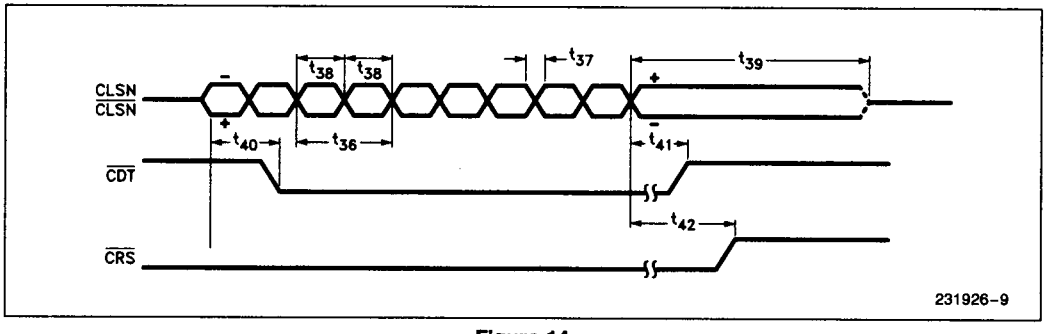


Figure 14

LOOPBACK TIMING

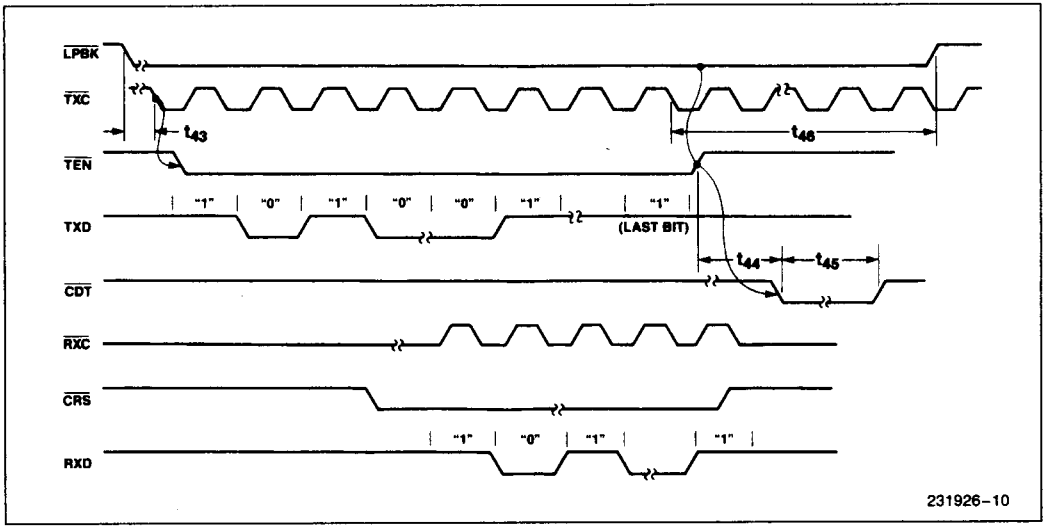


Figure 15

NOISE FILTER TIMING

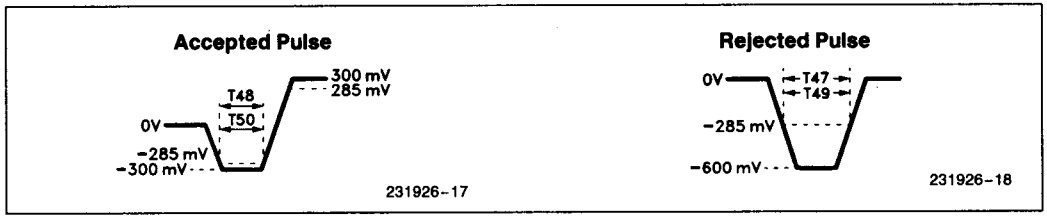
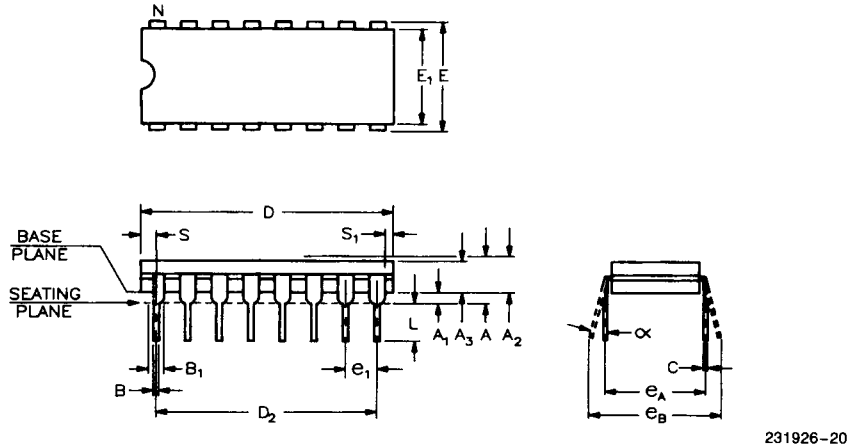


Figure 16. Noise Filter Characteristics

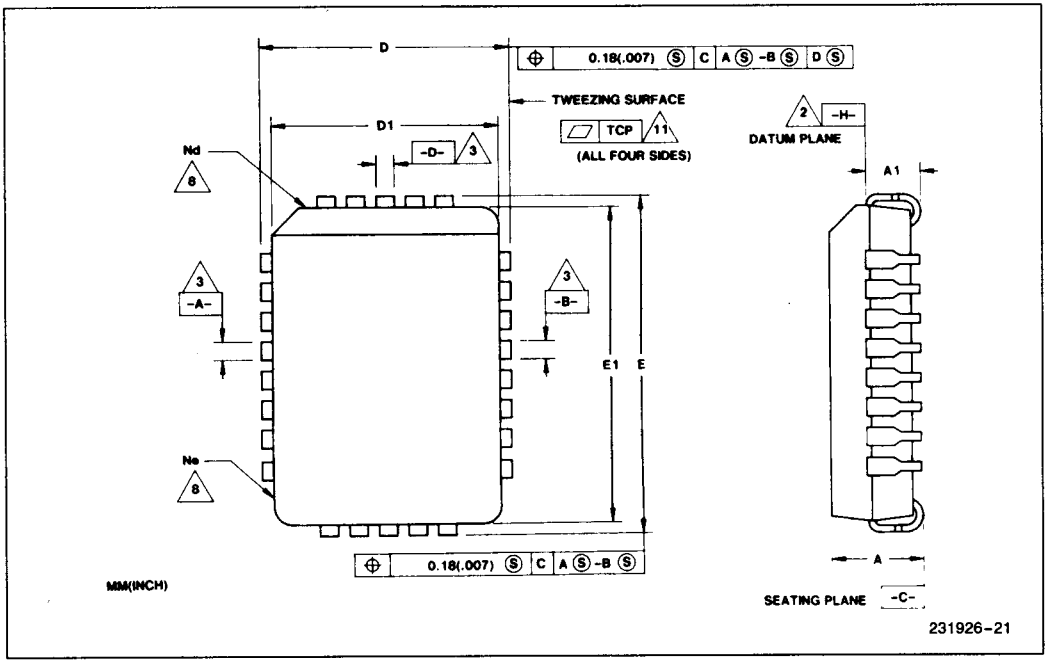
20 LEAD CERDIP DUAL IN-LINE PACKAGE INTEL TYPE D



231926-20

Family : CerDIP Dual-In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.24		0.140	0.167	
A_3	3.56	4.24		0.140	0.167	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	24.38	25.27	Reference	0.960	0.995	
D_2	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.90		0.280	0.31	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	20		½ Leads	20		½ Leads
S	0.38	1.78		0.015	0.070	
S_1	0.13			0.005		
ISSUE	IWS 1/15/87					

PLASTIC LEADED CHIP CARRIER RECTANGULAR



Dimension	28 Lead (Inch)		28 Lead (mm)	
	Min	Max	Min	Max
Overall Height (A)	0.126	0.140	3.20	3.56
Shoulder to Board Height (A_1)	0.076	0.090	1.93	2.29
Outside Dimension (D)	0.385	0.396	9.78	10.0
Plastic Body Dimension (D_1)	0.347	0.353	8.81	8.97
Foot Print (D_2)	0.290	0.330	7.37	8.38
Foot Print (D_3)	0.200 Ref.		5.08 Ref.	
Outside Dimension (E)	0.585	0.595	14.9	15.1
Platic Body Dimension (E_1)	0.547	0.553	13.9	14.0
Foot Print (E_2)	0.490	0.530	12.4	13.5
Foot Print (E_3)	0.400 Ref.		10.2 Ref.	
# of Leads (N)	28		28	
# of Leads on Short Side (N_d)	5		5	
# of Leads on Long Side (N_e)	9		9	
Seating Plane Coplanarity (CP)	0.000	0.004	0.00	0.10
Tweezing Coplanarity (TCP)	0.000	0.004	0.000	0.10
Lead Thickness (LT)	0.009	0.015	0.23	0.38
Issue	IWS 1/15/87			