MC74HCT244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High−Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. The device has non−inverted outputs and two active−low output enables.

The HCT244A is the noninverting version of the HCT240. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates
- **These devices are available in Pb−free package(s). Specifications herein apply to both standard and Pb−free devices. Please see our website at www.onsemi.com for specific Pb−free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

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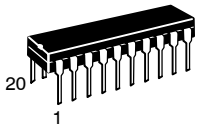
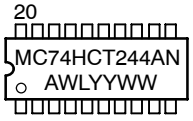
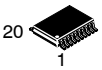
MARKING DIAGRAMS



PDIP−20
N SUFFIX
CASE 738



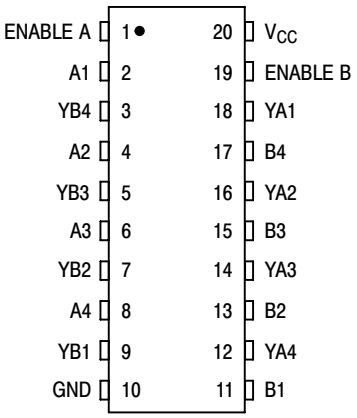
SOIC WIDE−20
DW SUFFIX
CASE 751D



TSSOP−20
DT SUFFIX
CASE 948E

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

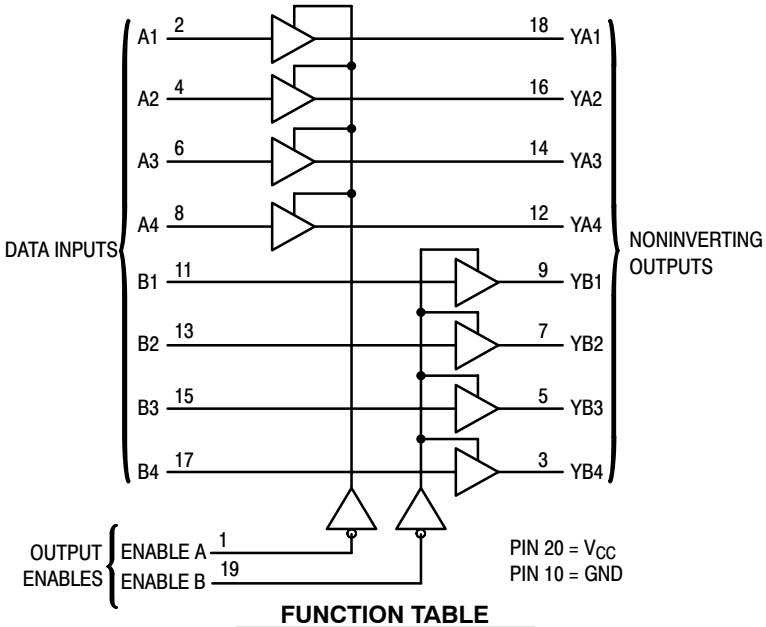
PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT244AN	PDIP−20	1440 / Box
MC74HCT244ADW	SOIC−WIDE	38 / Rail
MC74HCT244ADWR2	SOIC−WIDE	1000 / Reel
MC74HCT244ADT	TSSOP−20	75 / Rail
MC74HCT244ADTR2	TSSOP−20	2500 / Reel

LOGIC DIAGRAM



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance, X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7	V
V_{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C
SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2 2	2 2	2 2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ –55°C 2.9	25°C to 125°C 2.4	mA

NOTES:
1. Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	26	33	39	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	55	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

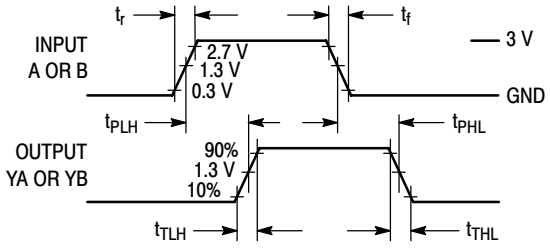


Figure 1.

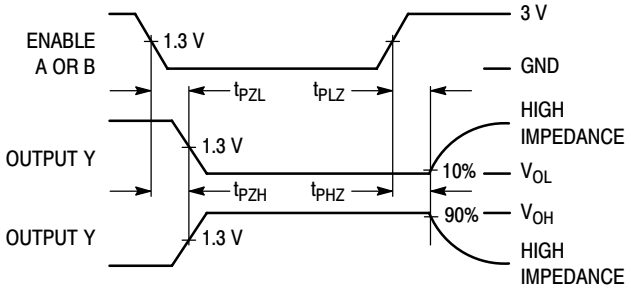
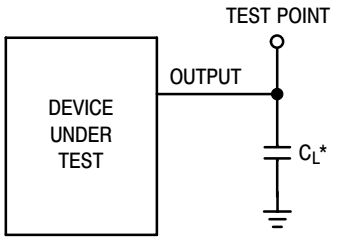


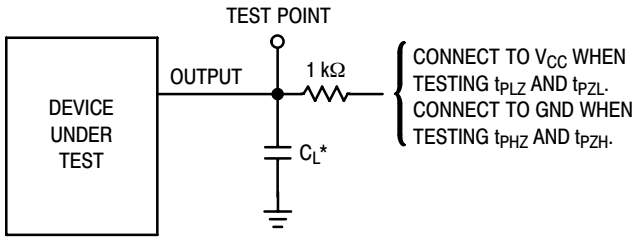
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

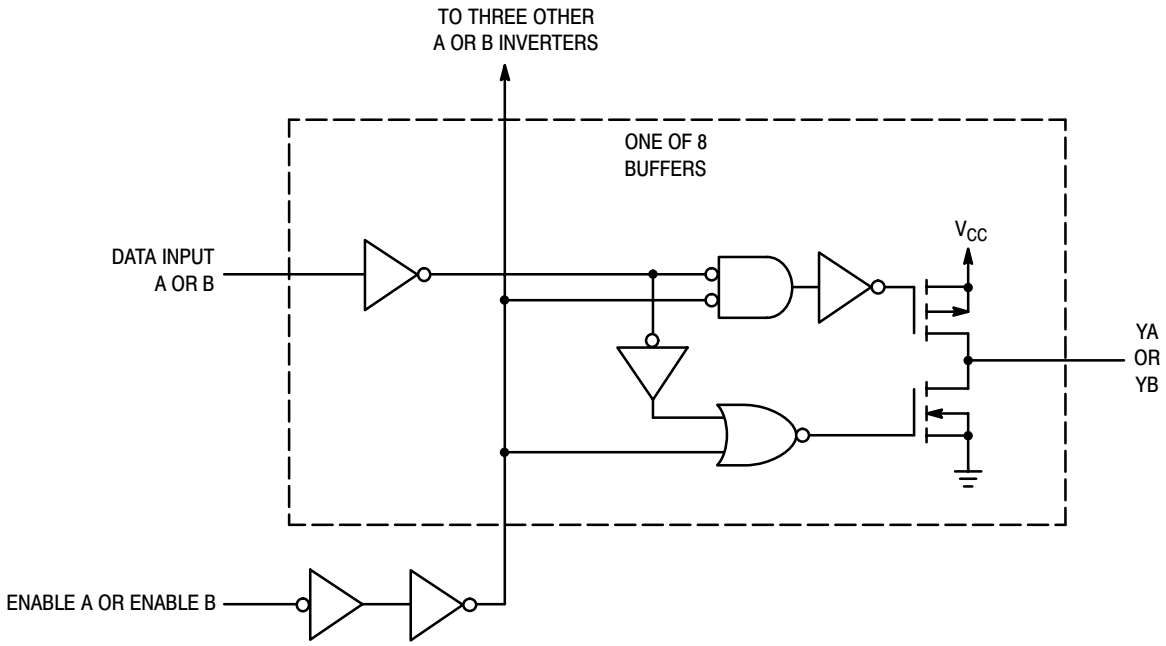
Figure 3.



*Includes all probe and jig capacitance

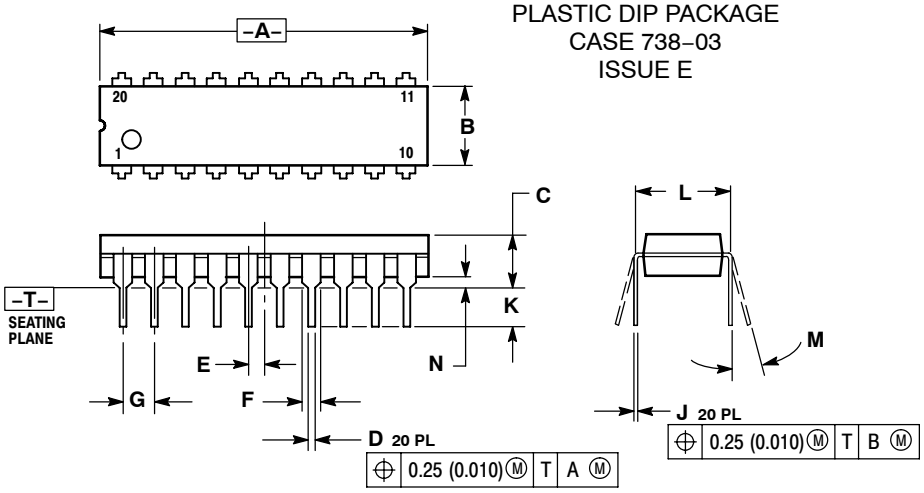
Figure 4.

LOGIC DETAIL



PACKAGE DIMENSIONS

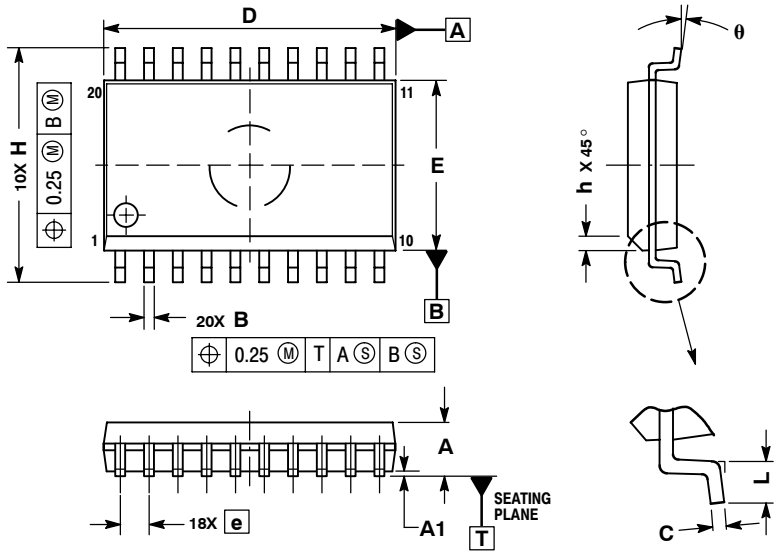
PDIP–20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO–20
DW SUFFIX
CASE 751D–05
ISSUE F

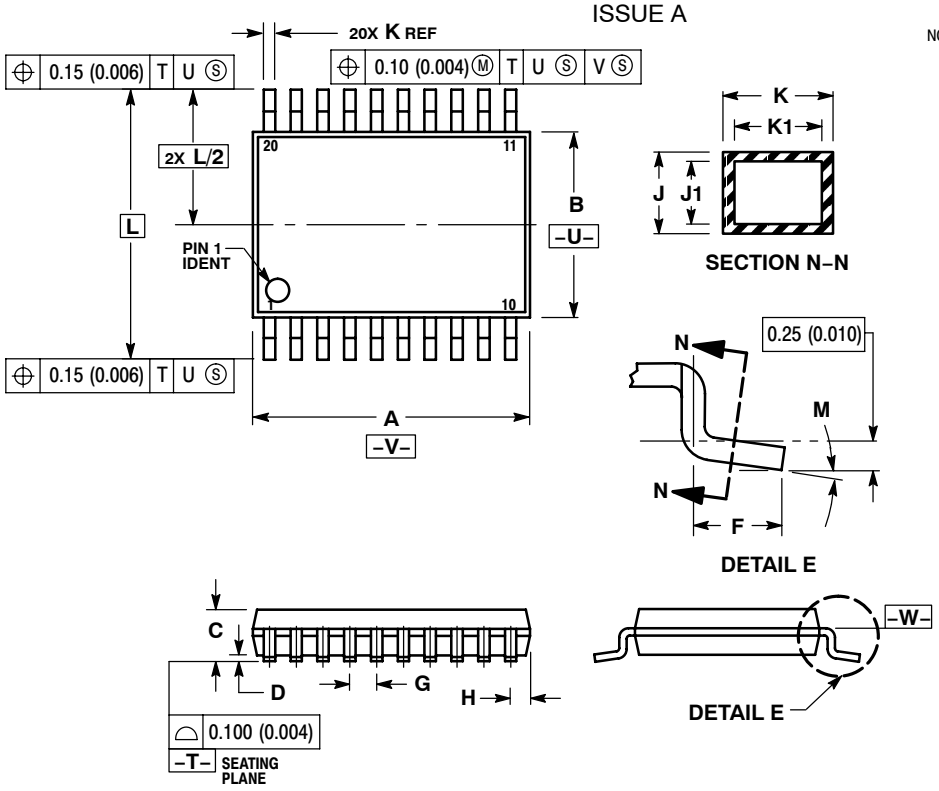


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP−20
DT SUFFIX
CASE 948E−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

PUBLICATION ORDERING INFORMATION

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Literature Distribution Center for ON Semiconductor
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