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Kind regards,

Team Nexperia

# PML340SN

N-channel TrenchMOS standard level FET

Rev. 01 — 24 August 2006

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a surface-mounted plastic package using TrenchMOS technology.

### 1.2 Features

- Standard level threshold
- Very low thermal impedance
- Low profile and small footprint
- Low on-state resistance

### 1.3 Applications

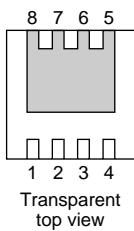
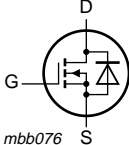
- Primary side switching
- DC-to-DC converters

### 1.4 Quick reference data

- $V_{DS} \leq 220$  V
- $R_{DS(on)} \leq 386$  m $\Omega$
- $I_D \leq 7.3$  A
- $Q_{GD} = 4.25$  nC (typ)

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
5, 6, 7, 8	drain (D)		

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### 3. Ordering information

**Table 2. Ordering information**

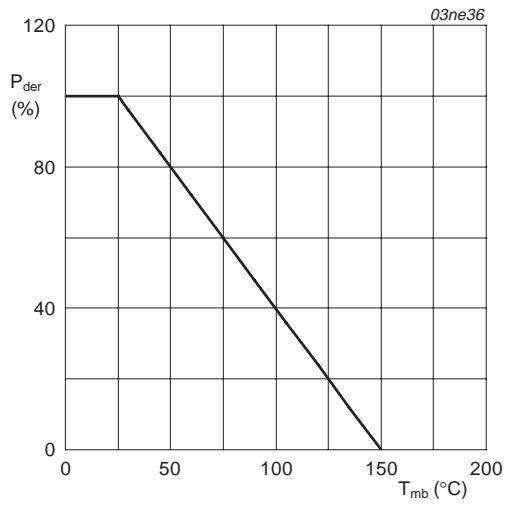
Type number	Package		Version
	Name	Description	
PML340SN	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3.3 × 3.3 × 0.85 mm	SOT873-1

### 4. Limiting values

**Table 3. Limiting values**

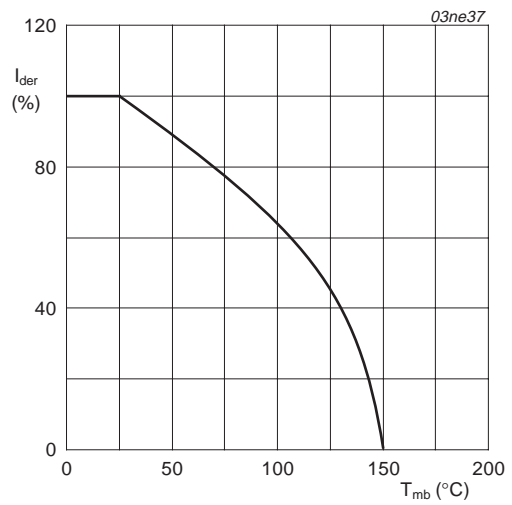
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	220	V
$V_{GS}$	gate-source voltage		-	±20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 2</a> and <a href="#">3</a>	-	7.3	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 2</a>	-	4.4	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see <a href="#">Figure 3</a>	-	14	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a>	-	50	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	7.6	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	14	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 3.5\text{ A};$ $t_p = 0.05\text{ ms}; V_{DS} \leq 220\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	-	22	mJ



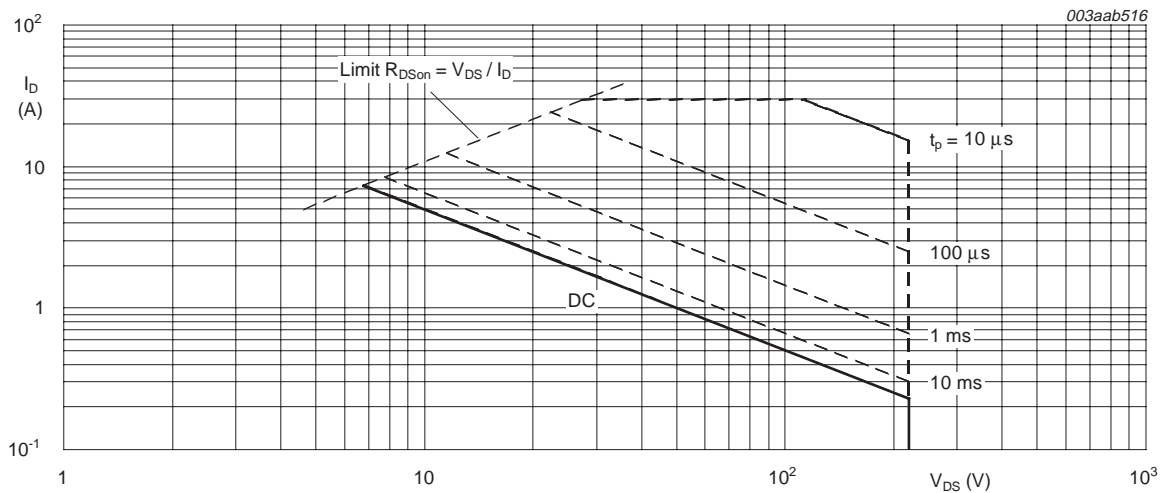
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2.5	K/W

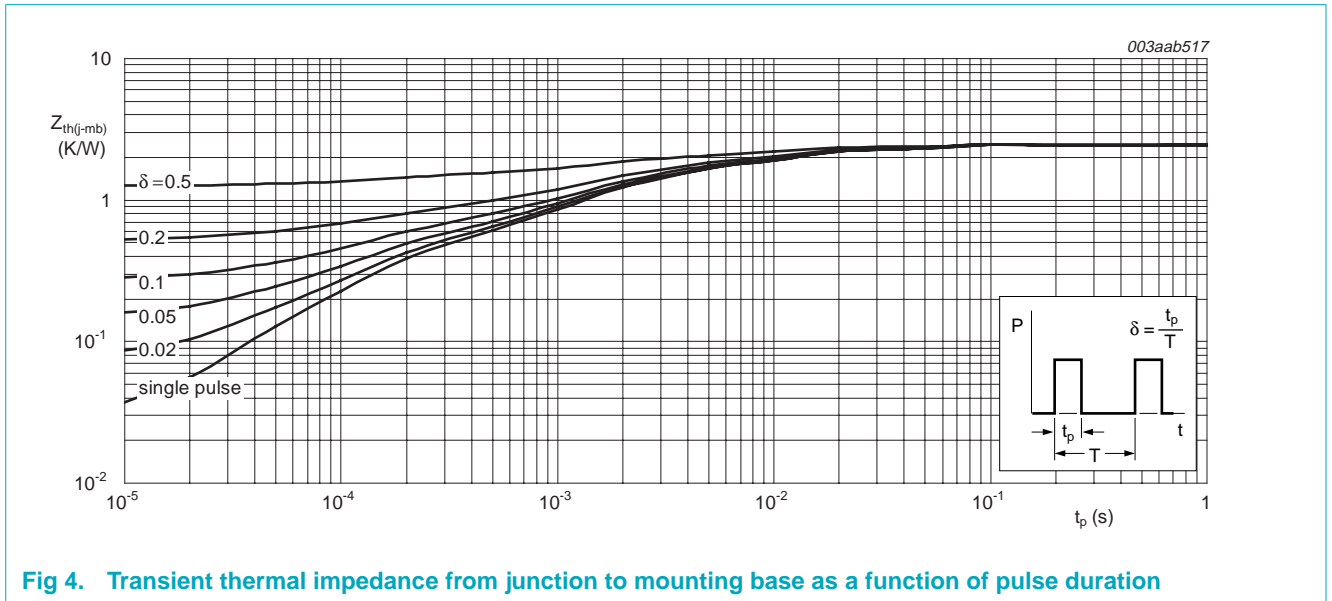


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	220	-	-	V
		$T_j = -55\text{ °C}$	196	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a> $T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 176\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\ \text{V}$ ; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_G$	gate resistance	$f = 1\ \text{MHz}$	-	0.6	-	$\Omega$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 2.6\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a> $T_j = 25\text{ °C}$	-	320	386	m $\Omega$
		$T_j = 150\text{ °C}$	-	768	927	m $\Omega$
		$V_{GS} = 6\ \text{V}$ ; $I_D = 2.5\ \text{A}$	-	330	396	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 2.6\ \text{A}$ ; $V_{DS} = 110\ \text{V}$ ; $V_{GS} = 10\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	13.2	-	nC
$Q_{GS}$	gate-source charge		-	2.5	-	nC
$Q_{GS1}$	pre- $V_{GS(th)}$ gate-source charge		-	1.72	-	nC
$Q_{GS2}$	post- $V_{GS(th)}$ gate-source charge		-	0.78	-	nC
$Q_{GD}$	gate-drain charge		-	4.25	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	4.35	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 30\ \text{V}$ ; $f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	656	-	pF
$C_{oss}$	output capacitance		-	69	-	pF
$C_{riss}$	reverse transfer capacitance		-	24	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 100\ \text{V}$ ; $R_L = 100\ \Omega$ ; $V_{GS} = 10\ \text{V}$ ; $R_G = 5.6\ \Omega$	-	9	-	ns
$t_r$	rise time		-	11.8	-	ns
$t_{d(off)}$	turn-off delay time		-	19.8	-	ns
$t_f$	fall time		-	4.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 2.8\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 3.2\ \text{A}$ ; $di_S/dt = -100\ \text{A}/\mu\text{s}$ ; $V_{GS} = 0\ \text{V}$ ;	-	111	-	ns
$Q_r$	recovered charge	$V_R = 120\ \text{V}$	-	340	-	nC

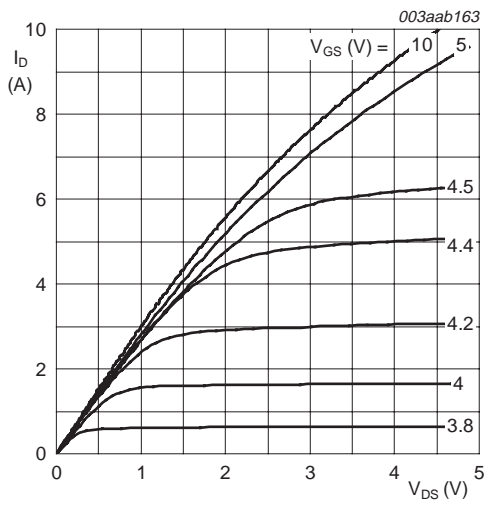


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

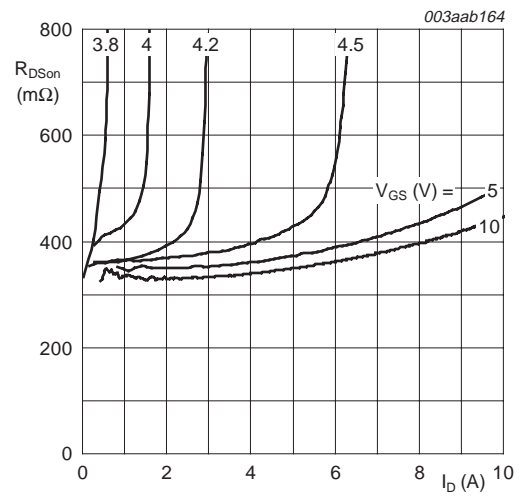


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

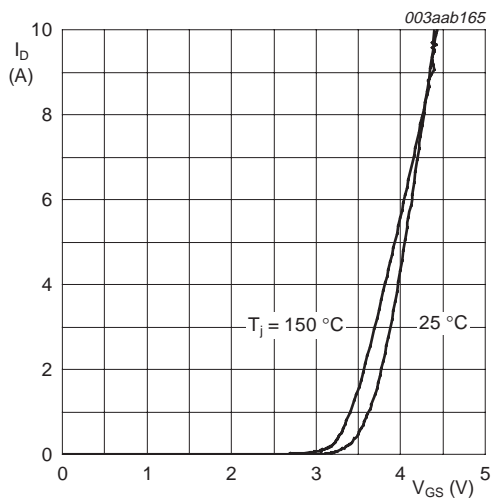
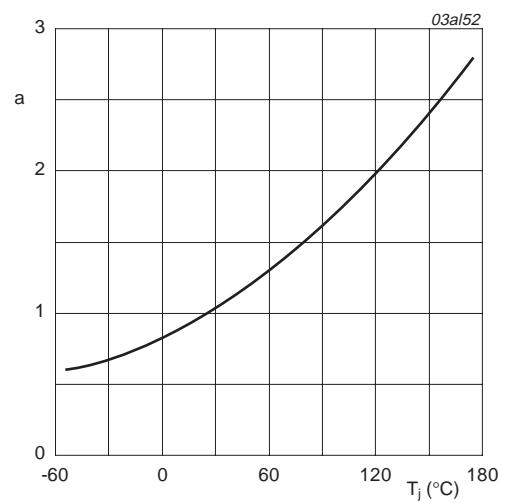
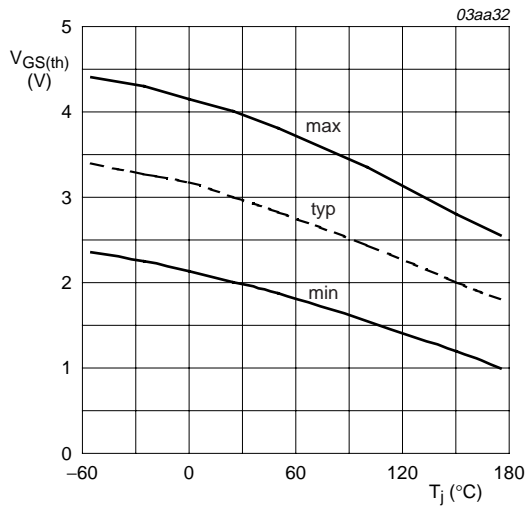


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



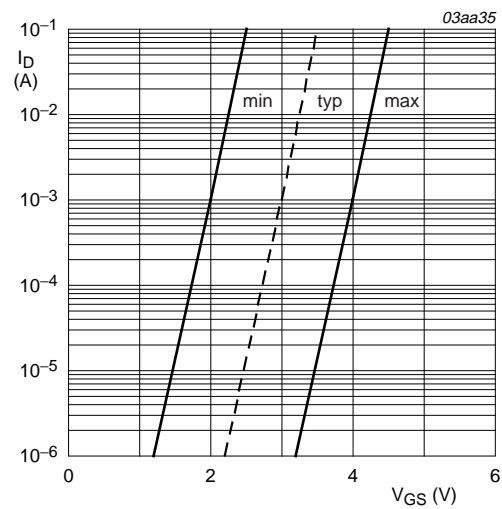
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



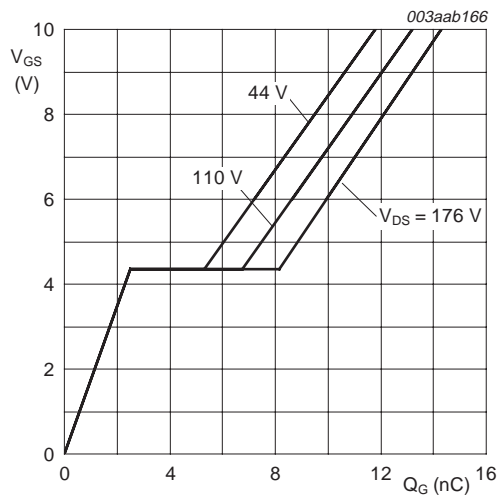
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



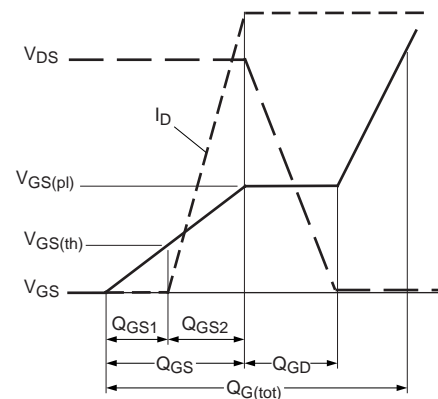
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



$I_D = 2.6 \text{ A}; V_{DS} = 110 \text{ V}$

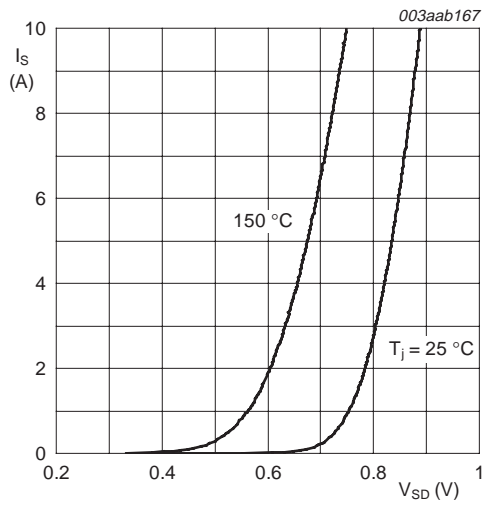
**Fig 11. Gate-source voltage as a function of gate charge; typical values**



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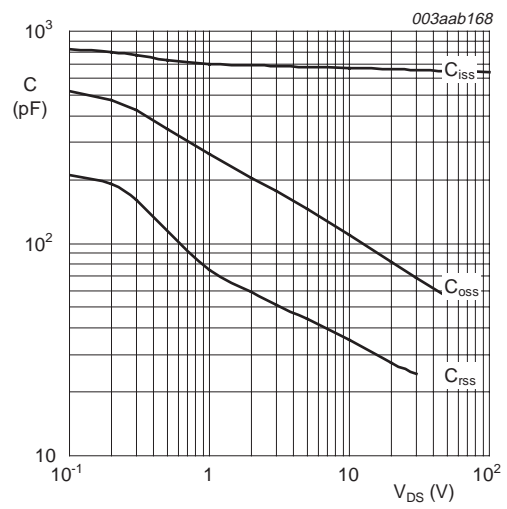
**Fig 12. Gate charge waveform definitions**





$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

7. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads;  
8 terminals; body 3.3 × 3.3 × 0.85 mm

SOT873-1

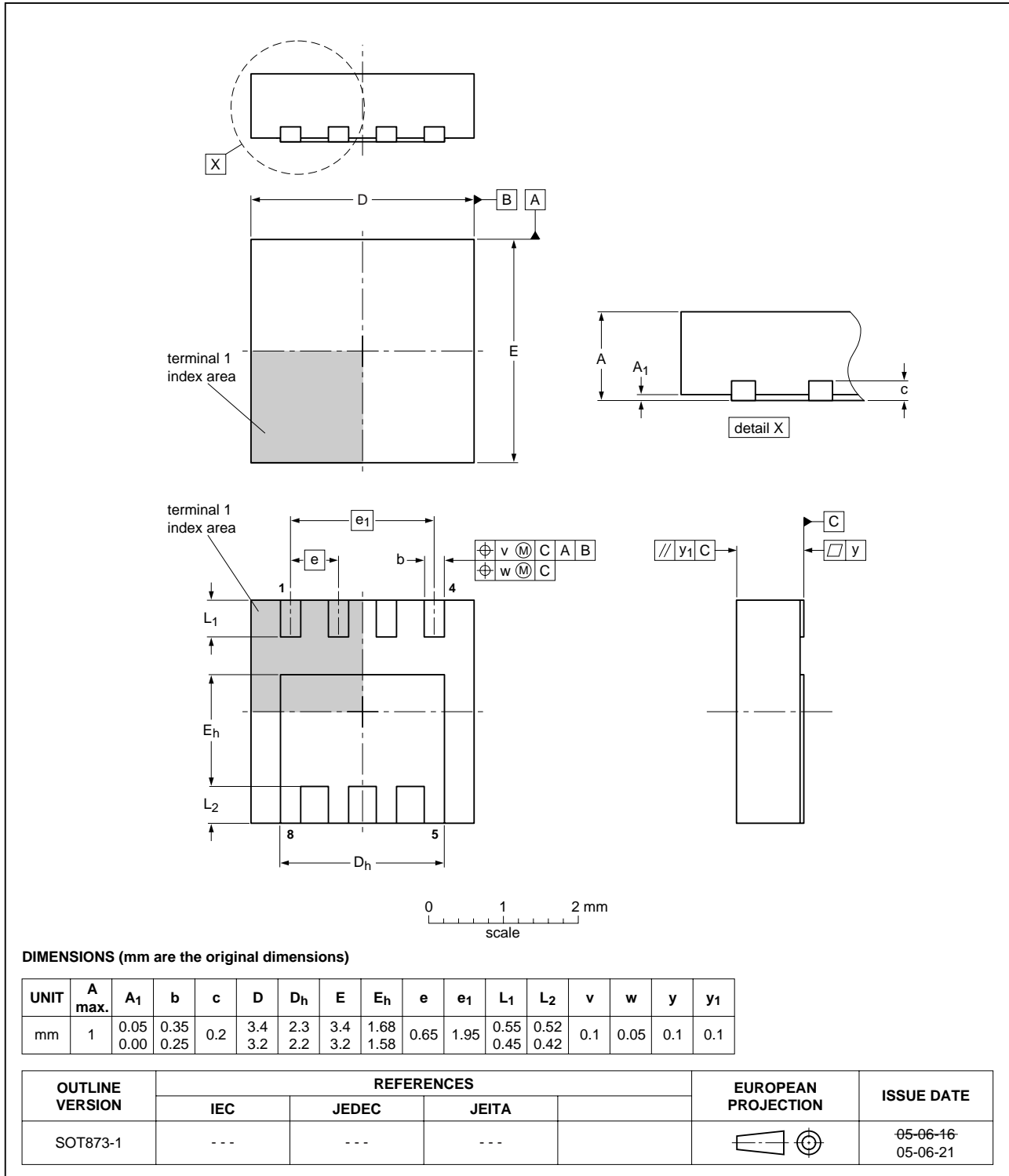


Fig 15. Package outline SOT873-1 (HVSON8)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PML340SN_1	20060824	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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