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T-46-07-11



# 74FCT563 Octal Latch with TRI-STATE® Outputs

## General Description

The 'FCT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

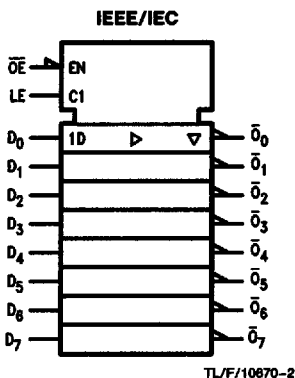
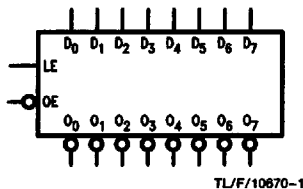
The 'FCT563 device is functionally identical to the 'FCT573, but with inverted outputs.

## Features

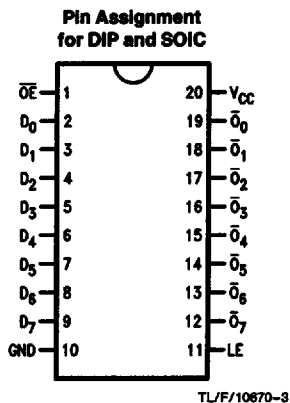
- $I_{CC}$  and  $I_{OZ}$  reduced to 40.0  $\mu$ A and  $\pm 2.5 \mu$ A respectively
- Inputs and outputs on opposite side of package allow easy interface with microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- $I_{OL} = 48$  mA
- CMOS power levels
- ESD immunity  $\geq 4$  kV typ

**Ordering Code:** See Section 8

## Logic Symbols



## Connection Diagram



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
OE	TRI-STATE Output Enable Input
$\bar{Q}_0$ - $\bar{Q}_7$	TRI-STATE Latch Outputs

### Functional Description

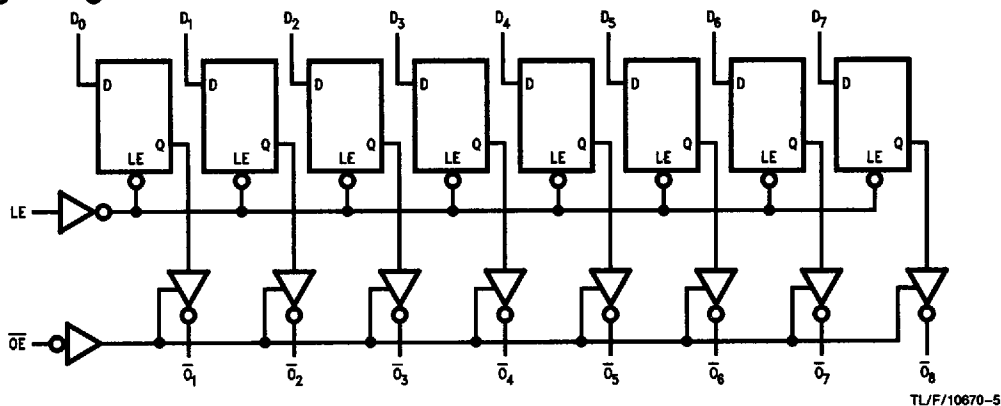
The 'FCT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the TRI-STATE mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs	Function
$\overline{OE}$	LE	D	O	
H	X	X	Z	High-Z
L	H	L	H	Transparent
L	H	H	L	Transparent
L	L	X	NC	Latched

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 NC = No Change

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND ( $V_{TERM}$ )	
74FCT	-0.5V to +7.0V
Temperature under Bias ( $T_{BIAS}$ )	
74FCT	-55°C to +125°C
Storage Temperature ( $T_{STG}$ )	
74FCT	-55°C to +125°C
DC Output Current ( $I_{OUT}$ )	120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
74FCT	4.75V to 5.25V
Input Voltage	0V to $V_{CC}$
Output Voltage	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74FCT	0°C to +70°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

### DC Characteristics for 'FCT Family Devices

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ;  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
$V_{IH}$	Minimum High Level Input Voltage	2.0			V		
$V_{IL}$	Maximum Low Level Input Voltage			0.8	V		
$I_{IH}$	Input High Current			5.0 5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Current			-5.0 -5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
$I_{OZ}$	Maximum TRI-STATE Current			2.5 2.5 -2.5 -2.5	$\mu A$	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = \text{GND}$
$V_{IK}$	Clamp Diode Voltage		-0.7	-1.2	V	$V_{CC} = \text{Min}; I_N = -18 \text{ mA}$	
$I_{OS}$	Short Circuit Current	-60	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = \text{GND}$	
$V_{OH}$	Minimum High Level Output Voltage	2.8	3.0		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$	
		$V_{HC}$ 2.4	$V_{CC}$ 4.3			$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -300 \mu A$ $I_{OH} = -15 \text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage		GND	0.2	V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OL} = 300 \mu A$	
			GND	0.2		$V_{CC} = \text{Min}$	$I_{OL} = 300 \mu A$
			0.3	0.50		$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48 \text{ mA}$

### DC Characteristics for FCT Family Devices

Typical values are at  $V_{CC} = 5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ;  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
$I_{CC}$	Maximum Quiescent Supply Current		1.0	40.0	$\mu A$	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC} \leq 0.2V$ $f_i = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	
$I_{CCD}$	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
$I_C$	Total Power Supply Current (Note 6)		1.5	4.5	mA	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		$LE = V_{CC}$ $f_i = 10 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
			3.0	8.0		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		$LE = V_{CC}$ $f_i = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
$V_H$	Input Hysteresis on LE Only		200		mV		

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Input Frequency

$N_i$  = Number of Inputs at  $f_i$

All currents are in milliamperes and all frequencies are in megahertz.

**AC Electrical Characteristics:** See Section 2 for Waveforms

Symbol	Parameter	74FCT	74FCT		Units	Fig. No.
		$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_A, V_{CC} = \text{Com}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$			
		Typ	Min (Note 1) Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $\bar{O}_n$	5.0	1.5	8.0	ns	2-8
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $\bar{O}_n$	9.0	2.0	13.0	ns	2-8
$t_{PZL}$ $t_{PZH}$	Output Enable Time	7.0	1.5	12.0	ns	2-11
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	6.0	1.5	7.5	ns	2-11
$t_S$	Set Up Time High or Low $D_n$ to LE	1.0	2.0	—	ns	2-11
$t_H$	Hold Time High or Low $D_n$ to LE	1.0	1.5	—	ns	2-10
$t_W$	LE Pulse Width High or Low	5.0	6.0	—	ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

**Capacitance**  $T_A = +25^\circ\text{C}, f = 1.0\text{MHz}$

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Input Capacitance	6	10	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0\text{V}$

Note: This parameter is measured at characterization but not tested.  
 $C_{OUT}$  for 74FCT only.