- Replaces SN74ABT328
- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V_{CC} and GND Pins Reduce Switching Noise
- High-Drive Outputs (–15-mA I_{OH}, 64-mA I_{OL})
- State-of-the-Art *EPIC-IIB* ™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages

(TOP VIEW) GND 16 1Y1 1Y2 🛮 2 15 1T/C 2Y1 **∏**3 14 V_{CC} GND ∏4 2T/C 2Y2 [5 12] ∨<u>c</u>c 3Y **∏** 6 GND ∏7 10 3T/C 9 1 4T/C 4Y

D OR DB PACKAGE

description

The CDC328 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs (\overline{T}/C) , various combinations of true and complementary outputs can be obtained.

The CDC328 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUT	OUTPUT		
T,	/C	Α	Υ	
	L	L	L	
	L	Н	Н	
	Н	L	Н	
	Н	Н	L	

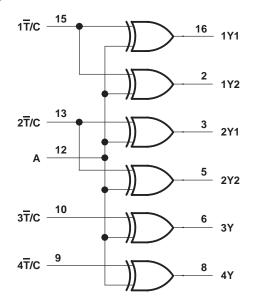
logic symbol†

Α	12	\triangleright	1	16	1Y1
1 <u>T</u> /C	15	N1	- 1	2	1Y2
2T/C	13		1	3	
21/6		N2	2	5	2Y1
3 T /C	10		2	6	2Y2
	9	N3	3	8	3Y
4T/C		N4	4		4Y

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V	to 7 V
Input voltage range, V _I (see Note 1) –0.5 V	to 7 V
Voltage range applied to any output in the high state	
or power-off state, V _O (see Note 1)	· 0.5 V
Current into any output in the low state, I _O	28 mA
Input clamp current, I_{IK} ($V_I < 0$)	18 mA
Output clamp current, I _{OK} (V _O < 0) –5	50 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) 100	00 mW
Storage temperature range, T _{stg} –65°C to	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
VI	Input voltage	0		VCC	V
ІОН	High-level output current			-15	mA
loL	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
fclock	Input clock frequency			80	MHz
TA	Operating free-air temperature	-40		85	°C

NOTE 3: Unused inputs must be held high or low.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} For operation above 25°C free-air temperature, derate to 478 mW at 85°C at the rate of 8.7 mW/°C.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MAX	UNIT
VIK	V _{CC} = 4.75 V,	$I_{I} = -18 \text{ mA}$				-1.2	V
Voн	V _{CC} = 4.75 V,	$I_{OH} = -15 \text{ mA}$		2.5			V
V _{OL}	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 64 \text{ mA}$				0.55	V
IĮ	$V_{CC} = 5.25 \text{ V},$	$V_I = V_{CC}$ or GND				±1	μΑ
IO [‡]	V _{CC} = 5.25 V,	V _O = 2.5 V		-15		-100	mA
loo	V _{CC} = 5.25 V,	$I_{O} = 0$,	Outputs high			50	μΑ
lcc	$V_I = V_{CC}$ or GND		Outputs low		20	30	mA
C _i	V _I = 2.5 V or 0.5 V				3		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

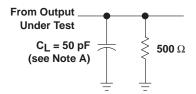
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
^t PLH	_	Any V	1.7		7	ns
^t PHL	A	Any Y	1.5		5.4	
^t PLH	T/C	Any V	1.5		8	no
^t PHL	1/C	Any Y	1.4		6.6	ns
*	Any Y (same phase)				0.7	no
^t sk(o)	A	Any Y (any phase)			2.6	ns
t _r				1.2		ns
t _f				0.5		ns

switching characteristics, V_{CC} = 5 V \pm 0.25 V, T_A = 25°C to 70°C (see Figures 1 and 2)

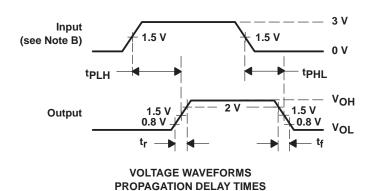
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
^t PLH	Λ.	Any Y	2.1	6.1	ns
t _{PHL}	κ	Ally I	1.7	4.8	115
4.7.	^	Any Y (same phase)		0.7	no
^t sk(o)	A	Any Y (any phase)		2.1	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C ‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



NOTES: A. C_L includes probe and jig capacitance.

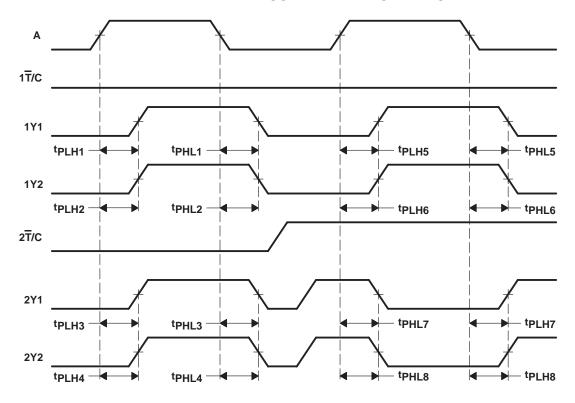
B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.

Figure 1. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(0)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs (\overline{T}/C) are at the same logic level. It is calculated as the greater of:

- The difference between the fastest and slowest of tpLH from A↑ to any Y (e.g., tpLHn, n = 1 to 4; or tpLHn, n = 5 to 6)
- The difference between the fastest and slowest of tp_{HL} from A↓ to any Y (e.g., tp_{HLn}, n = 1 to 4; or tp_{HLn}, n = 5 to 6)
- The difference between the fastest and slowest of tpLH from A↓ to any Y (e.g., tpLHn, n = 7 to 8)
- The difference between the fastest and slowest of tpHL from A↑ to any Y (e.g., tpHLn, n = 7 to 8)
- B. Output skew, $t_{sk(0)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs (\overline{T}/C) are at the same or different logic levels. It is calculated as the greater of:
 - The difference between the fastest and slowest of tp_{LH} from A[↑] to any Y or tp_{HL} from A[↑] to any Y (e.g., tp_{LHn}, n = 1 to 4; or tp_{LHn}, n = 5 to 6, and tp_{HLn}, n = 7 to 8)
 - The difference between the fastest and slowest of tpHL from A↓ to any Y or tpLH from A↓ to any Y (e.g., tpHLn, n = 1 to 4; or tpHLn, n = 5 to 6, and tpLHn, n = 7 to 8)

Figure 2. Waveforms for Calculation of t_{sk(o)}





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC328D	OBSOLETE	SOIC	D	16	TBD	Call TI	Call TI
CDC328DBLE	OBSOLETE	SSOP	DB	16	TBD	Call TI	Call TI
CDC328DR	OBSOLETE	SOIC	D	16	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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