Digitally Controlled Potentiometer (XDCP™)

The Intersil X9116 is a digitally controlled nonvolatile potentiometer designed to be used in trimmer applications. The pot consists of 15 equal resistor segments that connect to the wiper pin through programmable CMOS switches. The tap position is programmed through a 3-wire up/down serial port. The last position of the wiper is stored in a nonvolatile memory location which is recalled at the time of power up of the device.

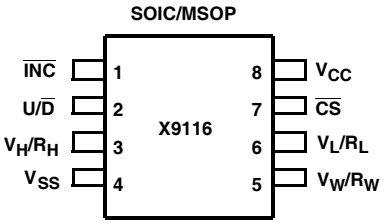
The wiper moves through sequential tap positions with inputs on the serial port. A falling edge on INC (bar) causes the tap position to increment one position up or down based on whether the U/D (bar) pin is held high or low.

The X9116 can be used in many applications requiring a variable resistance. In many cases it can replace a mechanical trimmer and offers many advantages such as temperature and time stability as well as the reliability of a solid state solution.

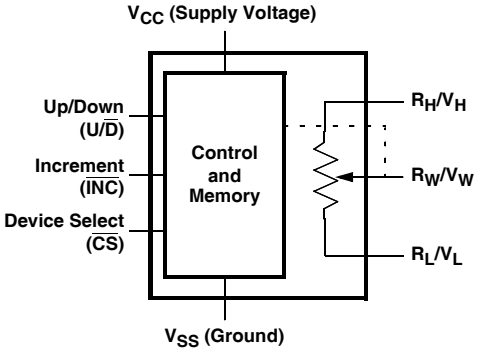
Features

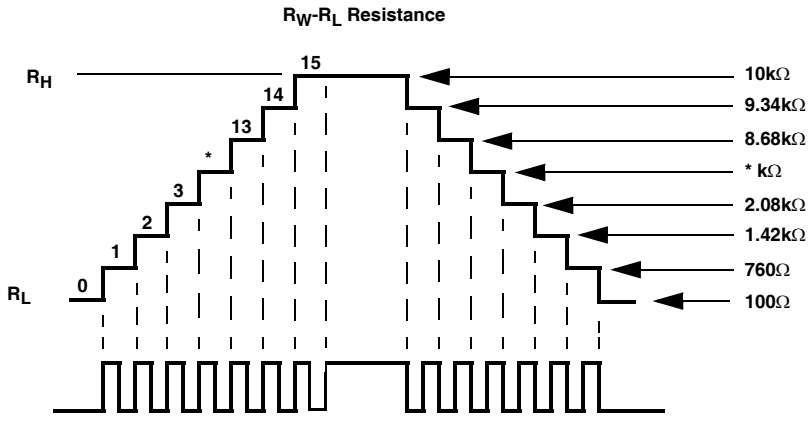
- Solid-state nonvolatile
- 16 wiper taps
- 3-wire up/down serial interface
- V_{CC} = 2.7V and 5V
- Active current < 50µA max.
- Standby current < 1µA max.
- R_{TOTAL} = 10kΩ
- Packages: 8 Ld MSOP, 8 Ld SOIC
- Pb-free plus anneal available (RoHS compliant)

Pinout



Block Diagram





Ordering Information

PART NUMBER (BRAND)	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X9116WM8T1	AAZ	5V ±10%	10	0 to +70	8 Ld MSOP Tape and Reel	M8.118
X9116WM8ZT1 (Note)	AKY			0 to +70	8 Ld MSOP (Pb-free) Tape and Reel	M8.118
X9116WM8I*	AFL			-40 to +85	8 Ld MSOP	M8.118
X9116WM8IZ* (Note)	DCG			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9116WS8*	X9116W			0 to +70	8 Ld SOIC	M8.15
X9116WS8Z* (Note)	X9116W Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9116WS8I*	X9116W I			-40 to +85	8 Ld SOIC	M8.15
X9116WS8IZ* (Note)	X9116W ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15
X9116WM8-2.7**	AFK	-2.7-5.5		0 to +70	8 Ld MSOP	M8.118
X9116WM8Z-2.7* (Note)	AOJ			0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9116WM8I-2.7*	ABA			-40 to +85	8 Ld MSOP	M8.118
X9116WM8IZ-2.7* (Note)	AKS			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9116WS8-2.7*	X9116W F			0 to +70	8 Ld SOIC	M8.15
X9116WS8Z-2.7* (Note)	X9116W ZF			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9116WS8I-2.7*	X9116W G			-40 to +85	8 Ld SOIC	M8.15
X9116WS8IZ-2.7* (Note)	X9116W ZG			-40 to +85	8 Ld SOIC (Pb-free)	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add "T1" suffix for tape and reel.
**Add “T2” suffix for tape and reel.

Pin Descriptions

V_H /R_H and V_L /R_L

The high (V_H/R_H) and low (V_L/R_L) terminals of the X9116 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}.

V_W/R_W

R_W/R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω to 400Ω depending upon V_{CC}.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented (up) or decremented (down).

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9116 will be placed in the low power standby mode until the device is selected once again.

Pin Descriptions

SYMBOL	DESCRIPTION
V_H/R_H	High Terminal
V_W/R_W	Wiper Terminal
V_L/R_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Control Input
$\overline{INC}$	Increment Control Input
$\overline{CS}$	Chip Select Input

Principles of Operation

There are three sections of the X9116: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 15 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper pin.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a four bit counter. The output of this counter is decoded to select one of 16 wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9116, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

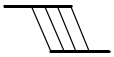
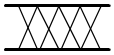
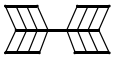
This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, V_H/R_H, V_L/R_L
and V_{CC} with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = |V_H/R_H - V_L/R_L|$ 5.5V
Lead temperature (soldering, 10 seconds) . . . . . +300°C
I_W (10 seconds) . . . . . ±10.0mA

Recommended Operating Conditions

Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage (V_{CC}) Limits
X9116 . . . . . 5V ± 10%
X9116-2.7 . . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Potentiometer Specifications Over recommended operating conditions unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
R_{TOTAL}	End to end resistance variation		-20		+20	%
V_{VH}	V_H/R_H terminal voltage	V_{SS} = 0V	V_{SS}		V_{CC}	V
V_{VL}	V_L/R_L terminal voltage	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Power rating	R_{TOTAL} = 10kΩ			10	mW
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 5V		200	400	Ω
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 2.7V		400	1000	Ω
I_W	Wiper current		-5.0		+5.0	mA
	Noise	Ref: 1kHz		-120		dBV$\sqrt{Hz}$
	Resolution			6		%
	Absolute linearity (Note 1)	$V_{w(n)(actual)} - V_{w(n)(expected)}$	-1		+1	MI (Note 3)
	Relative linearity (Note 2)	$V_{w(n+1)} - [V_{w(n)} + MI]$	-0.2		+0.2	MI (Note 3)
	R_{TOTAL} temperature coefficient			±300		ppm/°C
	Ratiometric temperature coefficient				±20	ppm/°C
$C_H/C_L/C_W$	Potentiometer capacitances	See Circuit #3		10/10/25		pF

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) - $V_{w(n)}$(expected)) = ±1 MI Maximum.
2. Relative linearity is a measure of the error in step size between taps = $V_{W(n+1)}$ -[$V_{w(n)}$ + MI] = ±0.2 MI.
3. 1 MI = Minimum Increment = R_{TOT}/15.

DC Electrical Specifications

Over recommended operating conditions unless otherwise specified

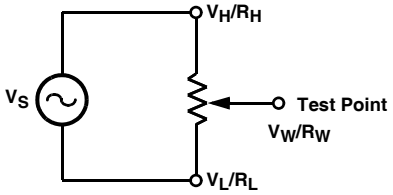
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNIT
I_{CC1}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ max t_{CYC}			150	µA
I_{CC2}	V_{CC} active current (Store) (EEPROM Store)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max t_{WR}			400	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V			1	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		2V		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-0.5		0.8	V
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz			10	pF

4. Typical values are for T_A = +25°C and nominal supply voltage.
5. This parameter is periodically sampled and not 100% tested.

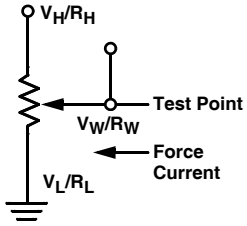
Endurance And Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

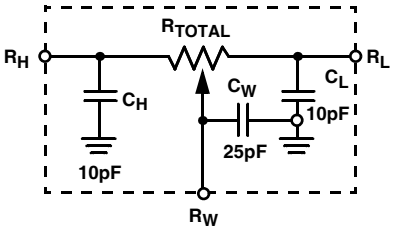
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



A.C. Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

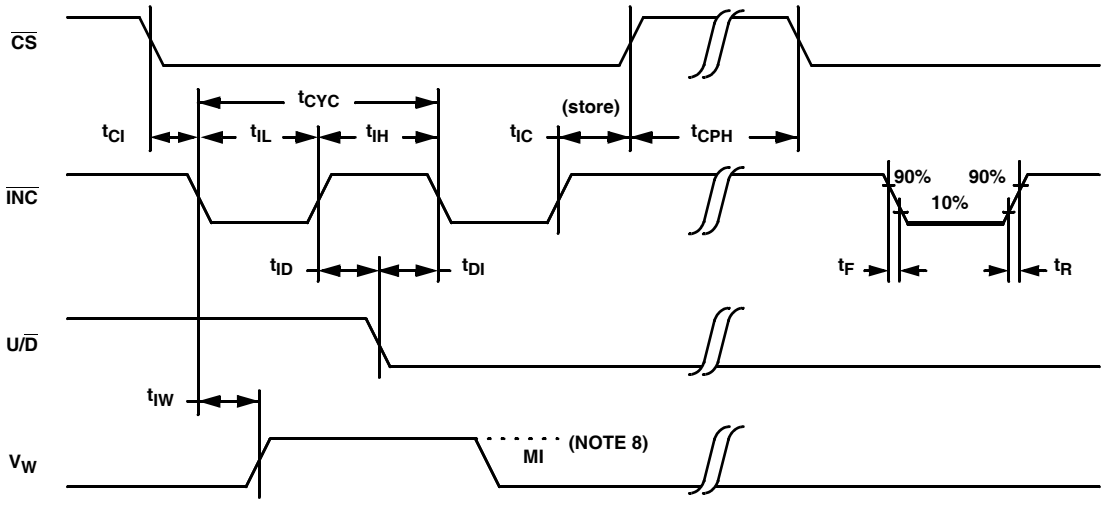
DC Electrical Specifications Over recommended operating conditions unless otherwise specified

SYMBOL	PARAMETER	MIN	TYP (NOTE 6)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPH}	$\overline{CS}$ deselect time (STORE)	10			ms
t_{IW}	$\overline{INC}$ to Vw change		1	5	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F (Note 7)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU} (Note 7)	Power up to wiper stable			5	µs
t_R V_{CC} (Note 7)	V_{CC} Power-up rate	15		50	mV/µs
t_{WR}	Store cycle		5	10	ms

Power Up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H$, V_L, V_W. The V_{CC} ramp rate spec is always in effect.

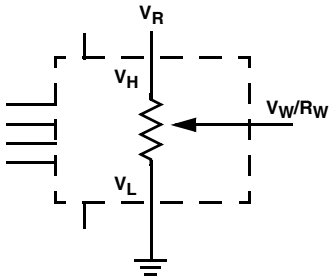
A.C. Timing



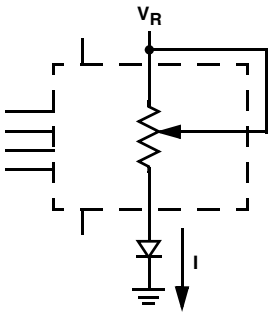
NOTES:

6. Typical values are for T_A = +25°C and nominal supply voltage.
7. This parameter is not 100% tested.
8. MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Basic Configurations of Electronic Potentiometers



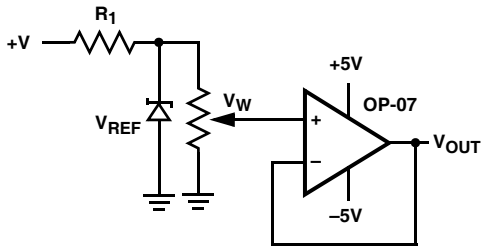
THREE-TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



TWO-TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

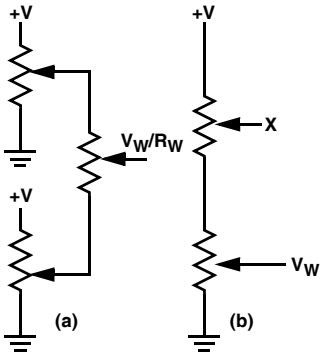
Basic Circuits

BUFFERED REFERENCE VOLTAGE

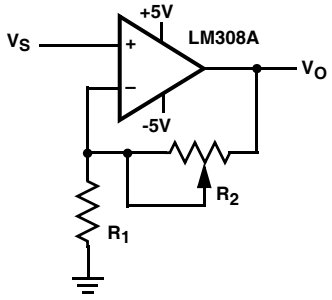


$V_{OUT} = V_W/R_W$

CASCADING TECHNIQUES

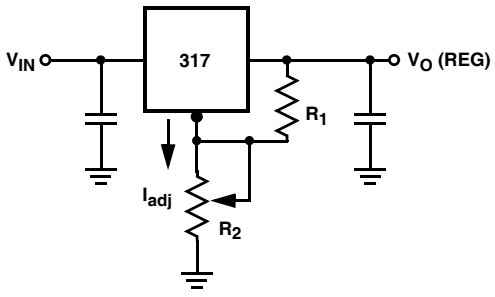


NONINVERTING AMPLIFIER



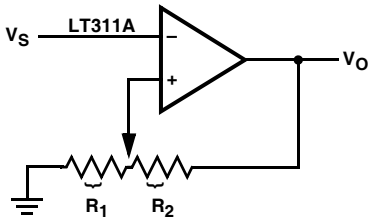
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR



V_O (REG) = 1.25V (1+R_2/R_1)+Iadj R_2

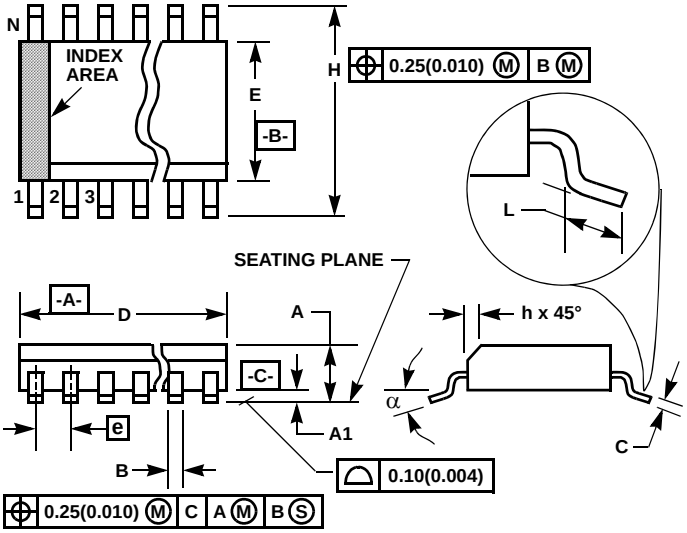
COMPARATOR WITH HYSTERESIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

(FOR ADDITIONAL CIRCUITS, SEE AN115)

Small Outline Plastic Packages (SOIC)



NOTES:

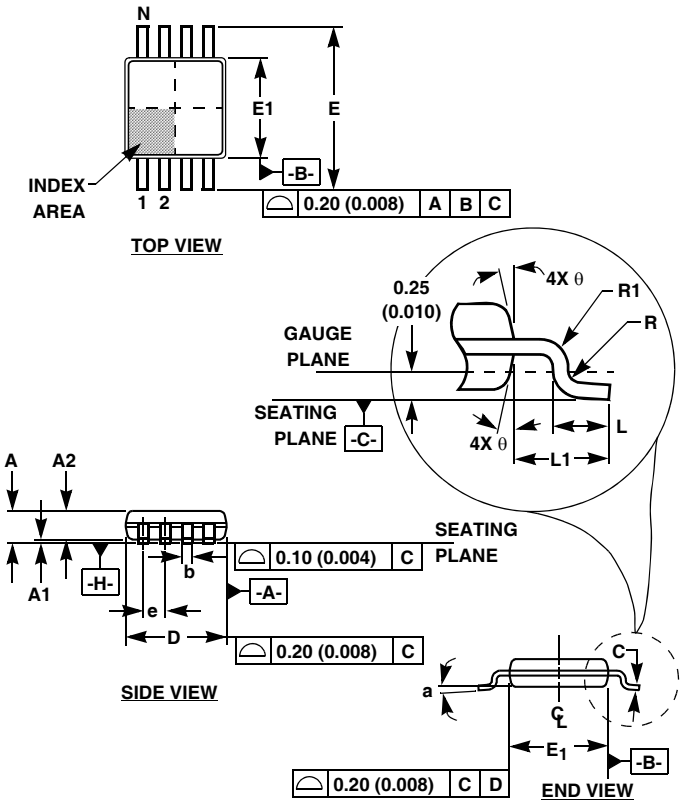
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Device Information

X9116

Printer Friendly Version

Digitally Controlled Potentiometer (XDCP™)

DS Datasheets, Related Docs & Simulations | Description | Key Features | PT Parametric Data | Related Devices

Ordering Information — RoHS/Pb-Free/Green Device

Part No.	Design-In Status	Temp.	Package	MSL	Price US $	
X9116WM8	Active	Comm	8 Ld MSOP	1	1.03	Buy
X9116WM8-2.7	Active	Comm	8 Ld MSOP	1	1.12	Buy
X9116WM8-2.7C7975	Active	Comm	8 Ld MSOP	1		Buy
X9116WM8-2.7T1	Active	Comm	8 Ld MSOP T+R	1	1.12	Buy
X9116WM8-2.7T1C7975	Active	Comm	8 Ld MSOP T+R	1		Buy
X9116WM8-2.7T2	Active	Comm	8 Ld MSOP T+R	3	1.12	Buy
X9116WM8I	Active	Ind	8 Ld MSOP	1	1.29	Buy
X9116WM8I-2.7	Active	Ind	8 Ld MSOP	1	1.41	Buy Sample
X9116WM8I-2.7T1	Active	Ind	8 Ld MSOP T+R	1	1.41	Buy
X9116WM8I-2.7T2	Active	Ind	8 Ld MSOP T+R	3	1.41	Buy
X9116WM8IT1	Active	Ind	8 Ld MSOP T+R	1	1.29	Buy
X9116WM8IZ	Active	Ind	8 Ld MSOP	2	1.29	Buy
X9116WM8IZ-2.7	Active	Ind	8 Ld MSOP	2	1.41	Buy
X9116WM8IZ-2.7T1	Active	Ind	8 Ld MSOP T+R	2	1.41	Buy
X9116WM8IZT1	Active	Ind	8 Ld MSOP T+R	2	1.29	Buy
X9116WM8T1	Active	Comm	8 Ld MSOP T+R	1	1.03	Buy
X9116WM8Z	Active	Comm	8 Ld MSOP	2	1.03	Buy
X9116WM8Z-2.7	Active	Comm	8 Ld MSOP	2	1.12	Buy
X9116WM8Z-2.7T1	Active	Comm	8 Ld MSOP T+R	2	1.12	Buy
X9116WM8ZT1	Active	Comm	8 Ld MSOP T+R	2	1.03	Buy
X9116WS8	Active	Comm	8 Ld SOIC	1	0.87	Buy
X9116WS8-2.7	Active	Comm	8 Ld SOIC	1	0.96	Buy
X9116WS8-2.7T1	Active	Comm	8 Ld SOIC T+R	1	0.96	Buy
X9116WS8I	Active	Ind	8 Ld SOIC	1	1.09	Buy
X9116WS8I-2.7	Active	Ind	8 Ld SOIC	1	1.20	Buy Sample
X9116WS8I-2.7T1	Active	Ind	8 Ld SOIC T+R	1	1.20	Buy
X9116WS8IT1	Active	Ind	8 Ld SOIC	1	1.09	Buy
X9116WS8IZ	Active	Ind	8 Ld SOIC	1	1.09	Buy
X9116WS8IZ-2.7	Active	Ind	8 Ld SOIC	1	1.20	Buy
X9116WS8IZ-2.7T1	Active	Ind	8 Ld SOIC T+R	1	1.20	Buy
X9116WS8IZT1	Active	Ind	8 Ld SOIC T+R	1	1.09	Buy
X9116WS8T1	Active	Comm	8 Ld SOIC T+R	1	0.87	Buy
X9116WS8T2	Active	Comm	8 Ld SOIC T+R	3	0.87	Buy

X9116WS8Z	Active	Comm	8 Ld SOIC	1	0.87 Buy
X9116WS8Z-2.7	Active	Comm	8 Ld SOIC	1	0.96 Buy
X9116WS8Z-2.7T1	Active	Comm	8 Ld SOIC T+R	1	0.96 Buy
X9116WS8ZT1	Active	Comm	8 Ld SOIC T+R	1	0.87 Buy
X9116WM8IZ-2.7T2	Coming Soon	Ind	8 Ld MSOP T+R	3	
X9116WM8Z-2.7T2	Coming Soon	Comm	8 Ld MSOP T+R	3	
X9116WS8ZT2	Coming Soon	Comm	8 Ld SOIC T+R	3	
X9116WST1	InActive	Comm	8 Ld SOIC T+R	1	0.87

The price listed is the manufacturer's suggested retail price for quantities between 100 and 999 units. However, prices in today's market are fluid and may change without notice.

MSL = Moisture Sensitivity Level - per IPC/JEDEC J-STD-020

SMD = Standard Microcircuit Drawing

Description

The Intersil X9116 is a digitally controlled nonvolatile potentiometer designed to be used in trimmer applications. The pot consists of 15 equal resistor segments that connect to the wiper pin through programmable CMOS switches. The tap position is programmed through a 3-wire up/down serial port. The last position of the wiper is stored in a nonvolatile memory location which is recalled at the time of power up of the device.

The wiper moves through sequential tap positions with inputs on the serial port. A falling edge on INC (bar) causes the tap position to increment one position up or down based on whether the U/D (bar) pin is held high or low.

The X9116 can be used in many applications requiring a variable resistance. In many cases it can replace a mechanical trimmer and offers many advantages such as temperature and time stability as well as the reliability of a solid state solution.

Key Features

- Solid-state nonvolatile
- 16 wiper taps
- 3-wire up/down serial interface
- V_{CC} = 2.7V and 5V
- Active current <50µA max.
- Standby current <1µA max.
- R_{TOTAL} = 10kΩ
- Packages: 8 Ld MSOP, 8 Ld SOIC
- Pb-free plus anneal available (RoHS compliant)

Related Documentation

AN Application Note(s):

- A Compendium of Application Circuits for Intersil's Digitally-Controlled (XDCP) Potentiometers
- A Primer on Digitally-Controlled Potentiometers
- Application of Intersil Digitally Controlled Potentiometers (XDCP™) as Hybrid Analog/Digital Feedback System Control Elements
- DC/DC Module Trim with Digital Potentiometers
- Designing Power Supplies Using Intersil's XDCP Mixed Signal Products
- Power Supply and DC to DC Converter Control using Intersil Digitally Controlled Potentiontiometers (XDCPs)
- Putting Analog On The Bus
- Shaft Encoder Drives Multiple Intersil Digitally Controlled Potentiontiometers (XDCPs)
- Tone, Balance, and Volume Control using a Quad XDCP
- Working with the Intersil 3-Wire DCP Devices

DS Datasheet(s):

- Digitally Controlled Potentiometer (XDCP™)

TB Technical Brief(s):

- Converting a Fixed PWM to an Adjustable PWM

EV Evaluation Board(s):

- Intersil_XDCP_Test_Utility_Manual_rev_3.2.3.pdf
- LabView_XDCP_Software.zip
- LabView_XDCP_Upgrade_3.2.3.zip
- Readme_XicorLabVIEW_V3.2.3.txt
- accessHW.zip

TH Technical Homepage:

- Digitally Controlled Potentiometers (DCPs) and Capacitors (DCCs)
- Precision Analog Homepage

PT **Parametric Data**

Number of DCPs	Single
Number of Taps	16
Memory Type	Non-Volatile
Bus Interface Type	3-Wire (Up/Down)
Resistance Options (kΩ)	10
V_{CC} Range (V)	2.7 to 5.5
DCP Differential Terminal Voltage (V)	0 to +5.5
Terminal Voltage Range V_L to V_H (V)	0 to V_{CC}
Resistance Taper	Linear
Wiper Current (mA)	±1
Wiper Resistance (Ω)	200
Standby Current I_{SB} (µA)	1