

### Description

The [SiT9365](#) is a differential MEMS XO supporting standard frequencies between 25 MHz and 325 MHz, and engineered for low-jitter applications. Utilizing SiTime's unique DualMEMS<sup>®</sup> temperature sensing and TurboCompensation<sup>®</sup> technology, the SiT9365 delivers exceptional dynamic performance by providing resistance to airflow, thermal gradients, shock and vibration. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT9365 can be factory programmed for specific combinations of frequency, stability, voltage, and output signaling. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Standard frequencies and programmability makes this device ideal for telecom, networking, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

### Features

- 32 standard frequencies from 25 MHz to 325 MHz (For additional frequencies, refer to [SiT9366](#) and [SiT9367](#) datasheets)
- LVPECL, Low-swing LVPECL, LVDS and HCSL output signaling
- 0.1 ps RMS phase jitter (random) for Ethernet applications
- Frequency stability as low as  $\pm 10$  ppm
- Wide temperature ranges from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$
- Industry-standard packages:  $3.2 \times 2.5 \text{ mm}^2$ ,  $7.0 \times 5.0 \text{ mm}^2$  and  $5.0 \times 3.2 \text{ mm}^2$  package

### Applications

- 10/40/100 Gbps Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers



### Block Diagram

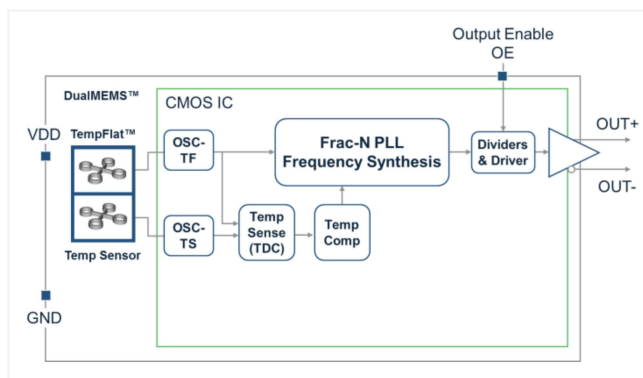


Figure 1. SiT9365 Block Diagram

### Package Pinout

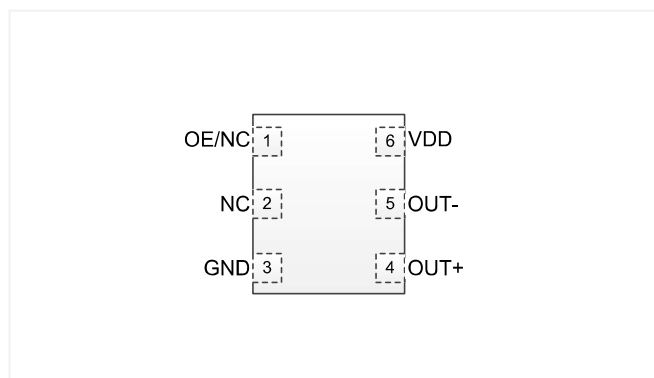
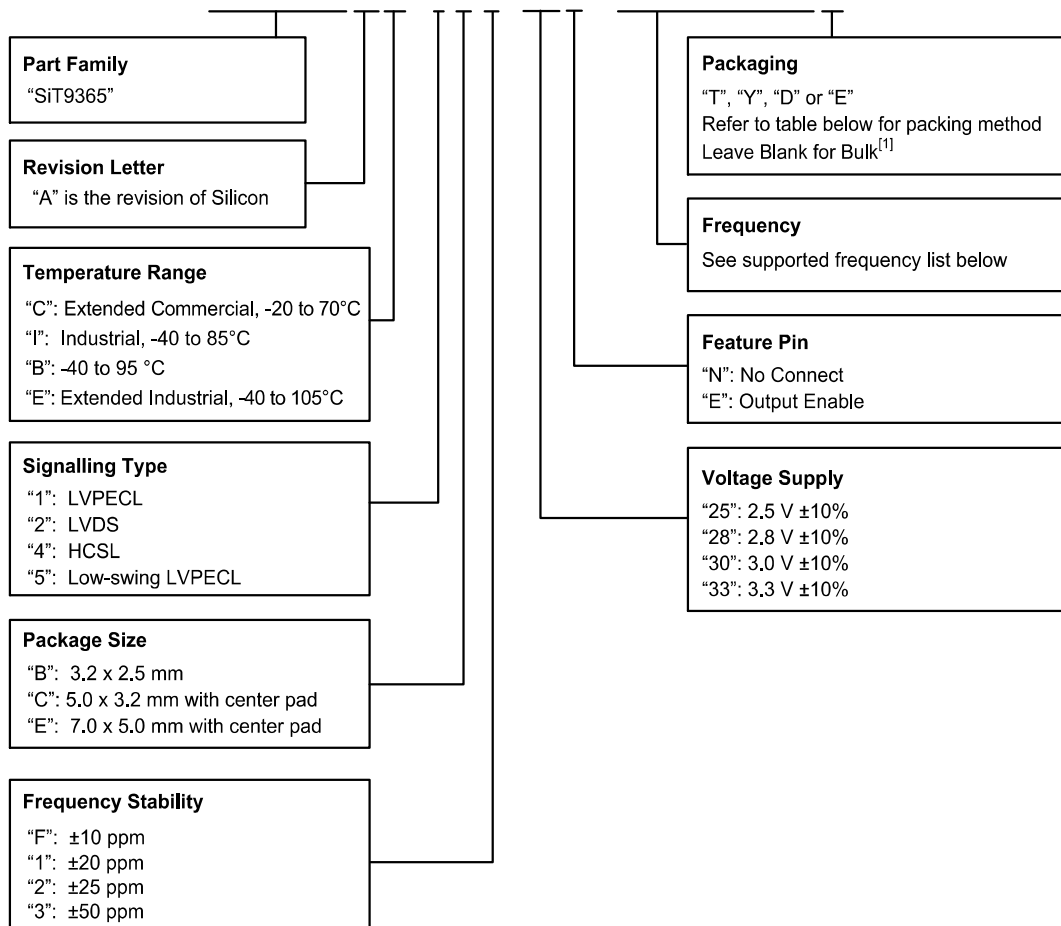


Figure 2. Pin Assignments (Top view)  
(Refer to [Table 7](#) for Pin Descriptions)

## Ordering Information

SiT9365AC-1B2-33E125.000000T



**Notes:**

1. Bulk is available for sampling only.

**Table 1. Supported Frequencies**

25.000000 MHz	30.720000 MHz	50.000000 MHz	53.125000 MHz	61.440000 MHz	62.500000 MHz	74.175824 MHz	74.250000 MHz
75.000000 MHz	77.760000 MHz	98.304000 MHz	100.000000 MHz	106.250000 MHz	122.880000 MHz	125.000000 MHz	133.333333 MHz
148.351648 MHz	150.000000 MHz	153.600000 MHz	155.520000 MHz	156.250000 MHz	159.375000 MHz	160.000000 MHz	161.132813 MHz
166.666666 MHz	168.040678 MHz	200.000000 MHz	212.500000 MHz	250.000000 MHz	300.000000 MHz	322.265625 MHz	325.000000 MHz

**Table 2. Ordering Codes for Supported Tape & Reel Packing Method**

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
5.0 x 3.2			T	Y		
3.2 x 2.5	D	E			—	—

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## Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

**Table 3. Electrical Characteristics – Common to LVPECL, Low-swing LVPECL, LVDS and HCSL (All temperature ranges)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	32 standard frequencies between 25 MHz and 325.000000 MHz			MHz	
<b>Frequency Stability</b>						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	-0.7	±0.4	+0.7	ppm	At 85°C
5 Year Aging	F_5y	-1.1	±0.7	+1.1	ppm	At 85°C
10 Year Aging	F_10y	-1.3	±0.8	+1.3	ppm	At 85°C
20 Year Aging	F_20y	-1.5	±1.0	+1.5	ppm	At 85°C
<b>Temperature Range</b>						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
		-40	–	+95	°C	
		-40	–	+105	°C	Extended Industrial
<b>Supply Voltage</b>						
Supply Voltage	Vdd	2.97	3.30	3.63	V	
		2.70	3.00	3.30	V	
		2.52	2.80	3.08	V	
		2.25	2.50	2.75	V	
<b>Input Characteristics</b>						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pin 1, OE logic high or logic low
<b>Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	
<b>Startup and OE Timing</b>						
Startup Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	μs	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See <a href="#">Figure 8</a> and <a href="#">Figure 9</a> .

**Table 4. Electrical Characteristics – LVPECL, Low-swing LVPECL**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
<b>Current Consumption</b>	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>OE Disable Supply Current</b>	I <sub>OE</sub>	–	–	58	mA	OE = Low
<b>Output Disable Leakage Current</b>	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Maximum Output Current</b>	I <sub>driver</sub>	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics for LVPECL</b>						
<b>Output High Voltage</b>	VOH	V <sub>dd</sub> -1.1	–	V <sub>dd</sub> -0.7	V	See <a href="#">Figure 4</a>
<b>Output Low Voltage</b>	VOL	V <sub>dd</sub> -1.9	–	V <sub>dd</sub> -1.5	V	See <a href="#">Figure 4</a>
<b>Output Differential Voltage Swing</b>	V <sub>Swing</sub>	1.2	1.6	2.0	V	See <a href="#">Figure 5</a>
<b>Rise/Fall Time</b>	Tr, Tf	–	225	290	ps	20% to 80%. See <a href="#">Figure 5</a>
<b>Output Characteristics for Low-swing LVPECL</b>						
<b>Output High Voltage</b>	VOH	V <sub>dd</sub> -1.2	–	V <sub>dd</sub> -0.75	V	See <a href="#">Figure 4</a>
<b>Output Low Voltage</b>	VOL	V <sub>dd</sub> -1.8	–	V <sub>dd</sub> -1.25	V	See <a href="#">Figure 4</a>
<b>Output Differential Voltage Swing</b>	V <sub>Swing</sub>	0.4	1	1.2	V	Output frequency less than or equal to 220 MHz, See <a href="#">Figure 5</a>
		0.4	1	1.6	V	Output frequency greater than 220 MHz, See <a href="#">Figure 5</a>
<b>Rise/Fall Time</b>	Tr, Tf	–	225	290	ps	20% to 80%. See <a href="#">Figure 5</a>
<b>Jitter – 7.0 x 5.0 mm Package</b>						
<b>RMS Period Jitter<sup>[2]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.
<b>Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm Packages</b>						
<b>RMS Period Jitter<sup>[2]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3V or 2.5V
<b>RMS Phase Jitter (random)</b>		–	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.

**Notes:**

2. Measured according to JESD65B.

**Table 5. Electrical Characteristics – LVDS**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
<b>Current Consumption</b>	I <sub>dd</sub>	–	–	79	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>OE Disable Supply Current</b>	I <sub>OE</sub>	–	–	58	mA	OE = Low
<b>Output Disable Leakage Current</b>	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Output Characteristics</b>						
<b>Differential Output Voltage</b>	V <sub>OD</sub>	300	–	450	mV	See <a href="#">Figure 6</a>
<b>Delta VOD</b>	ΔV <sub>OD</sub>	–	–	50	mV	See <a href="#">Figure 6</a>
<b>Offset Voltage</b>	V <sub>OS</sub>	1.125	–	1.375	V	See <a href="#">Figure 6</a>
<b>Delta VOS</b>	ΔV <sub>OS</sub>	–	–	50	mV	See <a href="#">Figure 6</a>
<b>Rise/Fall Time</b>	T <sub>r</sub> , T <sub>f</sub>	–	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See <a href="#">Figure 7</a>
<b>Jitter – 7.0 x 5.0 mm Package</b>						
<b>RMS Period Jitter<sup>[3]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.
<b>Jitter – 5.0 x 3.2 and 3.2 x 2.5 mm Packages</b>						
<b>RMS Period Jitter<sup>[1]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.

**Notes:**

3. Measured according to JESD65B.

**Table 6. Electrical Characteristics – HCSL**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
<b>Current Consumption</b>	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>OE Disable Supply Current</b>	I <sub>OE</sub>	–	–	58	mA	OE = Low
<b>Output Disable Leakage Current</b>	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Maximum Output Current</b>	I <sub>driver</sub>	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
<b>Output High Voltage</b>	VOH	0.60	–	0.90	V	See Figure 4
<b>Output Low Voltage</b>	VOL	-0.05	–	0.08	V	See Figure 4
<b>Output Differential Voltage Swing</b>	V <sub>Swing</sub>	1.2	1.4	1.80	V	See Figure 5
<b>Rise/Fall Time</b>	Tr, Tf	–	360	465	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 5
<b>Jitter – 7.0 x 5.0 mm Package</b>						
<b>RMS Period Jitter<sup>[4]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.
<b>Jitter – 5.0 x 3.2 and 3.2 x 2.5 mm Packages</b>						
<b>RMS Period Jitter<sup>[4]</sup></b>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>dd</sub> = 3.3 V or 2.5 V
<b>RMS Phase Jitter (random)</b>	T <sub>phj</sub>	–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dd</sub> levels, includes spurs. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V <sub>dd</sub> levels.

**Notes:**

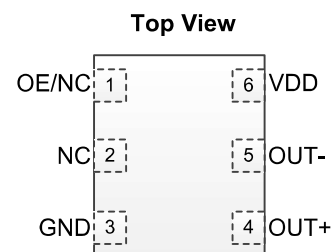
- 4. Measured according to JESD65B.

**Table 7. Pin Description**

Pin	Map	Functionality
1	OE/NC	Output Enable (OE) H <sup>[5]</sup> : specified frequency output L: output is high impedance
		Non Connect (NC) H or L or Open: No effect on output frequency or other device functions
2	NC	NA No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power VDD Power Supply Ground
4	OUT+	Output Oscillator output
5	OUT-	Output Complementary oscillator output
6 <sub>5</sub>	VDD	Power Power supply voltage <sup>[6]</sup>

**Notes:**

- 5. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- 6. A capacitor of value 0.1 μF or higher between VDD and GND is required. An additional 10 μF capacitor between VDD and GND is required for the best phase jitter performance.



**Figure 3. Pin Assignments**

**Table 8. Absolute Maximum Ratings**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

**Table 9. Thermal Considerations<sup>[7]</sup>**

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
<b>3225, 6-pin</b>	80	30
<b>5032, 6-pin</b>	53	20
<b>7050, 6-pin</b>	52	19

**Notes:**

7. Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

**Table 10. Maximum Operating Junction Temperature<sup>[8]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
95°C	120°C
105°C	130°C

**Notes:**

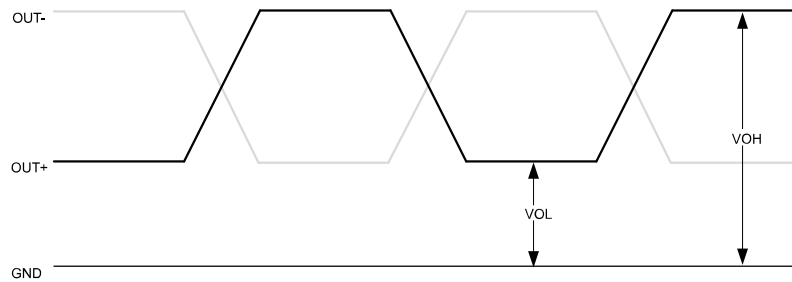
8. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

**Table 11. Environmental Compliance**

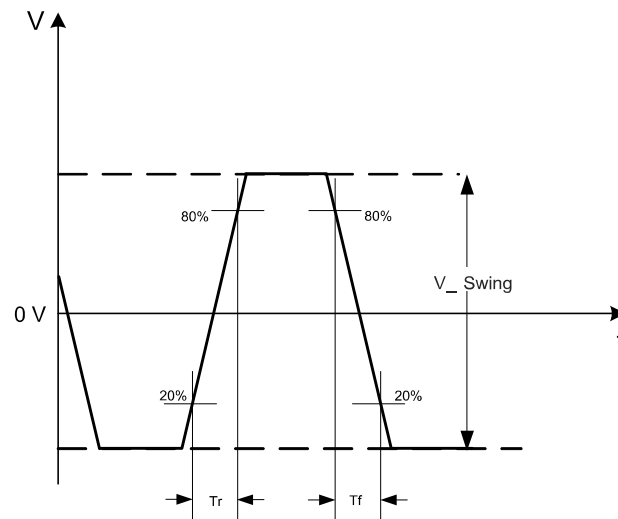
Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		



## Waveform Diagrams



**Figure 4. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)**



**Figure 5. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels Across Differential Pair (i.e. OUT+ minus OUT-)**

### Waveform Diagrams (continued)

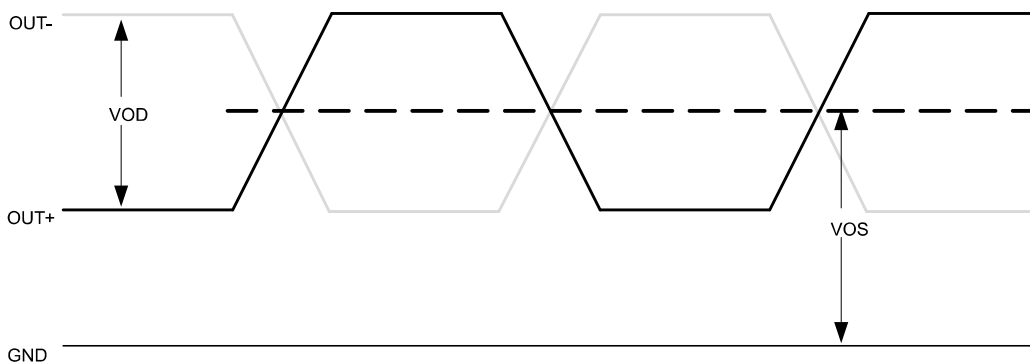


Figure 6. LVDS Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

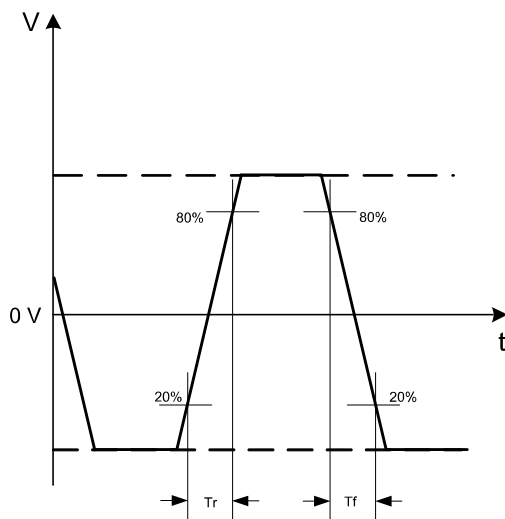


Figure 7. LVDS Differential Waveform (i.e. OUT+ minus OUT-)

### Timing Diagrams

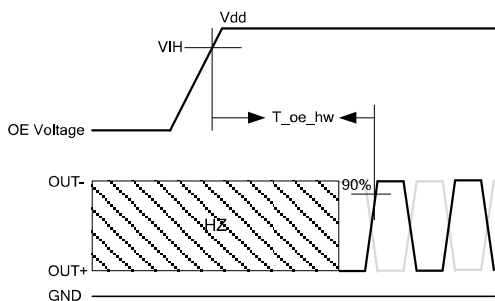


Figure 8. Hardware OE Enable Timing

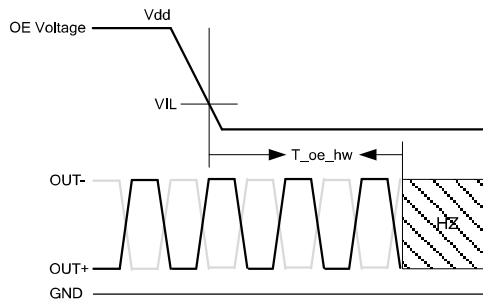


Figure 9. Hardware OE Disable Timing

## Termination Diagrams

### LVPECL and Low-swing LVPECL

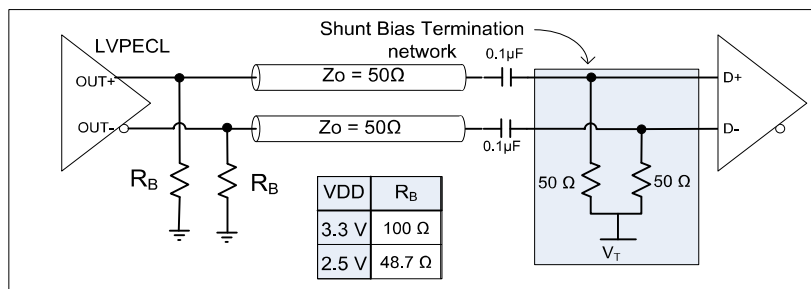


Figure 10. LVPECL and Low-swing LVPECL with AC-coupled Termination

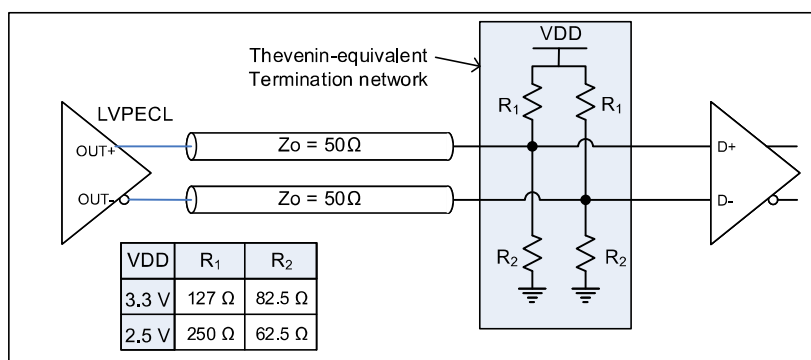


Figure 11. LVPECL and Low-swing LVPECL DC-coupled Load Termination with Thevenin Equivalent Network

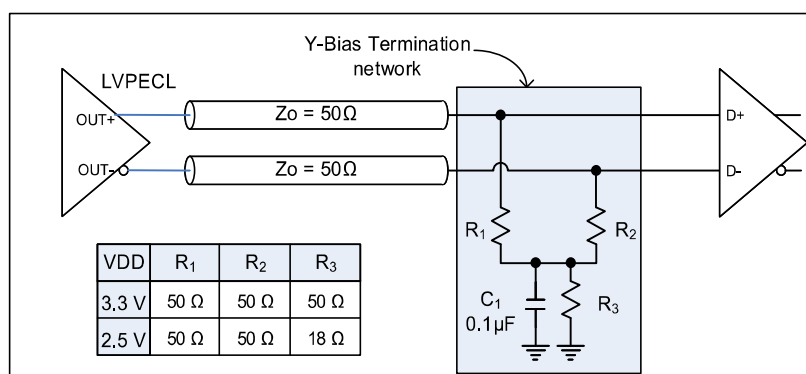


Figure 12. LVPECL and Low-swing LVPECL with Y-Bias Termination

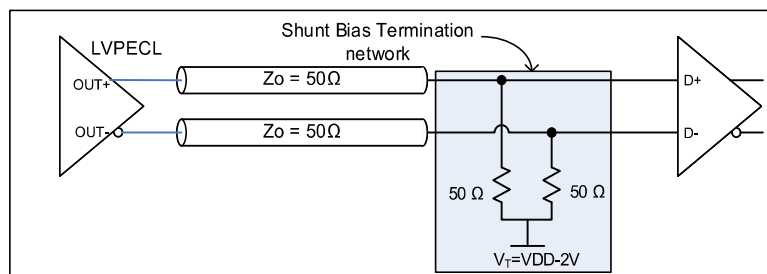
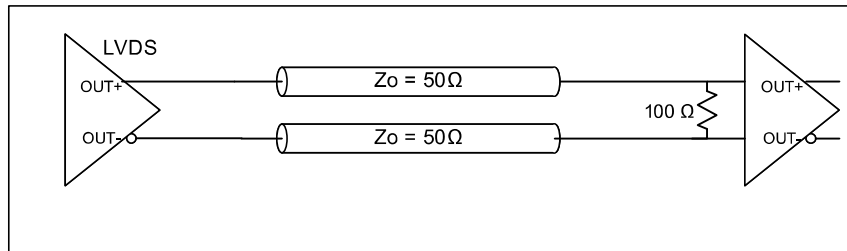


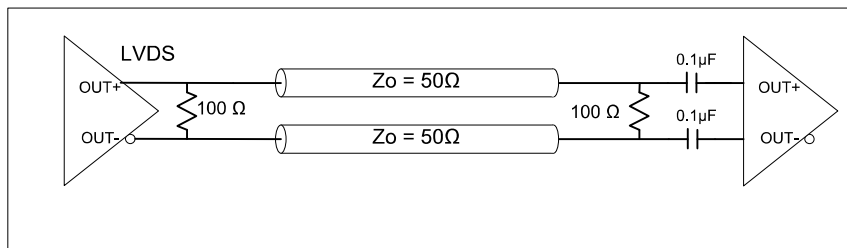
Figure 13. LVPECL and Low-swing LVPECL with DC-coupled Parallel Shunt Load Termination

## Termination Diagrams (continued)

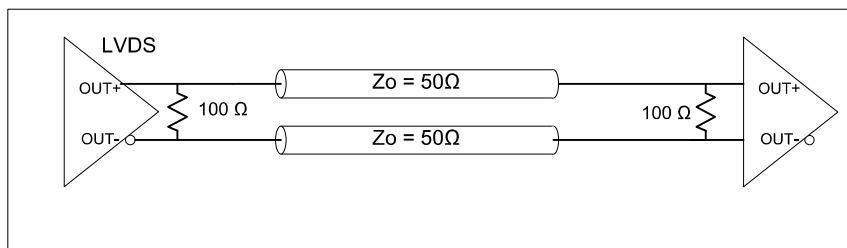
### LVDS



**Figure 14. LVDS Single DC Termination at the Load**

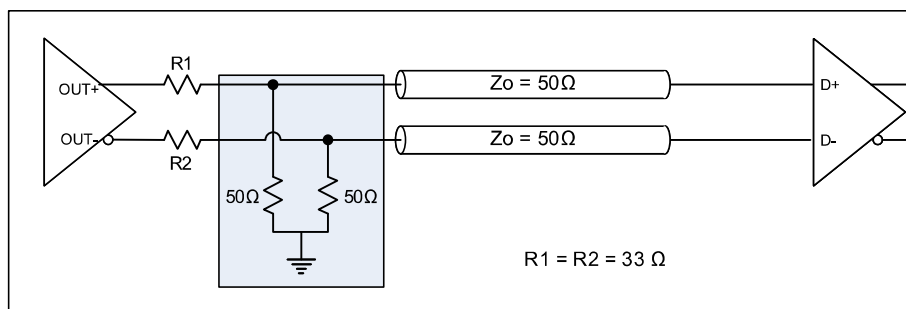


**Figure 15. LVDS double AC Termination with Capacitor Close to the Load**



**Figure 16. LVDS Double DC Termination**

### HCSL



**Figure 17. HCSL Interface Termination**

### Dimensions and Patterns — 3.2 x 2.5 mm<sup>2</sup>

Package Size – Dimensions (Unit: mm) <sup>[9]</sup>	Recommended Land Pattern (Unit: mm) <sup>[10]</sup>																																																																																	
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## Dimensions and Patterns — 7.0 x 5.0 mm<sup>2</sup>

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## Additional Information

**Table 12. Additional Information**

Document	Description	Download Link
<b>ECCN #: EAR99</b>	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
<b>HTS Classification Code: 8542.39.0000</b>	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
<b>Part number Generator</b>	Tool used to create the part number based on desired features.	<a href="https://www.sitime.com/part-number-generator">https://www.sitime.com/part-number-generator</a>
<b>Manufacturing Notes</b>	Tape & Reel dimension, reflow profile and other manufacturing related info	<a href="https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf">https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf</a>
<b>Qualification Reports</b>	RoHS report, reliability reports, composition reports	<a href="http://www.sitime.com/support/quality-and-reliability">http://www.sitime.com/support/quality-and-reliability</a>
<b>Performance Reports</b>	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	<a href="http://www.sitime.com/support/performance-measurement-report">http://www.sitime.com/support/performance-measurement-report</a>
<b>Termination Techniques</b>	Termination design recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
<b>Layout Techniques</b>	Layout recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
<b>Evaluation Boards</b>	SiT6085/6EB rev. 3.0, SiT6085EB rev.3.1 and SiT6097EB rev. 2.0 Evaluation Boards for Differential Oscillators User Manual	<a href="https://www.sitime.com/support/user-guides">https://www.sitime.com/support/user-guides</a>

## Revision History

**Table 13. Revision History**

Revision	Release Date	Change Summary
1.0	6-Sep-2017	Final release
1.04	17-Apr-2018	Added 5032 package Added -40 to 95°C and -40 to 105°C temperature ranges Corrected minor errors] Added Additional Information Table
1.05	3-Jul-2018	Performed minor edits and updated Ordering Information
1.06	25-Oct-2018	Removed "Contact SiTime" for $\pm 10$ ppm
1.07	30-Jul-2019	Updated package Dimensions Drawings Updated Table 9 Thermal Considerations for 5032 package Updated Table 3 specification for First Year Aging Added 5, 10, and 20 year aging specs Added Evaluation Boards SiT6085EB reference in Table 12 Rearranged layout, added Description, Block Diagram and TOC Tightened LVDS minimum VOD specification Added HTS code Added low-swing LVPECL package code and specifications
1.08	17-Aug-2019	Formatting changes
1.09	9-Mar-2021	Updated L1 and Dimple Width package dimensions for 3.2 x 2.5 mm package Updated trademarks, hyperlinks and changed rev table date format

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