

### 3MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

The CA5260A and CA5260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

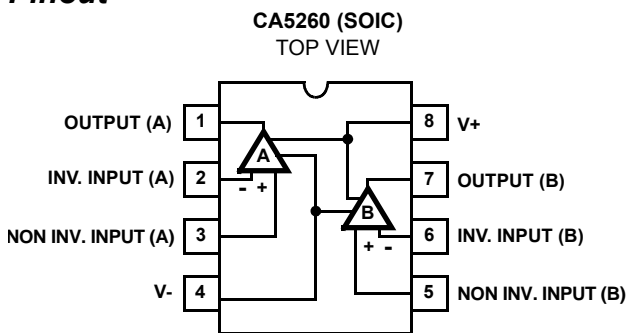
Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5260 Series circuits operate at supply voltages ranging from 4.5V to 16V, or  $\pm 2.25V$  to  $\pm 8V$  when using split supplies.

The CA5260, CA5260A have guaranteed specifications for 5V operation over the full military temperature range of  $-55^{\circ}C$  to  $125^{\circ}C$ .

#### Pinout



#### Features

- MOSFET Input Stage provides
  - Very High  $Z_i$  .....  $1.5T\Omega$  ( $1.5 \times 10^{12}\Omega$ ) (Typ)
  - Very Low  $I_i$  ..... 5pA (Typ) at 15V Operation  
2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5260A, CA5260 Have Full Military Temperature Range Guaranteed Specifications for  $V+ = 5V$
- CA5260A, CA5260 are Guaranteed to Operate Down to 4.5V for  $A_{OL}$
- Fully Guaranteed to Operate from  $-55^{\circ}C$  to  $125^{\circ}C$  at  $V+ = 5V, V- = GND$
- Pb-Free Plus Anneal Available (RoHS Compliant)

#### Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

#### Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE ( $^{\circ}C$ )	PACKAGE	PKG. DWG. #
CA5260AM96	5260A	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA5260M	5260	-55 to 125	8 Ld SOIC	M8.15
CA5260MZ (Note)	CA5260MZ	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
CA5260MZ96 (Note)	CA5260MZ	-55 to 125	8 Ld SOIC (Pb-free)	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# CA5260, CA5260A

## Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) . . . . . 16V  
 Differential Input Voltage . . . . . 8V  
 Input Voltage . . . . . (V+ +8V) to (V- -0.5V)  
 Input Current . . . . . 1mA  
 Output Short Circuit Duration (Note 1) . . . . . Indefinite

### Operating Conditions

Temperature Range . . . . . -55°C to 125°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

1. Short circuit may be applied to ground or to either supply.
2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Thermal Information

Thermal Resistance (Typical, Note 2)  $\theta_{JA}$  (°C/W)  
 SOIC Package . . . . . 157  
 Maximum Junction Temperature (Die) . . . . . 175°C  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (Lead Tips Only)

## Electrical Specifications

Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, T<sub>A</sub> = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA5260	CA5260A	
Input Resistance	R <sub>I</sub>		1.5	1.5	TΩ
Input Capacitance	C <sub>I</sub>	f = 1MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f <sub>T</sub>		3	3	MHz
Slew Rate	SR	V <sub>OUT</sub> = 2.5V <sub>P-P</sub>	5	5	V/μs
Transient Response	t <sub>r</sub>	C <sub>L</sub> = 25pF, R <sub>L</sub> = 2kΩ (Voltage Follower)	0.09	0.09	μs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, V <sub>IN</sub> = 4V <sub>P-P</sub> )	t <sub>S</sub>	C <sub>L</sub> = 25pF, R <sub>L</sub> = 2kΩ (Voltage Follower)	1.8	1.8	μs

## Electrical Specifications

T<sub>A</sub> = 25°C, V+ = 5V, V- = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V <sub>IO</sub>	V <sub>O</sub> = 2.5V	-	2	15	-	1.5	4	mV
Input Offset Current	I <sub>IO</sub>	V <sub>O</sub> = 2.5V	-	1	10	-	1	10	pA
Input Current	I <sub>I</sub>	V <sub>O</sub> = 2.5V	-	2	15	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V <sub>CM</sub> = 0 to 1V	70	85	-	80	85	-	dB
		V <sub>CM</sub> = 0 to 2.5V	50	55	-	50	55	-	dB
Common Mode Input Voltage Range	V <sub>ICR+</sub>		2.5	3	-	2.5	3	-	V
	V <sub>ICR-</sub>		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	84	-	75	84	-	dB
Large Signal Voltage Gain (Note 3)	A <sub>OL</sub>	R <sub>L</sub> = ∞, V <sub>O</sub> = 0.5 to 4V	105	111	-	107	113	-	dB
		R <sub>L</sub> = 10kΩ, V <sub>O</sub> = 0.5 to 3.6V	80	86	-	83	86	-	dB
Source Current	I <sub>SOURCE</sub>	V <sub>O</sub> = 0V	1.75	2.2	-	1.75	2.2	-	mA
Sink Current	I <sub>SINK</sub>	V <sub>O</sub> = 5V	1.70	2	-	1.70	2	-	mA

## CA5260, CA5260A

### Electrical Specifications $T_A = 25^\circ\text{C}$ , $V_+ = 5\text{V}$ , $V_- = 0\text{V}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$V_{OM+}$	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
	$V_{OM+}$	$R_L = 10\text{k}\Omega$	4.4	4.7	-	4.4	4.7	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
	$V_{OM+}$	$R_L = 2\text{k}\Omega$	3	3.4	-	3	3.4	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
Supply Current	$I_{SUPPLY}$	$V_O = 0\text{V}$	-	1.60	2.0	-	1.60	2.0	mA
		$V_O = 2.5\text{V}$	-	1.80	2.25	-	1.80	2.25	mA

NOTE:

3. For  $V_+ = 4.5\text{V}$  and  $V_- = \text{GND}$ ;  $V_{OUT} = 0.5\text{V}$  to  $3.2\text{V}$  at  $R_L = 10\text{k}\Omega$ .

### Electrical Specifications $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_+ = 5\text{V}$ , $V_- = 0\text{V}$

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{IO}$	$V_O = 2.5\text{V}$	-	3	20	-	2	15	mV
Input Offset Current	$I_{IO}$	$V_O = 2.5\text{V}$	-	1	10	-	1	10	nA
Input Current	$I_i$	$V_O = 2.5\text{V}$	-	2	15	-	2	15	nA
Common Mode Rejection Ratio	CMRR	$V_{CM} = 0$ to $1\text{V}$	60	78	-	65	78	-	dB
		$V_{CM} = 0$ to $2.5\text{V}$	50	60	-	50	60	-	dB
Common Mode Input Voltage Range	$V_{ICR+}$		2.5	3	-	2.5	3	-	V
	$V_{ICR-}$		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	$\Delta V_+ = 1\text{V}$ ; $\Delta V_- = 1\text{V}$	60	65	-	62	65	-	dB
Large Signal Voltage Gain (Note 4)	$A_{OL}$	$R_L = \infty$ , $V_O = 0.5$ to $4\text{V}$	70	78	-	70	78	-	dB
		$R_L = 10\text{k}\Omega$ , $V_O = 0.5$ to $3.6\text{V}$	60	65	-	60	65	-	dB
Source Current	$I_{SOURCE}$	$V_O = 0\text{V}$	1.3	1.6	-	1.3	1.6	-	mA
Sink Current	$I_{SINK}$	$V_O = 5\text{V}$	1.2	1.4	-	1.2	1.4	-	mA
Output Voltage	$V_{OM+}$	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
	$V_{OM+}$	$R_L = 10\text{k}\Omega$	4.2	4.4	-	4.2	4.4	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
	$V_{OM+}$	$R_L = 2\text{k}\Omega$	2.5	2.7	-	2.5	2.7	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
Supply Current	$I_{SUPPLY}$	$V_O = 0\text{V}$	-	1.65	2.2	-	1.65	2.2	mA
		$V_O = 2.5\text{V}$	-	1.95	2.35	-	1.95	2.35	mA

NOTE:

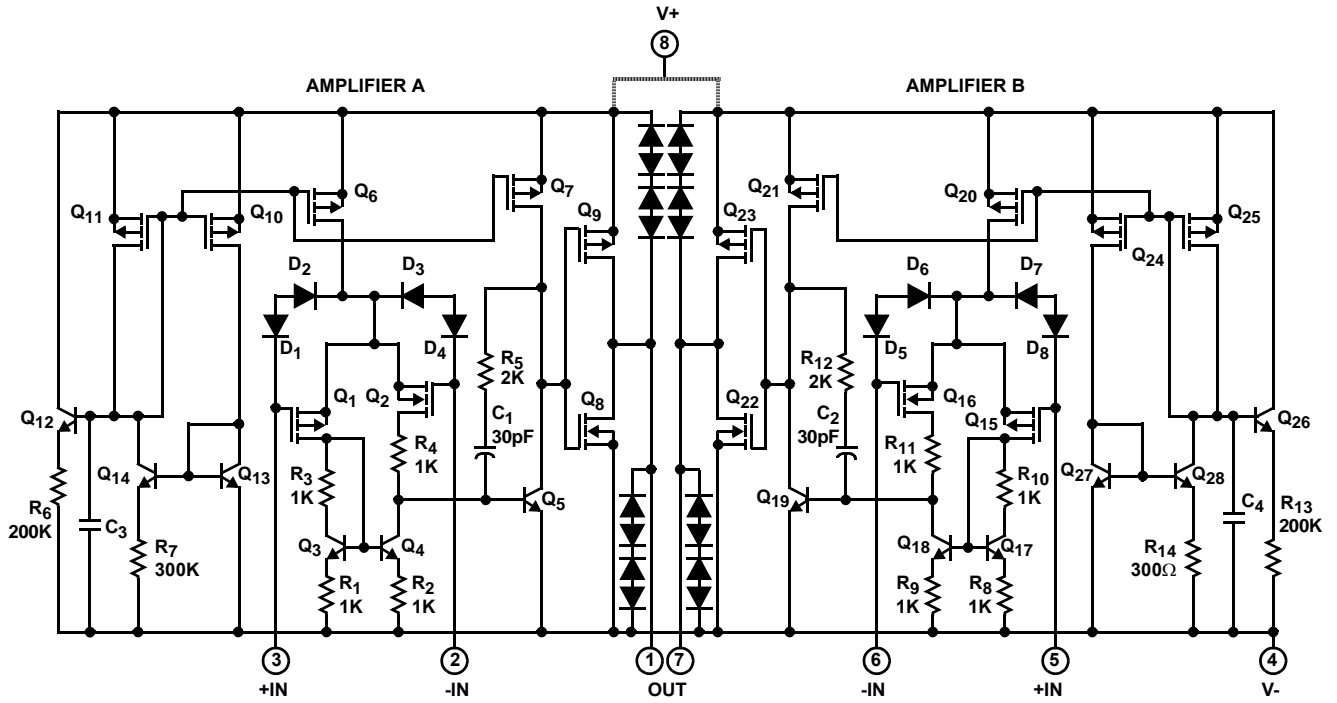
4. For  $V_+ = 4.5\text{V}$  and  $V_- = \text{GND}$ ;  $V_{OUT} = 0.5\text{V}$  to  $3.2\text{V}$  at  $R_L = 10\text{k}\Omega$ .

## CA5260, CA5260A

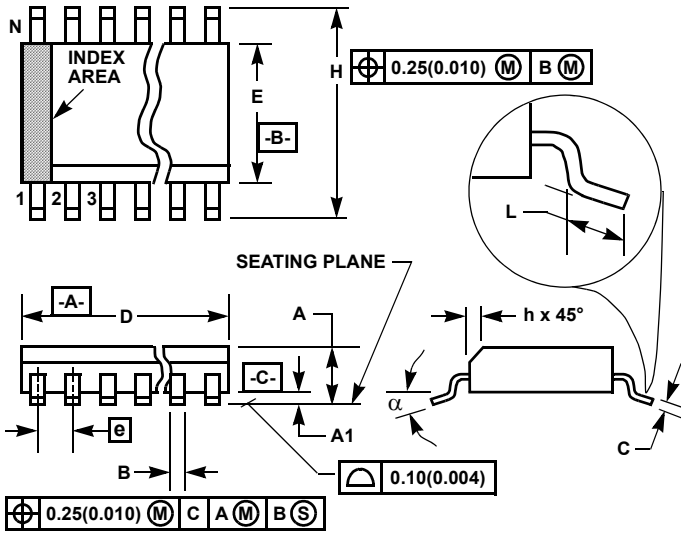
### Electrical Specifications Each Amplifier at $T_A = 25^\circ\text{C}$ , $V_+ = 15\text{V}$ , $V_- = 0\text{V}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{IO}$	$V_S = \pm 7.5$	-	6	15	-	2	5	mV
Input Offset Current	$I_{IO}$	$V_S = \pm 7.5$	-	0.5	30	-	0.5	20	pA
Input Current	$I_I$	$V_S = \pm 7.5$	-	5	50	-	5	30	pA
Large Signal Voltage Gain	$A_{OL}$	$V_O = 10V_{P-P}$ $R_L = 10k\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		70	90	-	80	95	-	dB
Common Mode Input Voltage Range	$V_{ICR}$		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio, $\Delta V_{IO} / \Delta V_{\pm}$	PSRR	$V_S = \pm 7.5$	-	32	320	-	32	150	$\mu\text{V/V}$
Maximum Output Voltage	$V_{OM+}$	$R_L = 10k\Omega$	11	13.3	-	11	13.3	-	V
	$V_{OM-}$		-	0.002	0.01	-	0.002	0.01	V
	$V_{OM+}$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM-}$		-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM+}$ (Source)	$V_O = 7.5\text{V}$	12	22	45	12	22	45	mA
	$I_{OM-}$ (Sink)		12	20	45	12	20	45	mA
Total Supply Current, $R_L = \infty$	I+	$V_O$ (Amp A) = 7.5V $V_O$ (Amp B) = 7.5V	-	9	16.5	-	9	16.5	mA
		$V_O$ (Amp A) = 0V $V_O$ (Amp B) = 0V	-	1.2	4	-	1.2	4	mA
		$V_O$ (Amp A) = 0V $V_O$ (Amp B) = 7.5V	-	5	9.5	-	5	9.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO} / \Delta T$		-	8	-	-	6	-	$\mu\text{V}/^\circ\text{C}$
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)  
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)