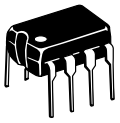
CAT64LC40

4 kb SPI Serial EEPROM

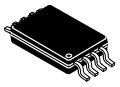
ON Semiconductor®

http://onsemi.com



PDIP−8
P, L SUFFIX
CASE 646AA

SOIC−8
J, W, S, V SUFFIX
CASE 751BD



TSSOP−8
U, Y SUFFIX
CASE 948AL

Description

The CAT64LC40 is a 4 kb Serial EEPROM which is configured as 256 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC40 is manufactured using ON Semiconductor's advanced CMOS EEPROM floating gate technology. It is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8−pin DIP, SOIC and TSSOP packages.

Features

- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5 V to 6.0 V Operation
- Self−Timed Write Cycle with Auto−Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Commercial, Industrial and Automotive Temperature Ranges
- Power−up Inadvertent Write Protection
- RDY/$\overline{\text{BSY}}$ Pin for End−of−Write Indication
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant*

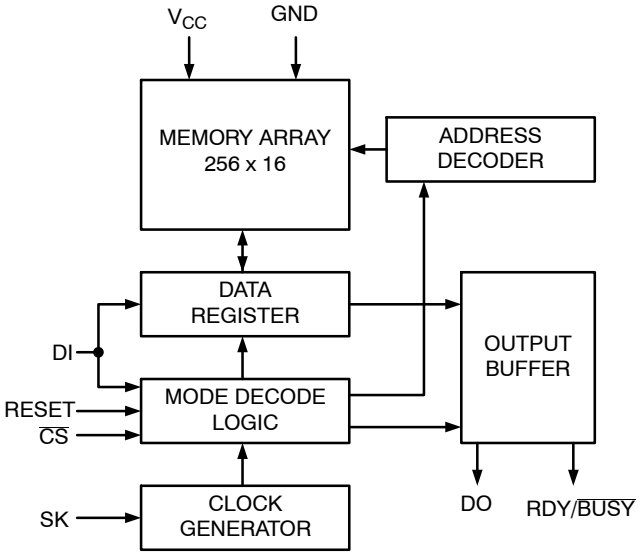


Figure 1. Block Diagram

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN FUNCTION

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.5 V to +6.0 V Power Supply
GND	Ground
RESET	Reset
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{BUSY}}$ Status

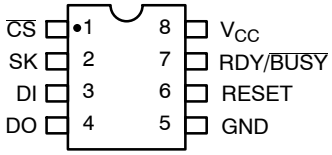
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

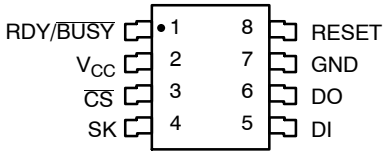
September, 2009 − Rev. 4

Publication Order Number:
CAT64LC40/D

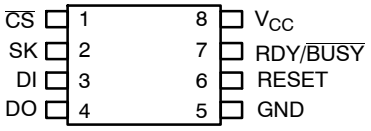
PIN CONNECTIONS



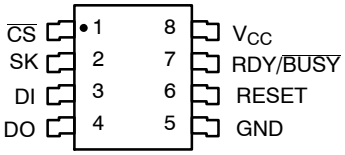
PDIP−8 (P, L)



SOIC−8 (J, W)



TSSOP−8 (U, Y)



SOIC−8 (S, V)

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Unit
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−2.0 to +V_{CC} +2.0	V
V_{CC} with Respect to Ground	−2.0 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 secs)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

Table 2. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
N_{END} (Note 3)	Endurance	1,000,000		Cycles/Byte
T_{DR} (Note 3)	Data Retention	100		Years
V_{ZAP} (Note 3)	ESD Susceptibility	2000		V
I_{LTH} (Notes 3 and 4)	Latch−Up	100		mA

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.

Table 3. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 6.0 V)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 5)	Input/Output Capacitance (DO, RDY/$\overline{BSY}$)	$V_{I/O}$ = 0 V	8	pF
C_{IN} (Note 5)	Input Capacitance ($\overline{CS}$, SK, DI, RESET)	V_{IN} = 0 V	6	pF

5. This parameter is tested initially and after a design or process change that affects the parameter.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, unless otherwise specified.)

Symbol	Parameter		Test Conditions	Limits			Units
				Min	Typ	Max	
I_{CC}	Operating Current	2.5 V	f_{SK} = 250 kHz			0.4	mA
	EWEN, EWDS, READ	6.0 V	f_{SK} = 1 MHz			1	mA
I_{CCP}	Program Current	2.5 V				2	mA
		6.0 V				3	mA
I_{SB} (Note 6)	Standby Current		V_{IN} = GND or V_{CC} $\overline{CS}$ = V_{CC}			3	μA
I_{LI}	Input Leakage Current		V_{IN} = GND to V_{CC}			2	μA
I_{LO}	Output Leakage Current		V_{OUT} = GND to V_{CC}			10	μA
V_{IL}	Low Level Input Voltage, DI			−0.1		V_{CC} x 0.3	V
V_{IH}	High Level Input Voltage, DI			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage, $\overline{CS}$, SK, RESET			−0.1		V_{CC} x 0.2	V
V_{IH}	High Level Input Voltage, $\overline{CS}$, SK, RESET			V_{CC} x 0.8		V_{CC} + 0.5	V
V_{OH} (Note 6)	High Level Output Voltage	2.5 V	I_{OH} = −10 μA	V_{CC} − 0.3			V
		6.0 V	I_{OH} = −10 μA	V_{CC} − 0.3			V
			I_{OH} = −400 μA	2.4			V
V_{OL} (Note 6)	Low Level Output Voltage	2.5 V	I_{OL} = 10 μA			0.4	V
		6.0 V	I_{OL} = 2.1 mA			0.4	V

6. V_{OH} and V_{OL} spec applies to READY/$\overline{BUSY}$ pin also.

Table 5. A.C. OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, unless otherwise specified.)

Symbol	Parameter		Limits			Units
			Min	Typ	Max	
t_{CSS}	$\overline{CS}$ Setup Time		100			ns
t_{CSH}	$\overline{CS}$ Hold Time		100			ns
t_{DIS}	DI Setup Time		200			ns
t_{DIH}	DI Hold Time		200			ns
t_{PD1}	Output Delay to 1				300	ns
t_{PD0}	Output Delay to 0				300	ns
t_{HZ} (Note 7)	Output Delay to High Impedance				500	ns
t_{CSMIN}	Minimum $\overline{CS}$ High Time		250			ns
t_{SKHI}	Minimum SK High Time	2.5 V	1000			ns
		4.5 V – 6.0 V	400			
t_{SKLOW}	Minimum SK Low Time	2.5 V	1000			ns
		4.5 V – 6.0 V	400			
t_{SV}	Output Delay to Status Valid				500	ns
f_{SK}	Maximum Clock Frequency	2.5 V	250			kHz
		4.5 V – 6.0 V	1000			
t_{RESS}	Reset to $\overline{CS}$ Setup Time		0			ns
t_{RESMIN}	Minimum RESET High Time		250			ns
t_{RESH}	RESET to READY Hold Time		0			ns
t_{RC}	Write Recovery		100			ns

7. This parameter is sampled but not 100% tested.

Table 6. POWER−UP TIMING (Notes 8 and 9)

Symbol	Parameter	Min	Max	Units
t_{PUR}	Power−Up to Read Operation		10	μs
t_{PUW}	Power−Up to Program Operation		1	ms

8. This parameter is tested initially and after a design or process change that affects the parameter.
9. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 7. WRITE CYCLE LIMITS

Symbol	Parameter		Min	Max	Units
t_{WR}	Program Cycle Time	2.5 V		10	ms
		4.5 V − 6.0 V		5	

Table 8. INSTRUCTION SET

Instruction	Opcode	Address	Data
Read	10101000	A7 A6 A5 A4 A3 A2 A1 A0	D15 − D0
Write	10100100	A7 A6 A5 A4 A3 A2 A1 A0	D15 − D0
Write Enable	10100011	X X X X X X X X	
Write Disable	10100000	X X X X X X X X	
[Write All Locations] (Note 10)	10100001	X X X X X X X X	D15 − D0

10. (Write All Locations) is a test mode operation and is therefore not included in the AC/DC Operations specifications.

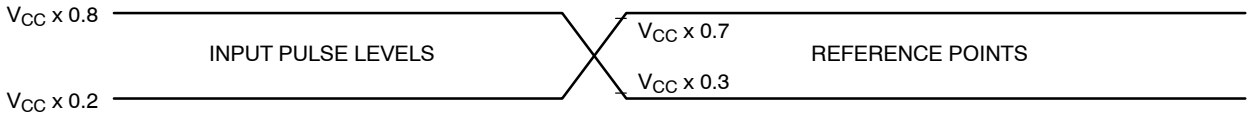


Figure 2. AC Testing Input/Output Waveform (Notes 11, 12 and 13) (C_L = 100 pF)

11. Input Rise and Fall Times (10% to 90%) < 10 ns.
12. Input Pulse Levels = V_{CC} x 0.2 and V_{CC} x 0.8.
13. Input and Output Timing Reference = V_{CC} x 0.3 and V_{CC} x 0.7.

Device Operation

The CAT64LC40 is a 4 kb nonvolatile memory intended for use with all standard controllers. The CAT64LC40 is organized in a 256 x 16 format. All instructions are based on an 8−bit format. There are four 16−bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC40 operates on a single power supply ranging from 2.5 V to 6.0 V and it has an on−chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{\text{BSY}}$ status when polled during a WRITE operation.

The format for all instructions sent to this device includes a 4−bit start sequence, 1010, a 4−bit op code and an 8−bit address field or dummy bits. For a WRITE operation, a 16−bit data field is also required following the 8−bit address field.

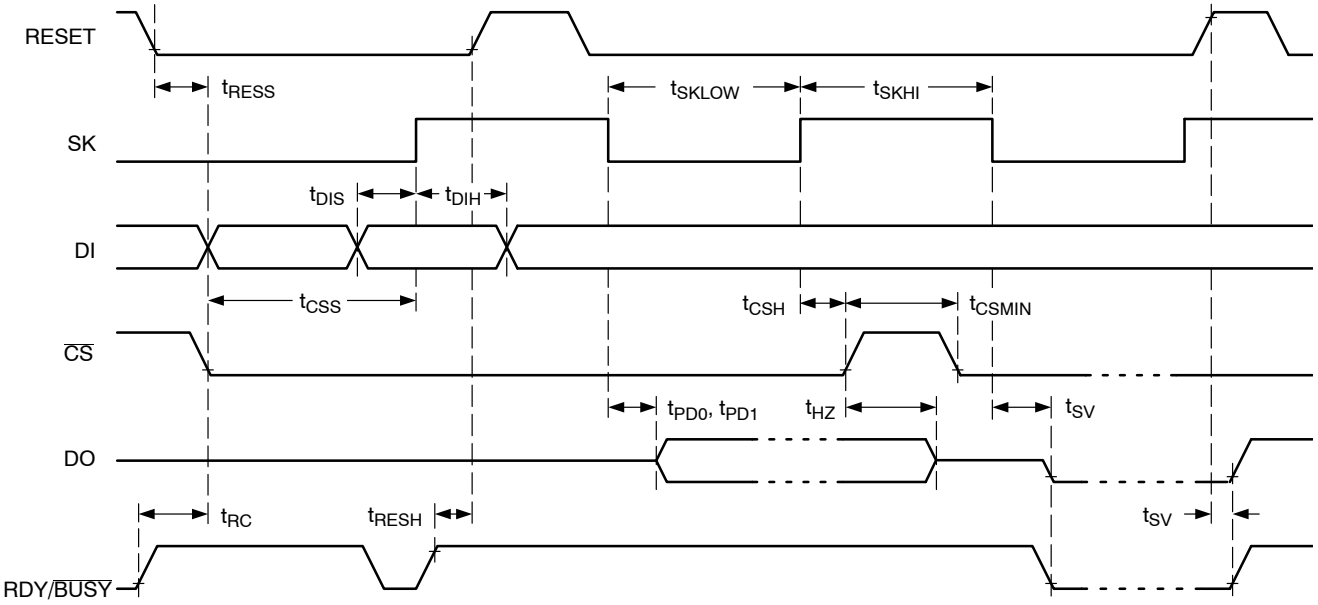


Figure 3. Synchronous Data Timing

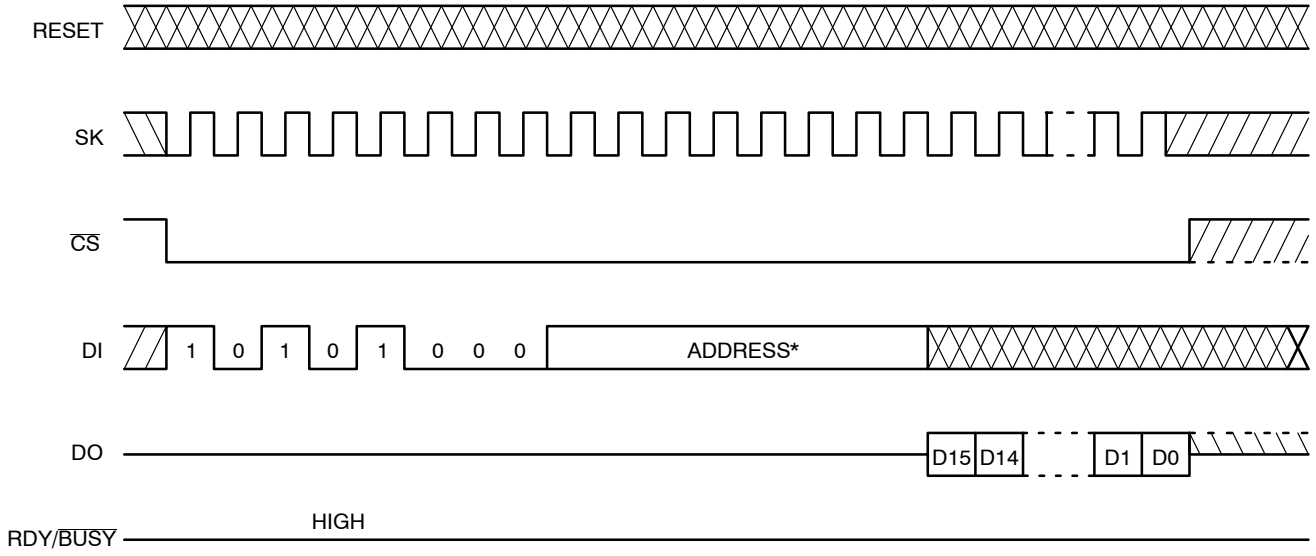


Figure 4. Read Instruction Timing

*Please check the instruction set table for address

The CAT64LC40 requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH−to−LOW transition of $\overline{CS}$ before the input of the 4−bit start sequence. Prior to the 4−bit start sequence (1010), the device will ignore inputs of all other logical sequence.

Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

After receiving a WRITE op code, address and data, the device goes into the AUTO−Clear cycle and then the WRITE cycle. The RDY/$\overline{BSY}$ pin will output the $\overline{BUSY}$ status (LOW) one t_{SV} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical “1” until the next WRITE cycle. The RDY/$\overline{BSY}$ output is not affected by the input of $\overline{CS}$.

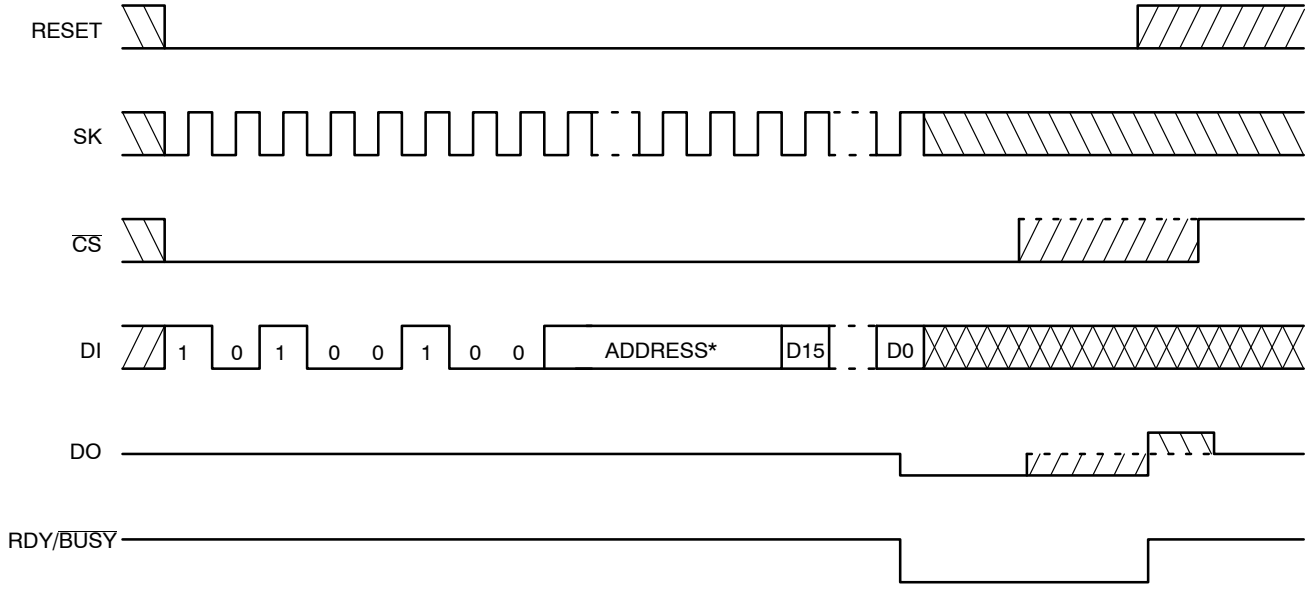


Figure 5. Write Instruction Timing

*Please check instruction set table for address.

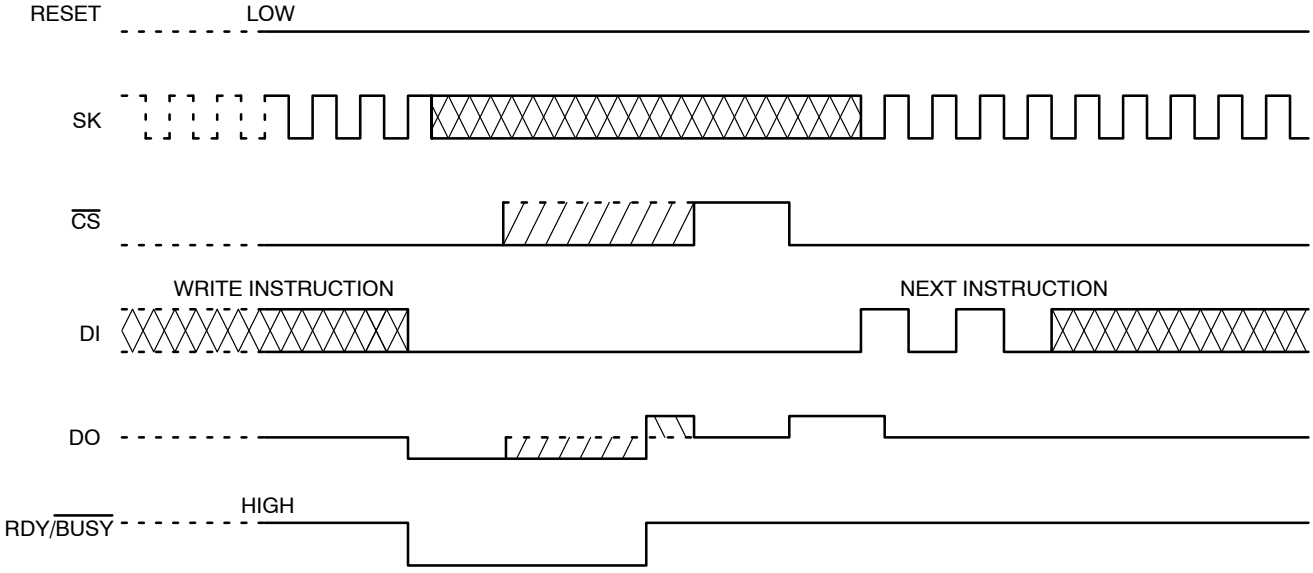


Figure 6. Ready/$\overline{BUSY}$ Status Instruction Timing

An alternative to get RDY/$\overline{BSY}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{CS}$ pin will cause the DO pin to output the RDY/$\overline{BSY}$ status. Bringing $\overline{CS}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a logical “1” when the device is deselected. The rising edge of the first “1” input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is $\overline{BUSY}$. If the reset occurs before the $\overline{BUSY}$ period, no writing will be initiated. However, if RESET occurs after the $\overline{BUSY}$ period, new data will have been written over the old data.

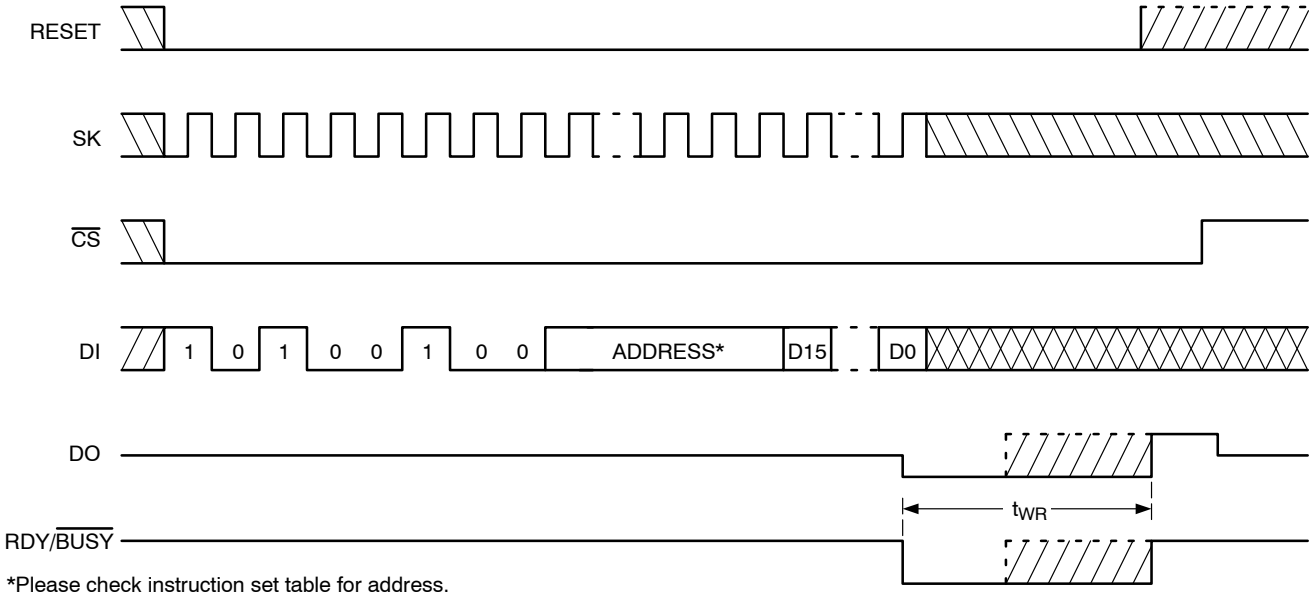


Figure 7. RESET During $\overline{BUSY}$ Instruction Timing

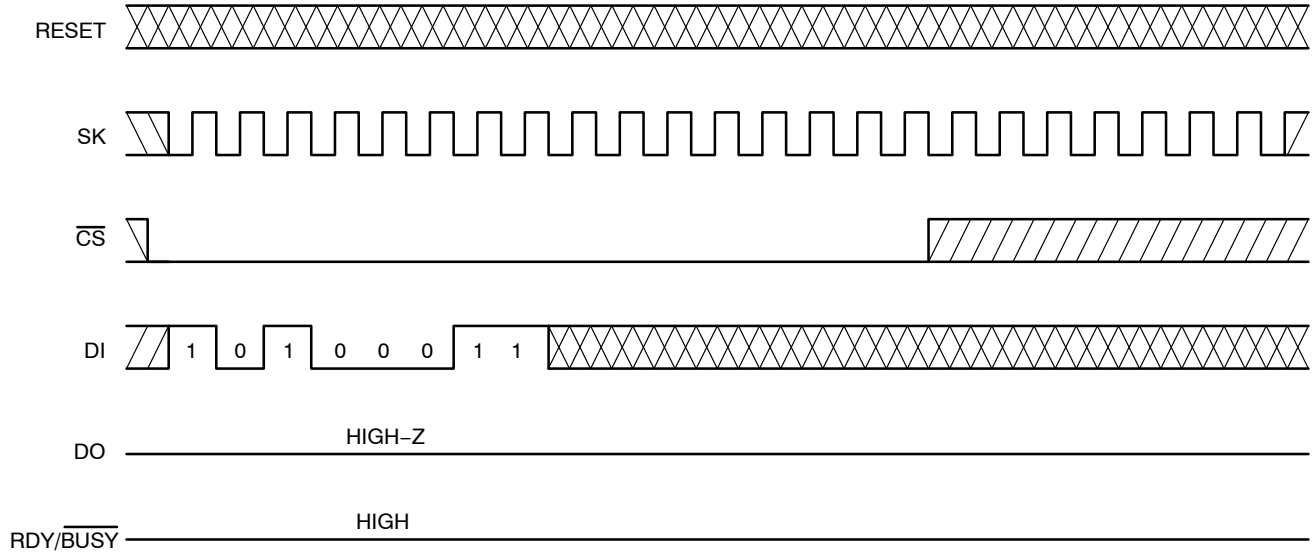


Figure 8. EWEN Instruction Timing

Reset

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High−Z condition.

When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{\text{BSY}}$ pin and on the DO pin if $\overline{\text{CS}}$ is low.

The RESET input affects only the WRITE and WRITEALL operations. It does not reset any other operations such as READ, EWEN and EWDS.

Erase/Write Enable and Disable

The CAT64LC40 powers up in the erase/write disabled state. After power−up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power−down has occurred. The EWDS is used to prevent any inadvertent over−writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

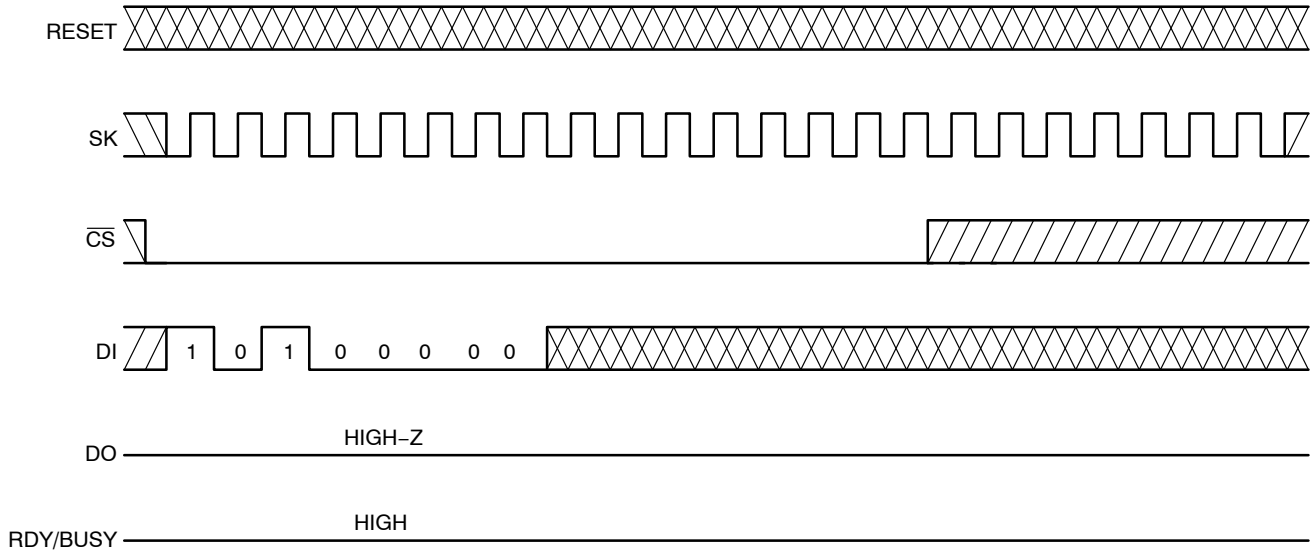
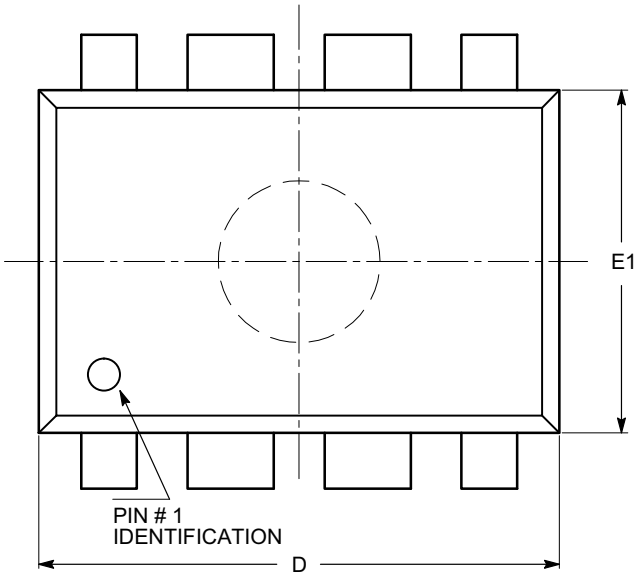


Figure 9. EWDS Instruction Timing

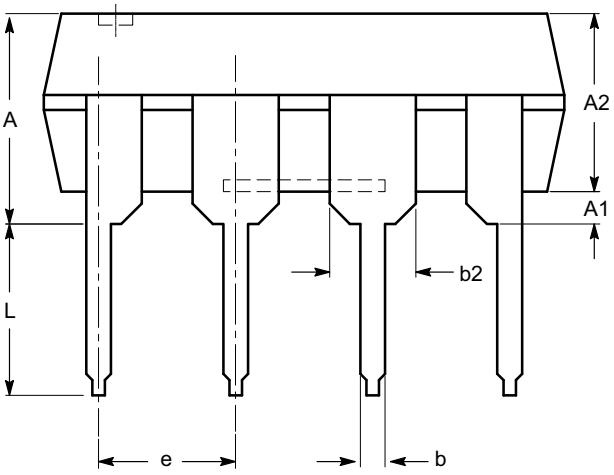
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

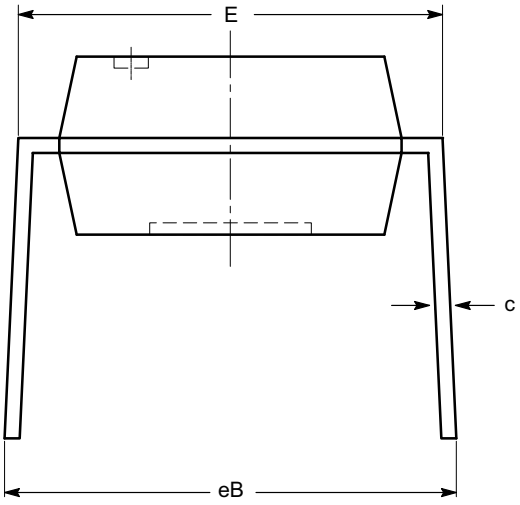


SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80

TOP VIEW



SIDE VIEW

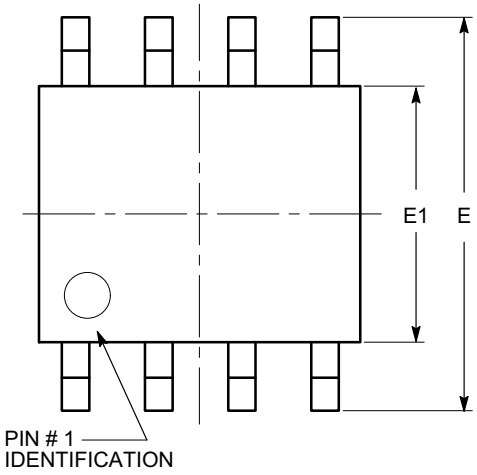


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

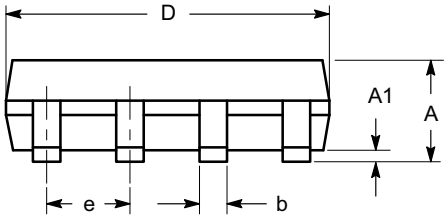
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

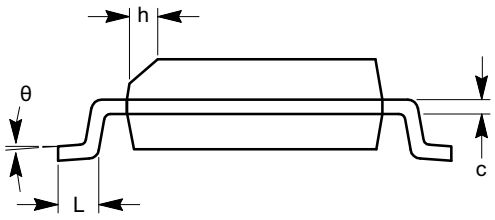


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

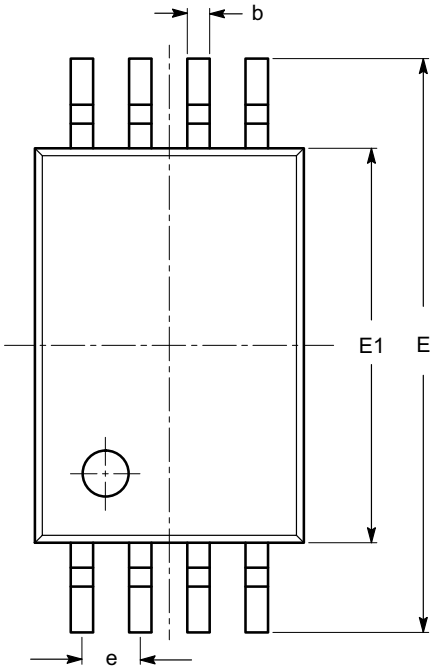


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

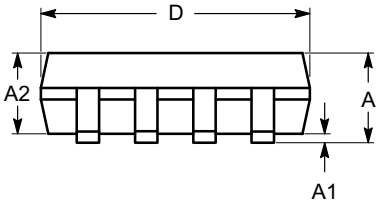
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

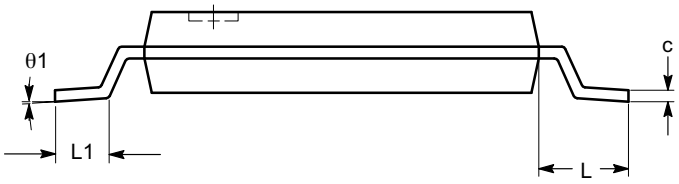


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



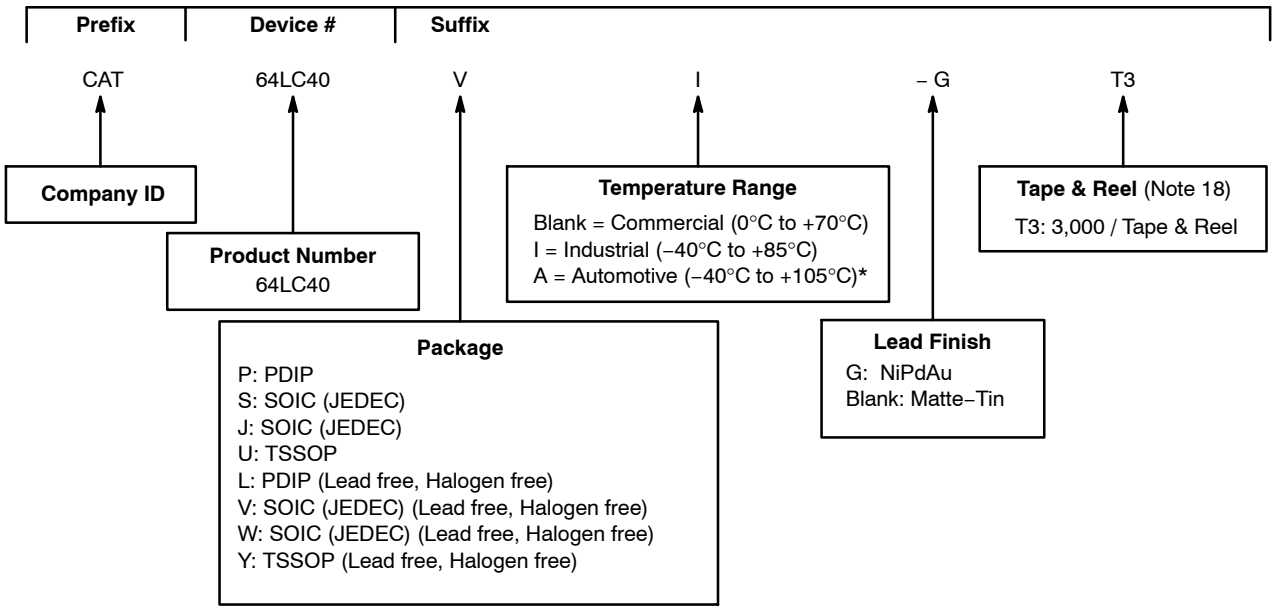
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information



*–40°C to +125°C is available upon request.

ORDERING INFORMATION

Orderable Part Number (for Pb–Free Devices)
CAT64LC40LI–GT3
CAT64LC40VI–GT3
CAT64LC40WI–GT3
CAT64LC40YI–GT3

14. All packages are RoHS–compliant (Lead–free, Halogen–free).
15. The standard lead finish is NiPdAu.
16. The device used in the above example is a 64LC40VI–GT3 (SOIC, Industrial Temperature, Tape & Reel).
17. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
18. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
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