

# SN74ALVC16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS267A – MARCH 1993 – REVISED MAY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## description

This 20-bit flip-flop is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation; it is tested at 2.5-V, 2.7-V, and 3.3-V  $V_{CC}$ .

The SN74ALVC16721's 20 flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable ( $\overline{CLKEN}$ ) input is low. If  $\overline{CLKEN}$  is high, no data is stored.

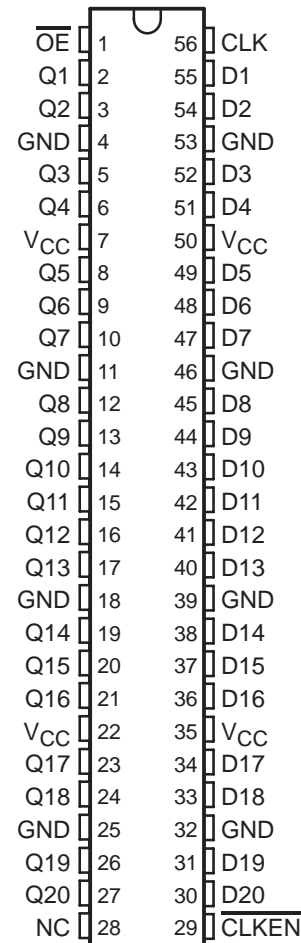
A buffered output-enable ( $\overline{OE}$ ) input places the 20 outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The SN74ALVC16721 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16721 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## DGG OR DL PACKAGE (TOP VIEW)



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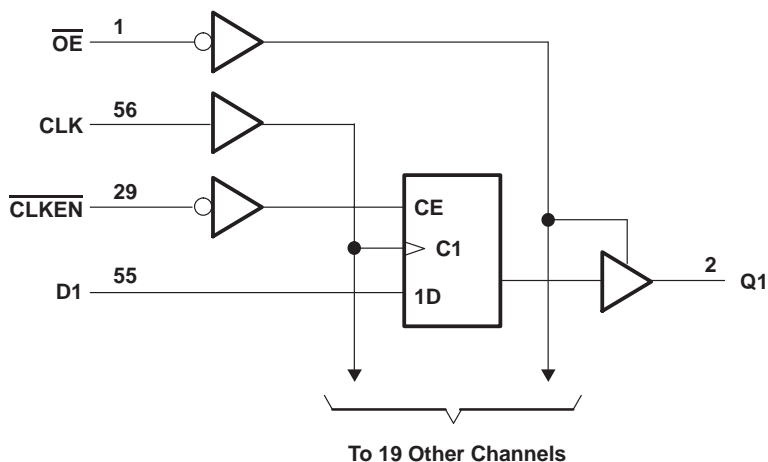
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**FUNCTION TABLE**  
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	Q
L	H	X	X	$Q_0$
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	$Q_0$
H	X	X	X	Z

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.



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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3\text{ V}$	-12	mA
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.3\text{ V}$	12	mA
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 4: Unused or floating control pins must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> †	T <sub>A</sub> = -40°C to 85°C			UNIT
			MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V	2.3 V	2			
	I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
	I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V	2.7 V	2.2			
	I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -24 mA, V <sub>IH</sub> = 2 V	3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V	2.3 V	0.4			
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.7 V	2.3 V	0.7			
	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V	2.3 V	45			μA
	V <sub>I</sub> = 1.7 V		-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V		-75			
	V <sub>I</sub> = 0 to 3.6 V	3.6 V	±500			
I <sub>OZ</sub> ‡	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			μA
ΔI <sub>CC</sub>	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		750			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5			pF
C <sub>io</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input-leakage current.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

				V <sub>CC</sub> = 3.3 V ± 0.15 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low			3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time	Data before CLK↑	High or low	4		3.6		3.1		ns
		$\overline{\text{CLKEN}}$ before CLK↑	High or low	3.4		3.1		2.7		
t <sub>h</sub>	Hold time	Data after CLK↑	High or low	0		0		0		ns
		$\overline{\text{CLKEN}}$ after CLK↑	High or low	0		0		0		

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			150		150		150		MHz
t <sub>pd</sub>	CLK	Q	1	7	1	5.7	1	4.9	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Q	1	7.4	1	6.5	1	5.4	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Q	1	6.2	1	5.1	1	4.8	ns

operating characteristics, T<sub>A</sub> = 25°C

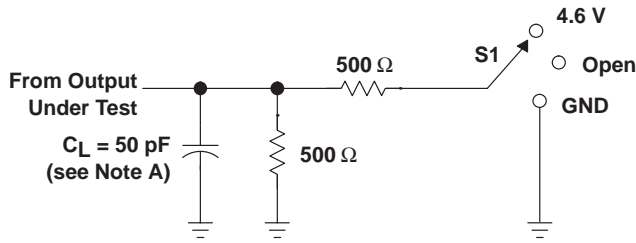
PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	55	59	pF
		Outputs disabled		46	49	



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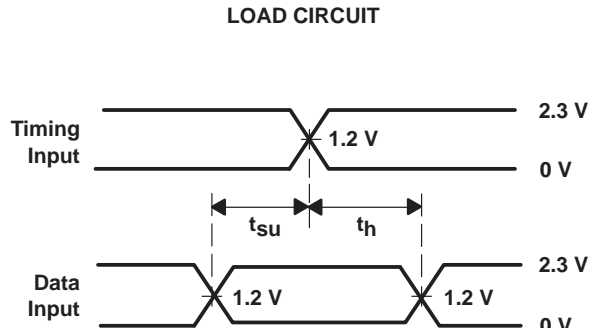
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**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

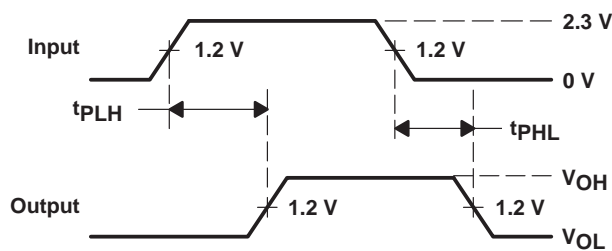


TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND

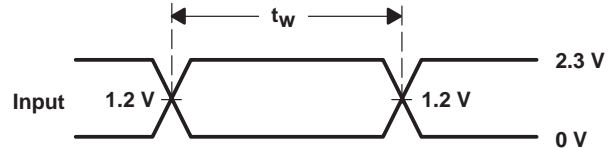
**LOAD CIRCUIT**



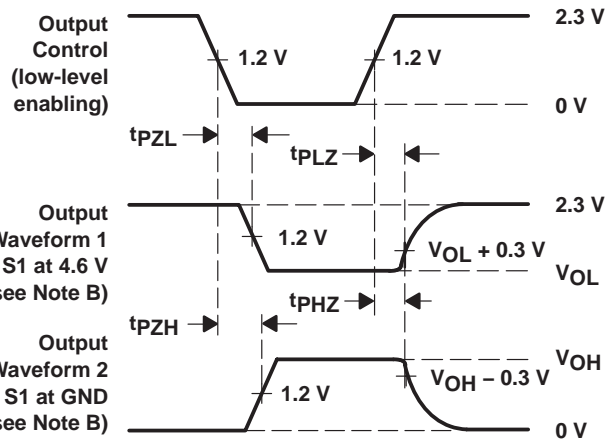
**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS PULSE DURATION**



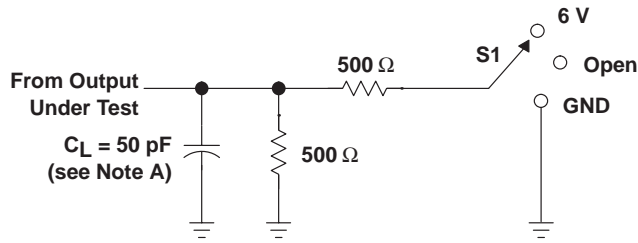
**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

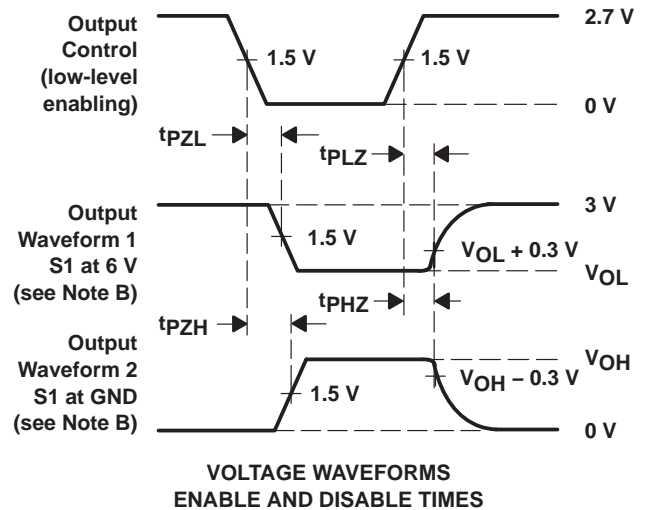
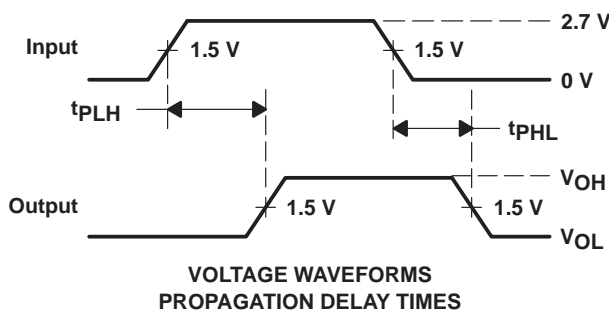
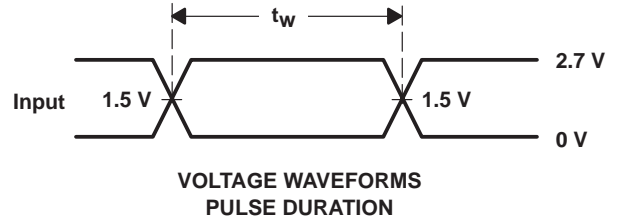
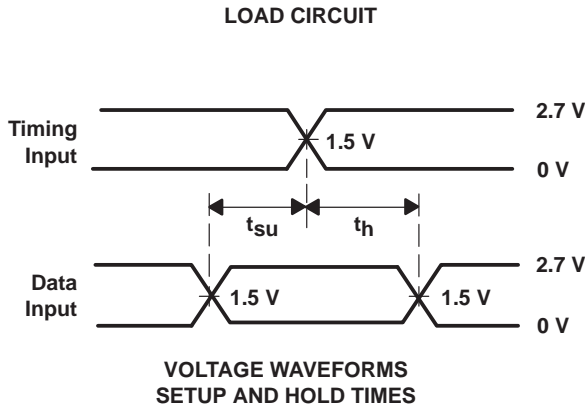


PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

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