QUALITY SEMICONDUCTOR, INC.

QuickSwitch® Products
Last Value Latch
20 Active Bus Terminators
(Bus Hold)

FEATURES/BENEFITS

- Active termination pulls bus pins to rails
- Holds last value of input signal
- Ideal replacement for resistive termination
- Ultra low 3µA DC quiescent current
- Available in 24-pin QSOP
- Bus-hold eliminates floating bus lines and reduces static power consumption
- Low power QCMOS technology
- Operates over 2.7 to 5.5V V_{CC} range
- TTL-compatible input and output levels
- No added noise or ground bounce
- 20 independent terminator circuits

APPLICATIONS

- Bus termination
- Extend data hold time

DESCRIPTION

The QS3389 provides a set of 20 active termination circuits which pull data bus signals to the voltage rails. This feature prevents bus signals from floating in the threshold region of standard TTL I/O devices. The QS3389 can replace resistor termination solutions which add DC power dissipation and increase component count. Input clamp diodes help to reduce reflections and undershoot in transmission line environments. Importantly, the terminator circuits pull signals to whichever logic state the signal previously held (HIGH or LOW). For this reason, this device is also referred to as a last value latch. This device is appropriate for data bus applications where interfacing devices have CMOS inputs with low input currents. These terminators provide sufficient drive to overcome leakage currents and drive corresponding signals away from the TTL threshold region.

Figure 1. Functional Block Diagram

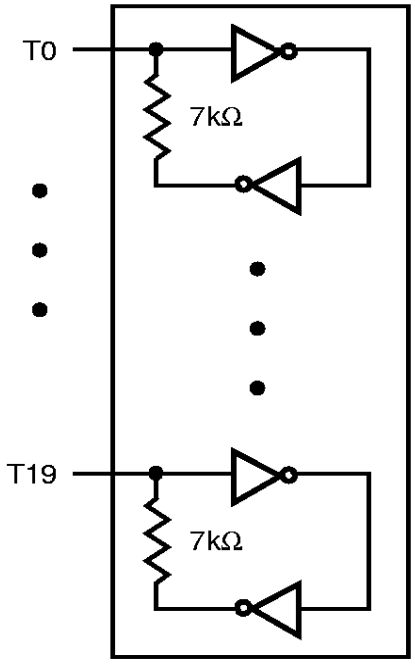

Table 1. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	QSOP Typ	QSOP Max
T19-T0	3	4

Note: Capacitance is characterized but not tested. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

Figure 2. Pin Configuration (All Pins Top View)

SOIC, QSOP

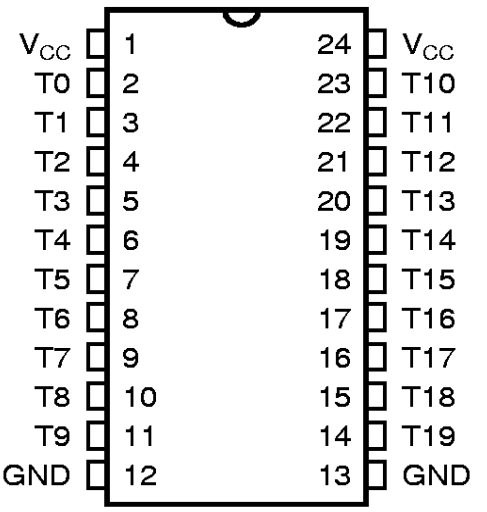

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage V_S	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATING are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated rating may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 3. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	1.5	mA

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.

Table 4. DC Electrical Characteristics Over Operating Range

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage			2.0	—	—	V
V_{IL}	Input LOW Voltage			—	—	0.8	V
V_T	Threshold Voltage			—	1.5	—	V
$\|I_{IN}\|$	Input Leakage Current(2)	V_{IN} = V_{CC} or GND		—	—	5	µA
$\|I_{BH}\|$	Input Current(5) Input High or Low	V_{CC} = Max., V_{IN} = 0V or V_{IN} = V_{CC}		—	—	20	µA
	Bus Hold Inputs(2,3)	V_{CC} = Max., 0.8V < V_{IN} < 2.0V		—	—	500(4)	µA
I_{BHH}	Bus Hold Sustaining(6,7) Current	V_{CC} = Min.	V_{IN} = 2.0V	–60	—	—	µA
I_{BHL}	Bus Hold Inputs		V_{IN} = 0.8V	+60	—	—	µA
R_T	Terminator Resistance			—	7k	—	Ω

Notes:

1. Typical values are measured at V_{CC} = 5.0V and T_A = 25°C.
2. Trip Current Definition (see Figure 1 and discussion):
   An external driver must source at least I_{TL} to switch the node from LOW to HIGH.
   An external driver must sink at least I_{TH} to switch the node from HIGH to LOW.
3. Hold Current Definition (see Figure 1 and discussion):
   I_{HH} is the Maximum Current the QS3389 can sink without raising the node above V_{IL} max.
   I_{HL} is the Maximum Current the QS3389 can source without lowering the node below V_{IH} min.
4. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus-hold input will change states.
5. $|I_{BH}|$ - Magnitude of the input current specified under two conditions:
   (a) Input voltage at GND or V_{CC}. This indicates the input current under steady-state conditions.
   (b) Input voltage between 0.8V and 2.0V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the Bus-hold circuit.
6. I_{BHL} - Minimum sustaining 'sink' current at the input for V_{IN} = 0.8V.
   This parameter signifies the latching capability of the Bus-hold circuit in logic LOW state.
7. I_{BHH} - Minimum sustaining 'source' current at the input for V_{IN} = 2.0V.
   This parameter signifies the latching capability of the Bus-hold circuit in log HIGH state.

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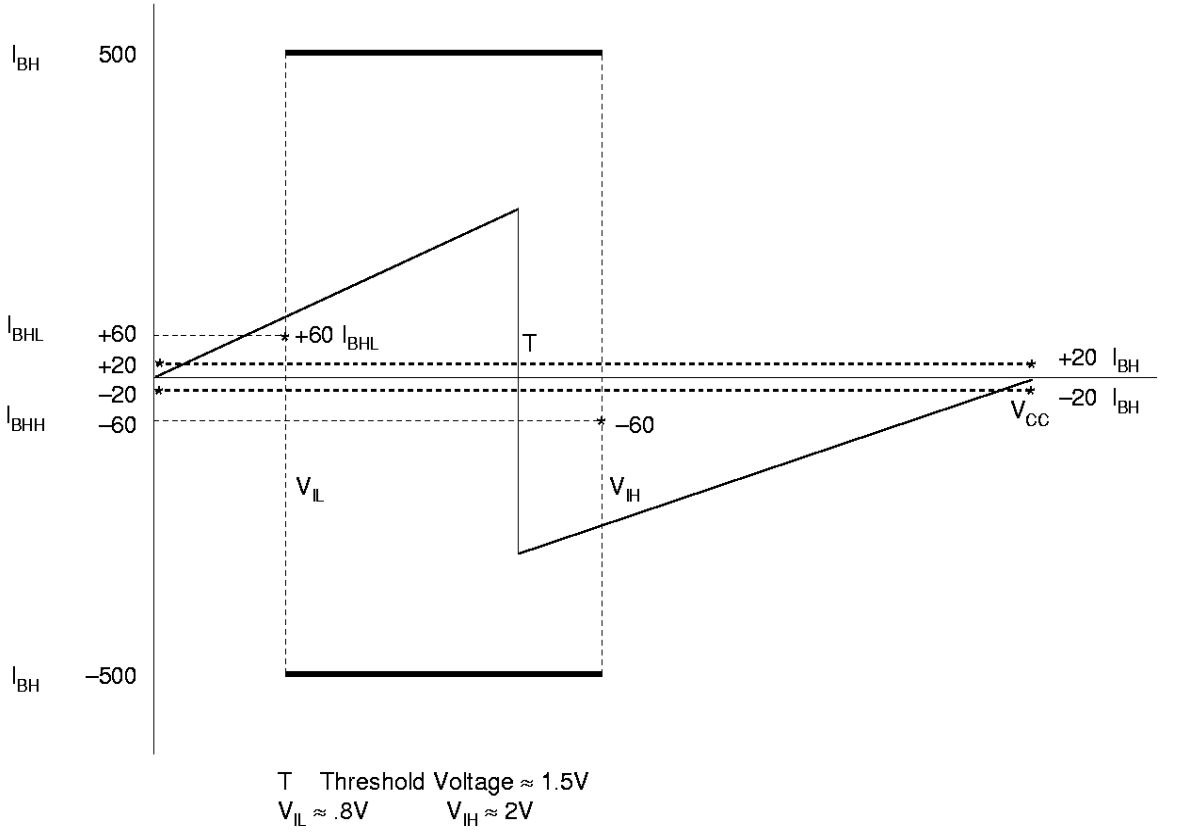

Figure 2: Trip and Hold Current Characteristics of the Last Valve Latch

Active Terminator or 'Bus-hold' Circuit

The Active Terminator circuit, also known as the Bus-hold circuit, is configured as a 'weak latch' with positive feedback. When connected to a TTL or CMOS input port, the Bus-hold circuit holds the last logic state at the input when the input is 'disconnected' from the driver. When the output of a device connected to such an input attempts a logic level transition, it will overdrive the Bus-hold circuit. The primary benefit of a Bus-hold circuit is that it prevents CMOS inputs from floating, a situation which should be avoided to prevent spurious switching of inputs and unnecessary power dissipation. Bus-hold is a better solution than the traditional approach of using resistive termination to V_{CC} or GND to prevent bus floating, because the Bus-hold circuit does not consume any static power.

Figure 2. shows the input V-I characteristics of a typical Bus-hold implementation. The input characteristics resemble a resistor. As the input voltage is increased from 0 Volts, the input 'sink' current increases linearly. When the TTL threshold of the circuit is reached (typically 1.5 Volts), the latch changes the logic state due to positive feedback and the direction of current is reversed. As the input voltage is further increased towards V_{CC}, the input 'source' current begins to decrease, reaching the lowest level at $V_{IN} = V_{CC}$.