SN74ALS819, SN74ALS29818
8-BIT DIAGNOSTICS/PIPELINE REGISTERS

D2298, JANUARY 1986—REVISED OCTOBER 1986

- High-Speed 8-Bit Parallel Pipeline Register
- Serial Shadow Register with Right-Shift Only
- 'ALS29818 Performs Parallel-to-Serial and Serial-to-Parallel Conversion
- Designed Specifically for Use in Applications Such As:
  - Write Control Store ('ALS29818)
  - Serial Shadow-Register Diagnostics
- 'ALS819 Provides Even-Parity Output
- Low Power Dissipation . . . 215 mW Typical
- 'ALS29818 is Functionally Equivalent to AMD AM29818
- Package Options Include Plastic "Small Outline" Packages, Standard Plastic DIPs, and Plastic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

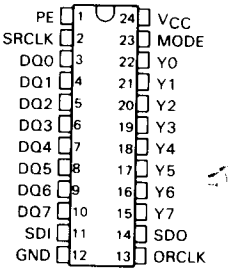
description

The 'ALS819 and 'ALS29818 are 8-bit pipeline registers each with an on-chip shadow register. They are for use in applications such as write control store and shadow register diagnostics.

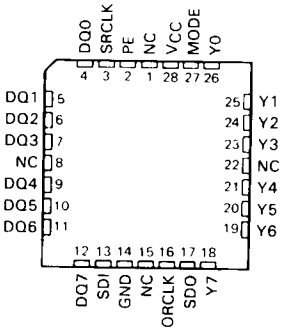
The output registers of the 'ALS819 and 'ALS29818 are loaded in parallel from either the I/O port (DQ0—DQ7) or the shadow register. The shadow register of the 'ALS29818 can be loaded serially or from either the I/O port (Y0—Y7) or the pipeline register. The 'ALS819 shadow register can be loaded serially or from the I/O port (DQ0—DQ7). In addition, the 'ALS819 provides a Parity-Even (PE) output, which monitors parity of the output register. Operation of these devices is controlled by the Mode and SDI inputs as shown in the function table.

The SN74ALS819 and SN74ALS29818 are characterized for operation from 0°C to 70°C.

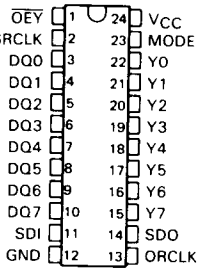
SN74ALS819 . . . DW OR JT PACKAGE
(TOP VIEW)



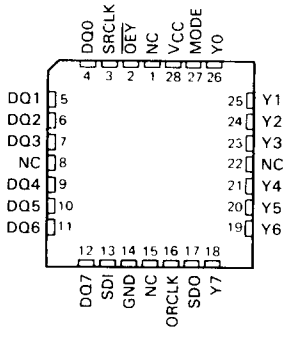
SN74ALS819 . . . FN PACKAGE
(TOP VIEW)



SN74ALS29818 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS29818 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

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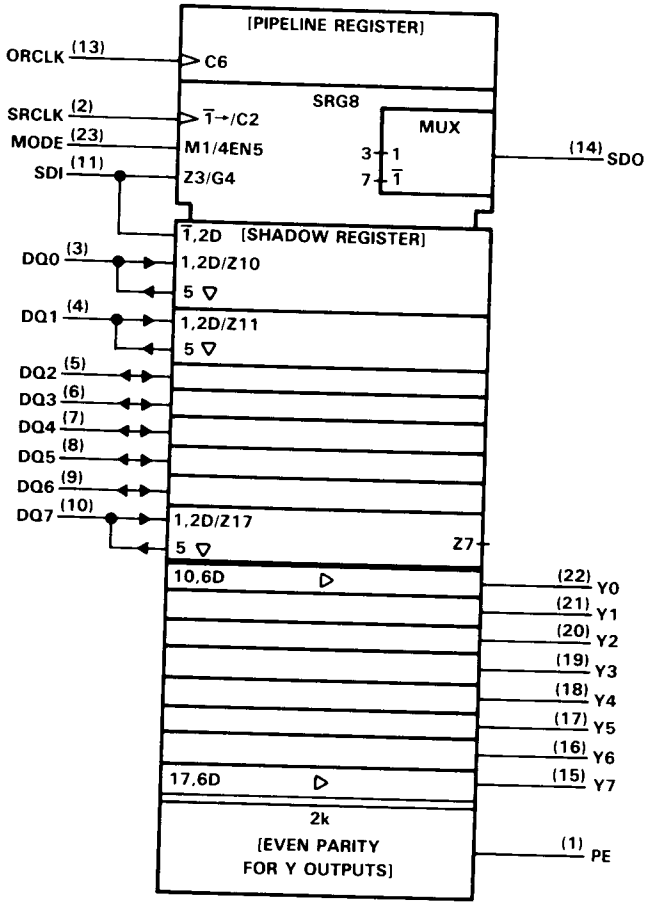
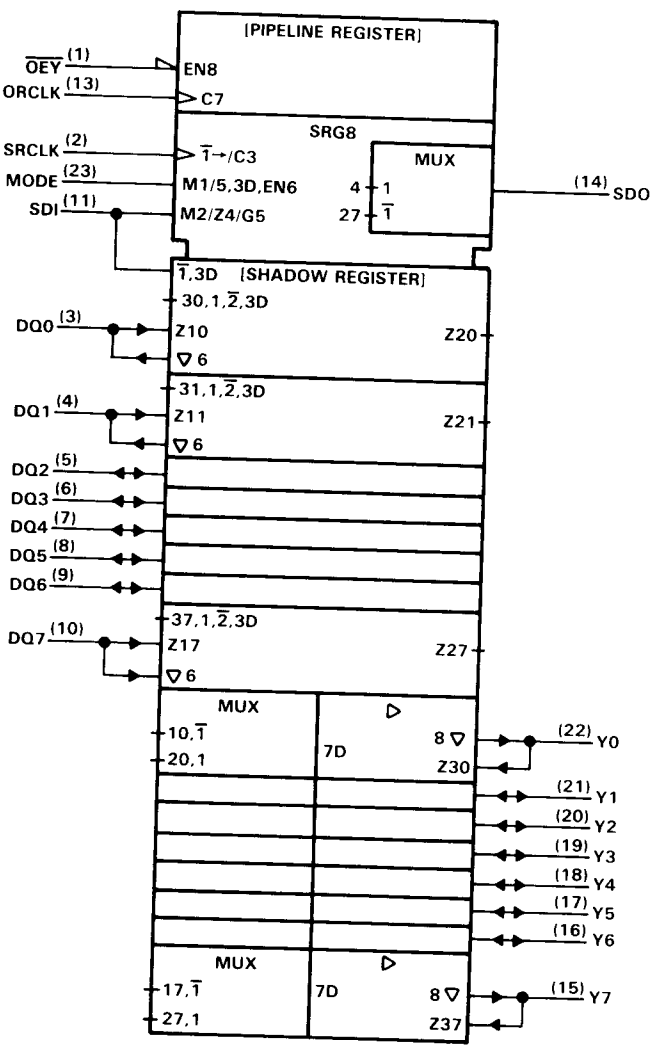
logic symbols†

'ALS819



'ALS29818



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

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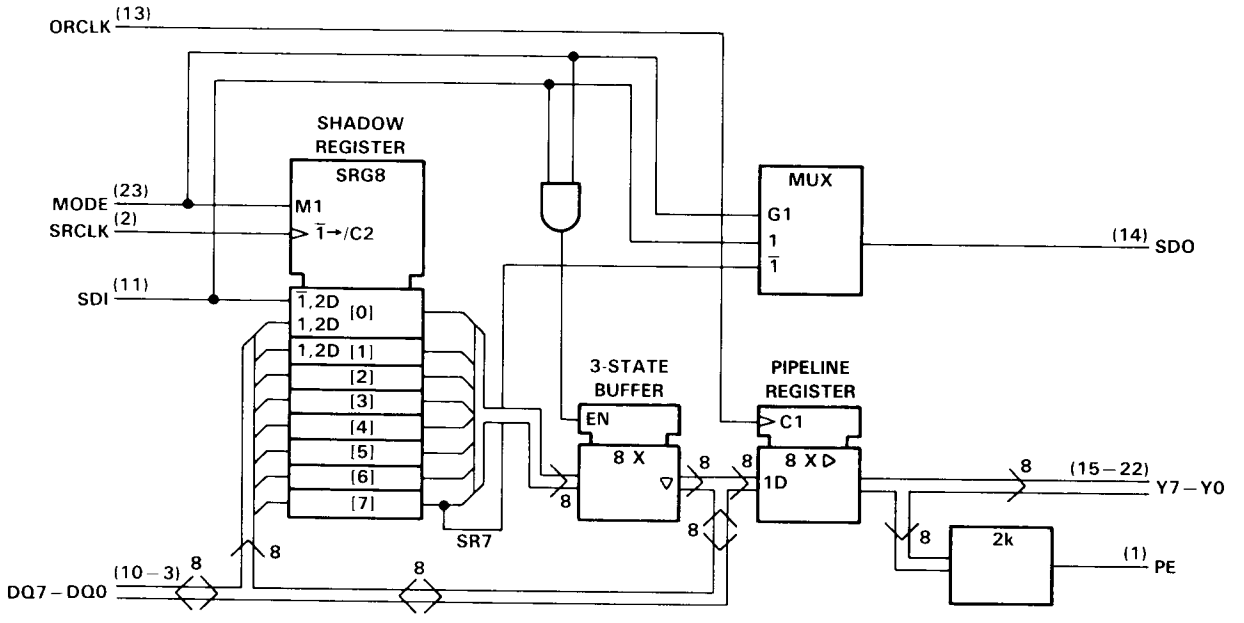
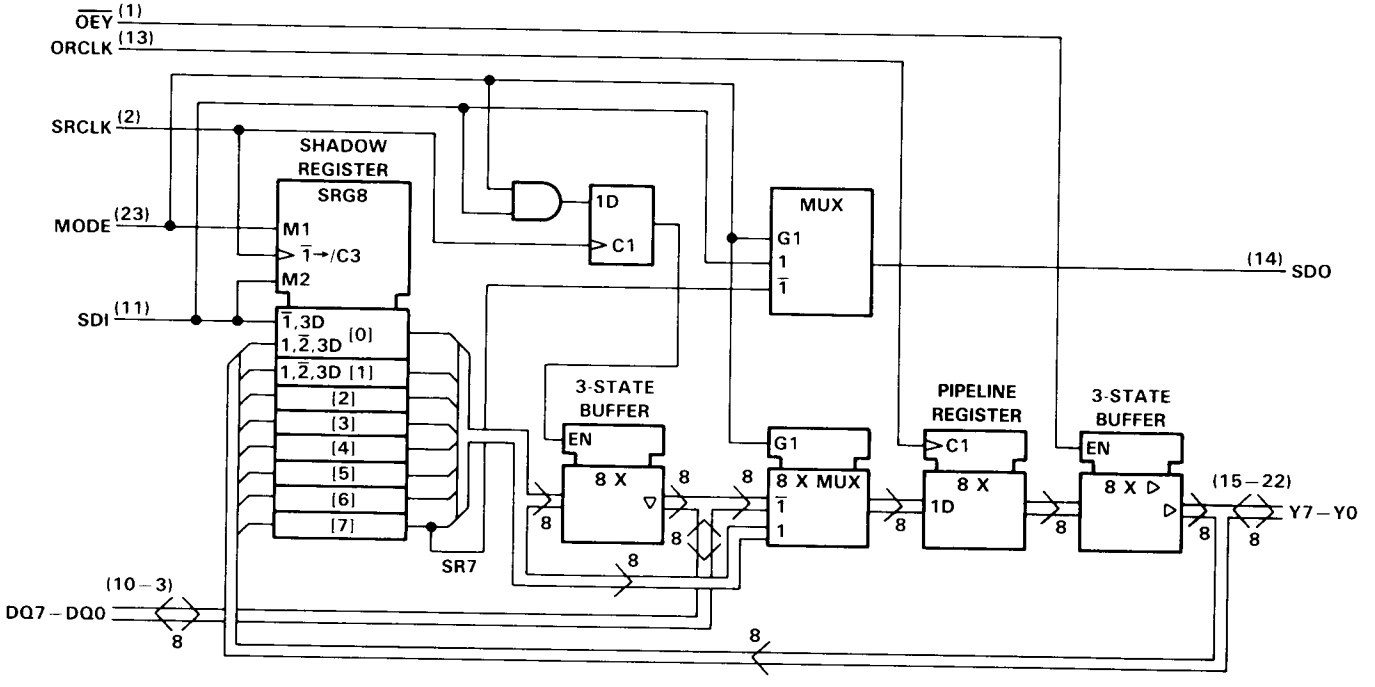
logic diagrams (positive logic)

'ALS819

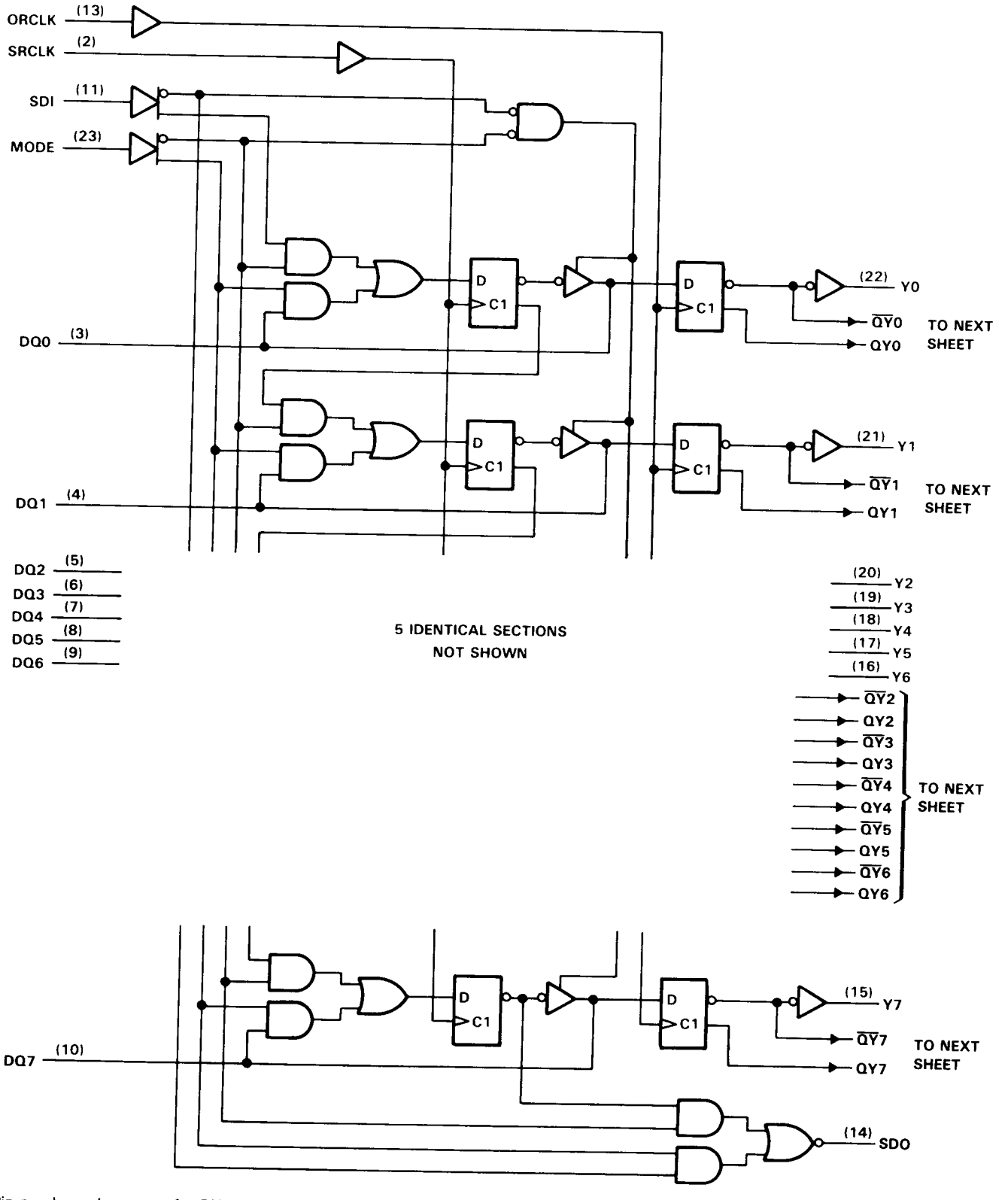


'ALS29818



Pin numbers shown are for DW and NT packages.

'ALS819 gate-level logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

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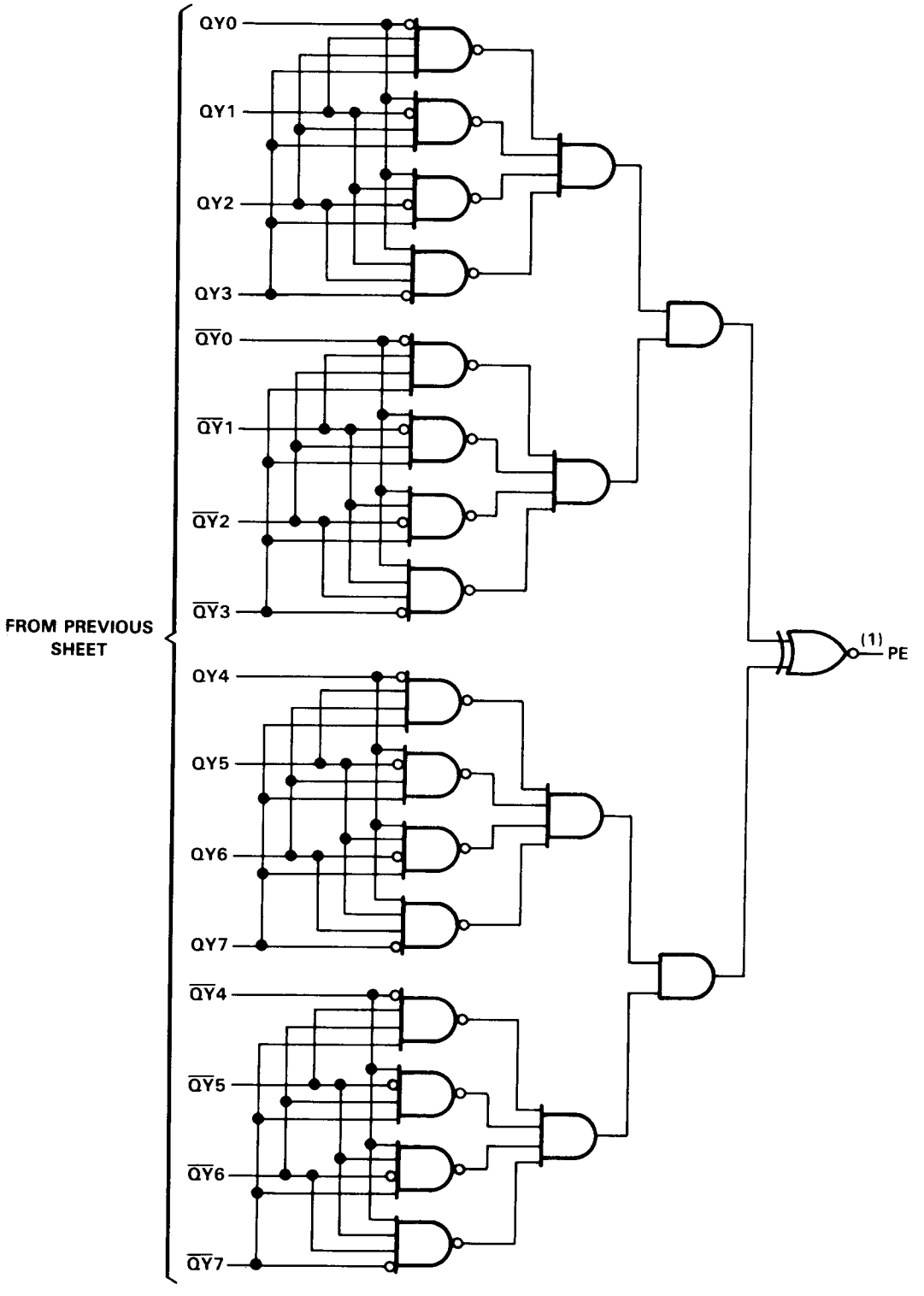
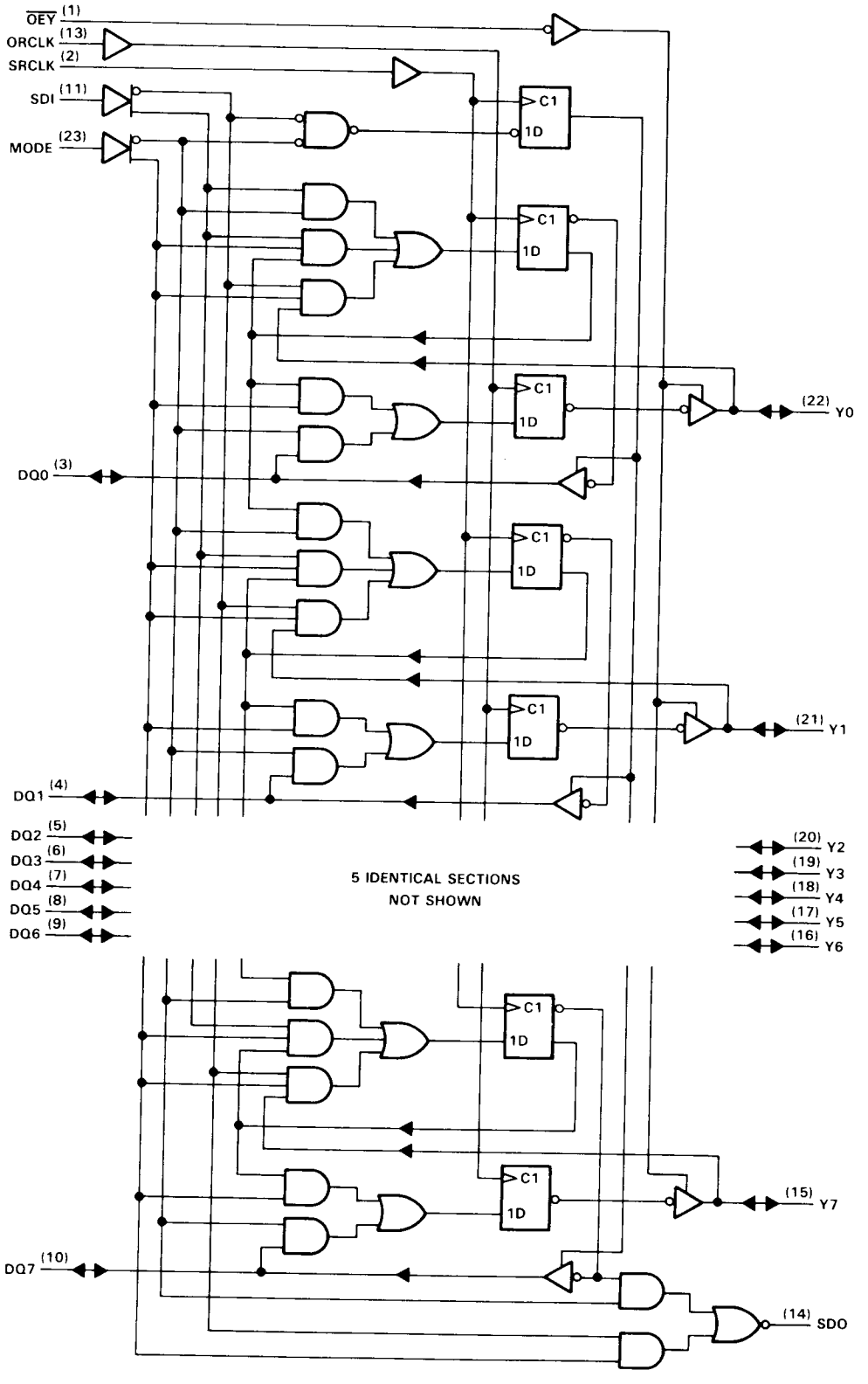
'ALS819 gate-level logic diagram (positive logic) (continued)



Pin numbers shown are for DW and NT packages.

'ALS29818 gate-level logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

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'ALS819 FUNCTION TABLE

INPUTS				OUTPUT AND I/O			OPERATION OR FUNCTION
MODE	SDI	SRCLK	ORCLK	SDO	Y0–Y7 PE	DQ0–DQ7	
L	X	↑	X	SR7	OUTPUT	HI-Z	Serial input, shift right
H	L	↑	X	SDI (L)	OUTPUT	INPUT	Parallel load shadow register from DQ0–DQ7
H	L	↑	↑	SDI (L)	OUTPUT	INPUT	Parallel load shadow register and pipeline register from DQ0–DQ7
L X	X L	X X	↑ ↑	SR7 –	OUTPUT	INPUT	Load pipeline register from DQ0–DQ7
L	X	↑	↑	SR7	OUTPUT	INPUT	Load pipeline register from DQ0–DQ7 while shifting shadow register
H	H	No ↑	↑	SDI (H)	OUTPUT	OUTPUT	Load pipeline register from shadow register
H	X	X	X	SDI	OUTPUT	–	Serial data in to serial data out
H	H	X	X	SDI (H)	OUTPUT	OUTPUT HOLD	Hold shadow register, enable DQ0–DQ7, transitions on SRCLK ignored
L X	X L	X X	X X	SR7 –	OUTPUT	HI-Z	Disable DQ0–DQ7 outputs

'ALS29818 FUNCTION TABLE

INPUTS					OUTPUT AND I/O			OPERATION OR FUNCTION
MODE	$\overline{OEY}$	SDI	SRCLK	ORCLK	SDO	Y0–Y7	DQ0–DQ7	
L	X	X	↑	X	SR7	–	HI-Z	Serial input, shift right, disable DQ0–DQ7
H	H	L	↑	X	SDI (L)	INPUT	HI-Z	Parallel load shadow register from Y0–Y7, disable DQ0–DQ7
H	L	L	↑	No ↑	SDI (L)	OUTPUT	HI-Z	Parallel load shadow register from pipeline register, disable DQ0–DQ7
L	X	X	X	↑	SR7	–	INPUT†	Load pipeline register from DQ0–DQ7
L	X	X	↑	↑	SR7	–	INPUT†	Load pipeline register from DQ0–DQ7 while shifting shadow register
H	X	X	No ↑	↑	SDI	–	–	Load pipeline register from shadow register
H	X	X	X	X	SDI	–	–	Serial data in to serial data out
H	L	L	↑	↑	SDI (L)	OUTPUT	HI-Z	Exchange data between registers, DQ0–DQ7 disabled
H	X	H	X	X	SDI (H)	–	–	Hold shadow register, transitions on SRCLK do not effect shadow register
H	X	H	↑	X	SDI (H)	–	OUTPUT	Enable DQ0–DQ7 for parallel shadow register output

†The DQ0–DQ7 outputs must be disabled before applying data to DQ0–DQ7.

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, any input or I/O port . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Y0–Y7, PE			−3	mA
		All others			−1	
I_{OL}	Low-level output current	Y0–Y7, PE			24	mA
		All others			8	
t_w	Pulse duration	SRCLK high or low	25			ns
		ORCLK high or low	15			
t_{su}	Setup time before SRCLK↑	Y0–Y7 ('ALS29818)†	5			ns
		MODE	12			
		SDI	10			
		ORCLK ('ALS29818)†	40			
t_{su}	Setup time before ORCLK↑	DQ0–DQ7	8			ns
		MODE ('ALS29818)†	15			
		SRCLK‡	15			
t_h	Hold time after SRCLK↑	Y0–Y7 ('ALS29818)†	5			ns
		MODE	2			
		SDI	0			
t_h	Hold time after ORCLK↑	DQ0–DQ7	2			ns
		MODE ('ALS29818)†	0			
		SDI ('ALS819)	0			
T_A	Operating free-air temperature		0		70	°C

† This setup time ensures that the shadow register will see stable data from the output register.
‡ This setup time ensures that the output register will see stable data from the shadow register.

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electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	Y0−Y7, PE	V_{CC} = 4.75 V,	I_{OH} = −3 mA	2.4	3.2		V
	All others	V_{CC} = 4.75 V,	I_{OH} = −1 mA	2.4	3.2		
V_{OL}	Y0-Y7, PE	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.35	0.5	V
	All others	V_{CC} = 4.75 V,	I_{OL} = 8 mA		0.35	0.5	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.4 V			20	μA
I_{IL}‡	MODE, SDI	V_{CC} = 5.25 V,	V_I = 0.5 V			−0.2	mA
	All others					−0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0	−75		−250	mA
I_{CC}	'ALS819	V_{CC} = 5.25 V,	See Note 1		65	100	mA
	'ALS29818				85	120	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with all three-state outputs in the high-impedance state.

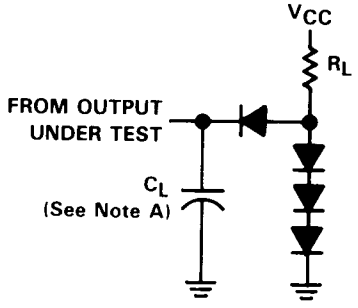
'ALS819 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	MODE	SDO	R_L = 2 kΩ		10	14	4	16	ns
t_{PHL}					8	11	4	13	
t_{PLH}	SDI	SDO	R_L = 2 kΩ		13	17	7	20	ns
t_{PHL}					10	14	5	16	
t_{PLH}	ORCLK	Y0-Y7	R_L = 2 kΩ		10	14	4	16	ns
t_{PHL}					9	12	4	14	
t_{PLH}	ORCLK	PE	R_L = 2 kΩ		25	32	10	45	ns
t_{PHL}					16	20	8	25	
t_{PLH}	SRCLK	SDO	R_L = 2 kΩ		14	18	7	22	ns
t_{PHL}					9	12	5	15	
t_{PZH}	MODE or SDI	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		11	15	5	17	ns
t_{PZL}					14	19	8	20	
t_{PHZ}	MODE or SDI	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		48	75	23	80	ns
t_{PLZ}					21	29	12	35	

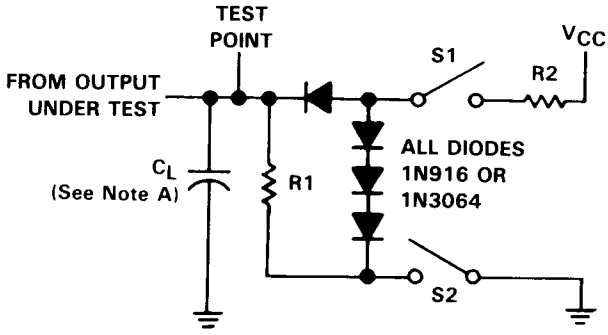
'ALS29818 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	MODE	SDO	R_L = 2 kΩ		10	14		16	ns
t_{PHL}					10	14		16	
t_{PLH}	SDI	SDO	R_L = 2 kΩ		10	14		16	ns
t_{PHL}					10	14		16	
t_{PLH}	ORCLK	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		10	12		13	ns
t_{PHL}					10	12		13	
t_{PLH}	SRCLK	SDO	R_L = 2 kΩ		12	18		25	ns
t_{PHL}					9	14		20	
t_{PZH}	SRCLK	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		13	20		25	ns
t_{PZL}					16	25		30	
t_{PHZ}	SRCLK	DQ0-DQ7	R1 = 5 kΩ, R2 = 2 kΩ		52	80		85	ns
t_{PLZ}					21	33		45	
t_{PHZ}	$\overline{OEY}$	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		12	19		25	ns
t_{PLZ}					8	12		15	
t_{PZH}	$\overline{OEY}$	Y0-Y7	R1 = 1 kΩ, R2 = 280 Ω		7	12		15	ns
t_{PZL}					11	15		15	

PARAMETER MEASUREMENT INFORMATION



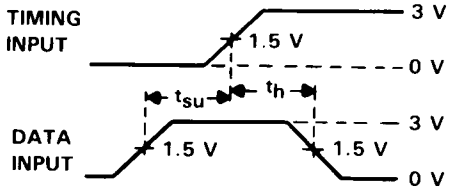
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



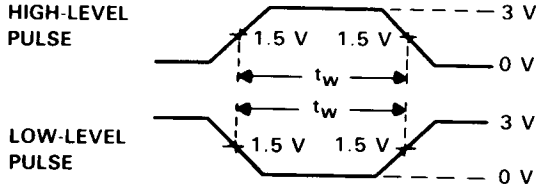
LOAD CIRCUIT FOR THREE-STATE OUTPUTS

SWITCH POSITION TABLE

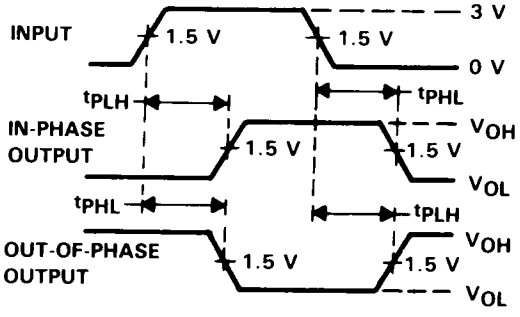
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



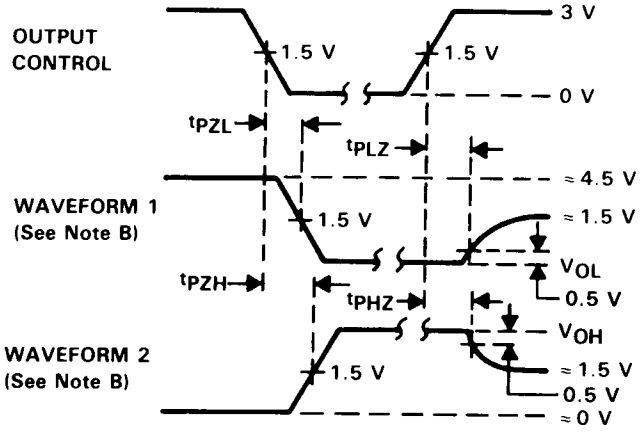
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1