

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1 μW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Industrial temperature: -40°C to +85°C
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Std., A, and C speed grades: 4.1ns t_{PD} for C

FCT16244T

- High drive standard FCT-T outputs:
 $I_{OL} = +64mA$, $I_{OH} = -32mA$
- Incident switching for driving buses and large loads

FCT162244T

- Balanced output drivers: ±24mA
- Reduced switching noise for point to point signals

DESCRIPTION

The FCT16244 family of products are 16-bit bus interface buffers with three-state outputs that are ideal for driving address and data buses. Output enables are used to enable or disable A and B ports by placing them in a high impedance condition. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product were designed not to load an active bus when V_{CC} is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162244 is recommended.

Figure 1. Functional Block Diagram

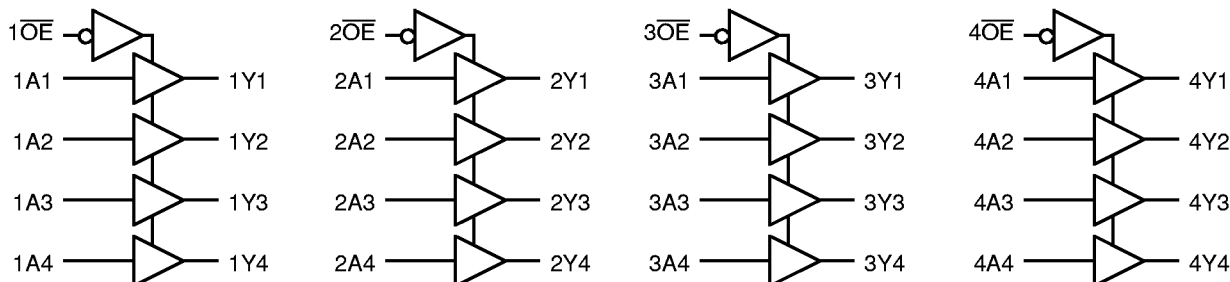


Figure 2. Pin Configuration (All Pins Top View)

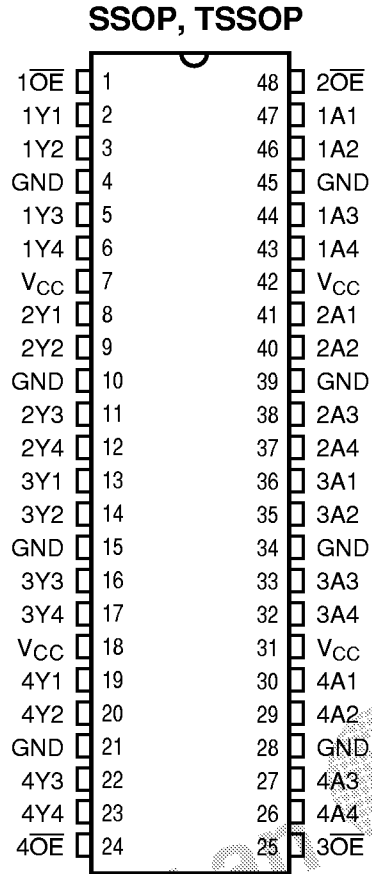


Table 1. Pin Description

Name	Description
\overline{xOE}	3-State Output Enable Inputs
xAx	Data Inputs
xYx	3-State Outputs

Table 2. Function Table

Inputs		Outputs
\overline{xOE}	xAx	xYx
L	L	L
L	H	H
H	X	Hi-Z

Table 3. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	Typ	Max	Unit
All	6.0	9.0	pF

Note: Capacitance is characterized but not tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.0 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	-0.5	5.5	V
V_{OUT}	Voltage Applied to Output or I/O	0	Vcc	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	-40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs ⁽⁴⁾	—	100	—	mV
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	1	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{OUT} \leq V_{CC}$	—	—	1	μA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(3,4)}$	-80	-140	-200	mA
V_{IK}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
3. Not more than one output should be tested at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not tested.

Table 7. Output Drive Characteristics for FCT16244T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit	
I_O	Output Drive Current	$V_{CC} = \text{Max}, V_{OUT} = 2.5V^{(3)}$	-50	—	-180	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3mA$	2.5	—	—	V
			$I_{OH} = -15mA$	2.4	—	—	V
			$I_{OH} = -32mA^{(4)}$	2.0	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64mA$	—	0.25	0.55	V
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$	—	—	± 1.0	μA	

Table 8. Output Drive Characteristics for FCT162244T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit	
I_{ODL}	Output LOW Current	$V_{CC} = 5V, V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 1.5V^{(3)}$	60	115	200	mA	
I_{ODH}	Output HIGH Current	$V_{CC} = 5V, V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 1.5V^{(3)}$	-60	-115	-200	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -24mA$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24mA$	—	0.3	0.55	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.
3. Not more than one output should be shorted and the duration is ≤ 1 second.
4. Duration of the condition should not exceed one second.

Table 9. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit	
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, \text{Freq} = 0$ $V_{IN} = \text{GND or } V_{CC}$	5	500	μA	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}^{(3)}$	0.5	1.5	mA	
Q_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ One Bit Toggling @ 50% Duty Cycle $x\overline{OE} = \text{GND}$	60	100	$\mu\text{A}/\text{MHz}$	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ One Bit Toggling @ 50% Duty Cycle $x\overline{OE} = \text{GND}, f_I = 10\text{MHz}$	$V_{IN} = V_{CC}$	0.6	1.5	mA
			$V_{IN} = \text{GND}$			
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ Sixteen Bits Toggling @ 50% Duty Cycle $x\overline{OE} = \text{GND}, f_I = 2.5\text{MHz}$	$V_{IN} = 3.4\text{V}$	0.9	2.3	mA
			$V_{IN} = \text{GND}$			
		$V_{IN} = V_{CC}$	2.4	4.5 ⁽⁵⁾	mA	
		$V_{IN} = \text{GND}$	6.4	16.5 ⁽⁵⁾	mA	

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}, +25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$). All Other Inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} = I_{\text{DYNAMIC}}$
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_I N_I)$
 I_{CCQ} = Quiescent Current ($I_{CCL}, I_{CCH},$ and I_{CCZ}).
 ΔI_{CC} = Power Supply Current for a TTL-High Input ($V_{IN} = 3.4\text{V}$).
 D_H = Duty Cycle for TTL High Inputs.
 N_T = Number of TTL High Inputs.
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
 f_{CP} = Clock Frequency for Register devices (Zero for Non-Register Devices).
 N_{CP} = Number of Clock Inputs at f_{CP} .
 f_I = Input Frequency.
 N_I = Number of Inputs at f_I .

Table 10. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.


Symbol	Description ⁽¹⁾	FCT16244T FCT162244T		FCT16244AT FCT162244AT		FCT16244CT FCT162244CT		Unit
		Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay xAx to xYx	1.5	6.5	1.5	4.8	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time x \overline{OE} to xYx	1.5	8.0	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾ x \overline{OE} to xYx	1.5	7.0	1.5	5.6	1.5	5.2	ns
$t_{SK(O)}$	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.

2. Guaranteed by design, but not tested.

3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design but not tested.

Now an  IDT company