High-Speed CMOS QuickSwitch® 16 to 8 Multiplexer

QS3390
QS32390

FEATURES/BENEFITS

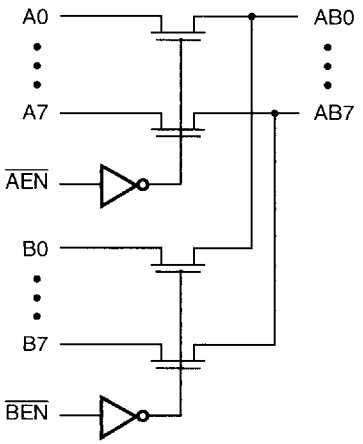
- 16:8 multiplexer function with zero delay
- 5Ω switches connect inputs to outputs
- Zero propagation delay
- Low power CMOS proprietary technology
- TTL compatible control inputs
- Direct connection for mux, demux
- QS32390 is 25Ω version for low noise
- Zero ground bounce in flow-through mode
- Available in 28-pin DIP, SOIC (SO) & QSOP

DESCRIPTION

The QS3390 and QS32390 each provide a 16 to 8 multiplexer logic switch. The low ON resistance (5Ω) of the QS3390 allows inputs to be connected to the output without adding propagation delay and without generating additional ground bounce noise. The QS32390 adds an internal 25Ω resistor to reduce reflection noise in high-speed applications. The select and enable inputs select and connect one of eight inputs to the common I/O pin, respectively. The multiplexer function can be used to select and route logic signals for zero delay, isolate bus capacitance, form crossbar switches, etc.

5

FUNCTIONAL BLOCK DIAGRAM

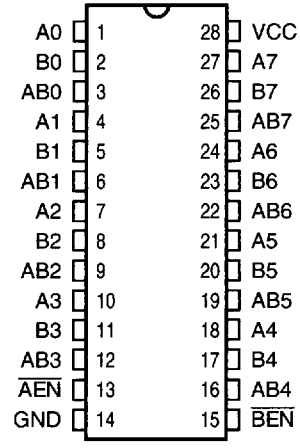


PIN DESCRIPTION

Name	I/O	Description
A9-A0	I/O	Bus A
B9-B0	I/O	Bus B
$\overline{AEN}$, $\overline{BEN}$	I	Bus Switch Enable

PIN CONFIGURATION (All Pins Top View)

PDIP, SOIC (SO), QSOP



FUNCTION TABLE

$\overline{AEN}$	$\overline{BEN}$	A Sw	B Sw	Function
H	H	Off	Off	Disconnect
L	H	On	Off	A to AB
H	L	Off	On	B to AB
L	L	On	On	A, B to AB

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground ..... –0.5V to +7.0V
DC Switch Voltage Vs ..... –0.5V to +7.0V
DC Input Voltage V_{IN} ..... –0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns) ..... –3.0V
DC Output Current Max. Sink Current/Pin ..... 120 mA
Maximum Power Dissipation ..... 0.5 watts
T_{STG} Storage Temperature ..... –65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Name	Discription	Conditions	SOIC	QSOP	PDIP	Unit
C_{IN}	Input Capacitance, Controls	V_{IN} = 0V	6	6	7	pF
C_{OFF}	A, B, AB I/O Capacitance, Switch Off	V_{IN} = 0V	8	8	8	pF

Note: Capacitance is characterized but not tested and the values are typical.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

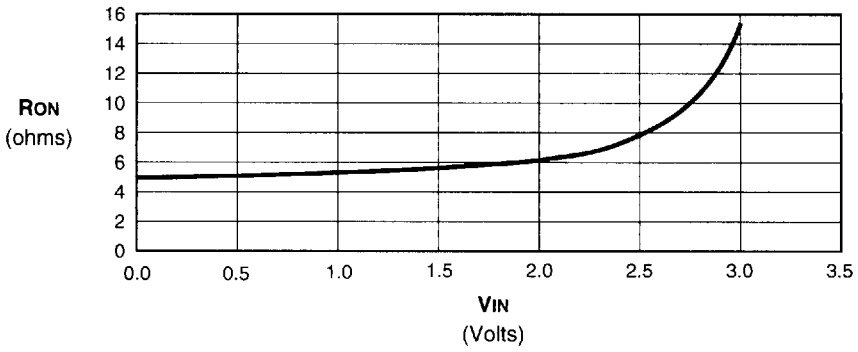
Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)(2)	$0 \le A, B, AB \le V_{CC}$		—	—	1	µA
R_{ON}	Switch ON Resistance(4,5)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 30 mA	3390 32390	— 20	5 28	7 40	Ω
R_{ON}	Switch ON Resistance(4,5)	V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15 mA	3390 32390	— 24	10 35	15 48	Ω

5

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the $\overline{G}$ control is HIGH.
3. Measured by voltage drop between A or B pins to AB pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
4. Max. value R_{ON} guaranteed but not tested.

Typical ON Resistance vs V_{IN} at 4.75 Vcc (3390 Only)



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc, f = 0	30	µA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	Vcc = Max., V_{IN} = 3.4V, f = 0 per Control Input	3.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	Vcc = Max., A, B, AB Pins Open, Control InputsToggling @ 50% Duty Cycle	0.25	mA/ MHz
Ic	Total Power Supply Current[4,5]	Vcc = Max., A, B, AB Pins at 0.0V, Control InputsToggling @ 50% Duty Cycle Vih = 3.4V, f Clock + MHz	9.0	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A, B, and AB pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, and AB I/Os generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
4. Ic = I Quiescent + I Inputs + I Dynamic.
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + Q_{CCD} (f_i N_i)$.
   I_{CC} = Power Supply Current for each TTL HIGH input (V_{IN} = 3.4V, control inputs only).
   D_H = Duty Cycle for each TTL input that is HIGH (control inputs only).
   N_T = Number of TTL inputs that are at D_H (control inputs only).
   f_i = frequency that the inputs are toggled (control inputs only).
5. Note that activity on A, B, and AB I/Os do not contribute to Ic if A, B, and AB I/Os are between GND and Vcc. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A, B, and AB I/Os.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	QS3390 Min	QS3390 Typ	QS3390 Max	QS32390[7] Min	QS32390[7] Typ	QS32390[7] Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,4] A,B to/from AB	—	0.25[3]	—	—	1.25	—	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay[1] $\overline{AEN}/\overline{BEN}$ to A, B, AB	1.5	—	6.5	1.5	—	7.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[1,2] $\overline{AEN}/\overline{BEN}$ to A, B, AB	1.5	—	5.5	—	—	5.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection[5]	—	1.5	—	—	1.5	—	pC

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The time constant for the switch alone is of the order of 0.25 ns for 50 pF.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, A/B to AB, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at $\overline{AEN}/\overline{BEN}$ = 0.0V.
6. Characterized parameter but not tested.
7. Preliminary data, subject to change.